09-01-2000

101448962

FORM PTO-1618A
Expires 06/30/99
OMB 0651-0027

U.S. Department of Commerce
Patent and Trademark Office
TRADEMARK

RECORDATION FORM COVER SHEET
TRADEMARKS ONLY

TO: The Commissioner of Patents and Trademarks: Please record the attached original document(s) or copy(ies).

Submission Type

[xx] New

[ ] Resubmission (Non-Recordation) Document ID #

[ ] Correction of PTO Error Reel # Frame #

[ ] Corrective Document Reel # Frame #

Conveyance Type

[xx] Assignment [ ] License

[ ] Security Agreement [ ] Nunc Pro Tunc Assignment

[ ] Merger Effective Date Month Day Year: 04 07 00

[ ] Change of Name

[ ] Other

Conveying Party

[ ] Mark if additional names of conveying parties attached

Name: World Access, Inc.

Execution Date Month Day Year: 05 29 00

Formerly:

[ ] Individual [ ] General Partnership [ ] Limited Partnership [xx] Corporation [ ] Association

[ ] Other

[xx] Citizenship/State of Incorporation/Organization: Delaware

Receiving Party

[ ] Mark if additional names of receiving parties attached

Name: BATM Advanced Communications Limited

DBA/AKA/TA:

Composed of:

Address (line 1): 22 Hamelacha Street, Building 4

Address (line 2): Cible Industrial Park, P.O.B 11387

Address (line 3): Ros Ha'ayn 48091 (City) Israel (State/Country) (Zip Code)

[ ] Individual [ ] General Partnership [ ] Limited Partnership [ ] If document to be recorded is an assignment and the receiving party is not domiciled in the United States, an appointment of a domestic representative should be attached. *(Designation must be a separate document from Assignment.)*

[xx] Corporation [ ] Association

[ ] Other

[X] Citizenship/State of Incorporation/Organization: Israeli

FOR OFFICE USE ONLY

08/31/2000 MTHAI1 00000002 75775025

01 FC:481 40.00 OP

02 FC:482 575.00 OP

00000077 75775025

$615.00

Refund Req 08/31/2000 MTHAI1

CHECK Detail

Public burden reporting for this collection of information is estimated to average approximately 30 minutes per Cover Sheet to be recorded, including time for reviewing the document and gathering the data needed to complete the Cover Sheet. Send comments regarding this burden estimate to the U.S. Patent and Trademark Office, Chief Information Officer, Washington, D.C. 20231 and to the Office of Information and Regulatory Affairs, Office of Management and Budget, Paperwork Reduction Project (0651-0027), Washington, D.C. 20503. See OMB Information Collection Budget Package 0651-0027, Patent and Trademark Assignment Practice. DO NOT SEND REQUESTS TO RECORD ASSIGNMENT DOCUMENTS TO THIS ADDRESS.

Mail documents to be recorded with required cover sheet(s) information to:
Commissioner of Patents and Trademarks, Box Assignments, Washington, D.C. 20231

Domestic Representative Name and Address

Enter for the first Receiving Party only.

Name: John M. McCafferty, Esquire

Address (line 1): Klehr, Harrison, Harvey, Branzburg & Ellers LLP

Address (line 2): 260 South Broad Street

Address (line 3): Philadelphia, PA 19102-5003

Address (line 4):

Correspondent Name and Address

Area Code and Telephone Number: 215-569-2524

Name: John M. McCafferty, Esquire

Address (line 1): Klehr, Harrison, Harvey, Branzburg & Ellers LLP

Address (line 2): 260 South Broad Street

Address (line 3): Philadelphia, PA 19102-5003

Address (line 4):

Pages

Enter the total number of pages of the attached conveyance document including any attachments. # 113

Trademark Application Number(s) or Registration Number(s)

☐ Mark if additional numbers attached

Enter either the Trademark Application Number or the Registration Number (DO NOT ENTER BOTH numbers for the same property).

Trademark Application Number(s)			Registration Number(s)		
75-775,025			2,220,814	2,165,641	1,936,449
75-679,515			2,200,340	2,075,965	1,924,529
75-395,104			2,195,021	1,985,921	1,915,794

Number of Properties

Enter the total number of properties involved. # 24

Fee Amount

Fee Amount for Properties Listed (37 CFR 3.41): $ 960.00

Method of Payment: Enclosed ☒ Deposit Account ☐

Deposit Account

(Enter for payment by deposit account or if additional fees can be charged to the account.)

Deposit Account Number: #

Authorization to charge additional fees: Yes ☐ No ☐

Statement and Signature

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document. Charges to deposit account are authorized, as indicated herein.

John M. McCafferty — Name of Person Signing

John M. McCafferty — Signature

7/31/00 — Date Signed

FORM PTO-1618C
Expires 06/30/99
OMB 0651-0027

RECORDATION FORM COVER SHEET
CONTINUATION
TRADEMARKS ONLY

U.S. Department of Commerce
Patent and Trademark Office
TRADEMARK

Conveying Party
Enter Additional Conveying Party

☐ Mark if additional names of conveying parties attached

Execution Date
Month Day Year

Name

Formerly

☐ Individual ☐ General Partnership ☐ Limited Partnership ☐ Corporation ☐ Association

☐ Other

☐ Citizenship State of Incorporation/Organization

Receiving Party
Enter Additional Receiving Party

☐ Mark if additional names of receiving parties attached

Name

DBA/AKA/TA

Composed of

Address (line 1)

Address (line 2)

Address (line 3)

City State/Country Zip Code

☐ Individual ☐ General Partnership ☐ Limited Partnership

☐ Corporation ☐ Association

☐ Other

☐ If document to be recorded is an assignment and the receiving party is not domiciled in the United States, an appointment of a domestic representative should be attached *(Designation must be a separate document from the Assignment.)*

☐ Citizenship/State of Incorporation/Organization

Trademark Application Number(s) or Registration Number(s)

☐ Mark if additional numbers attached

Enter either the Trademark Application Number or the Registration Number (DO NOT ENTER BOTH numbers for the same property).

Trademark Application Number(s)			Registration Number(s)		
			1,852,966	1,591,782	
			1,851,901	1,583,359	
			1,796,171	1,568,157	
			1,796,170	1,533,998	
			1,794,164	1,527,891	
			1,749,260		
			1,616,521		

ASSIGNMENT OF OWNERSHIP IN PATENTS, TRADEMARKS AND COPYRIGHTS

THIS AGREEMENT, entered this 7th day of April, 2000 (the "Effective Date"), by and between World Access, Inc., a Delaware corporation having its principal place of business in Atlanta, Georgia ("Assignor") and BATM Advanced Communications Limited, an Israeli corporation having its principal place of business in Ros Ha'ayn, Israel ("Assignee").

WHEREAS, pursuant to that Stock Purchase Agreement between the parties with an effective date of February 2, 2000, the parties desire to effect the transfer from Assignor to Assignee of all right, title and interest of Assignor in that intellectual property described below.

NOW, THEREFORE, for good and valuable consideration, the receipt of which is hereby acknowledged, the parties agree as follows:

ARTICLE 1 - ASSIGNMENT OF ALL PATENTS

1.1 Assignor hereby sells, assigns, transfers and sets over, to Assignee, its lawful successors and assigns, Assignor's entire right, title and interest in and to the U.S. Patents listed on Schedule A (the "Patents"), the inventions claimed therein, any other patent applications directed to the inventions, and all Letters Patent of the United States that may be granted thereon, and all reissues, reexaminations, and extensions thereof, and all priority rights under the International Convention for the Protection of Industrial Property for every member country, and all applications for patents (including related rights such as utility-model registrations, inventor's certificates, and the like) heretofore or hereafter filed for the inventions in any foreign countries, and all patents (including all extensions, renewals and reissues thereof) granted for said inventions in any foreign countries; and Assignor hereby authorizes and requests the United States Commissioner of Patents and Trademarks, and any officials of foreign countries whose duty it is to issue patents on applications as aforesaid, to issue all patents for said improvements to Assignee in accordance with the terms of this assignment;

1.2 Assignor hereby covenants that it has the full right to convey the entire interest herein assigned, that it will take all action and execute all documents necessary to perfect the interest assigned hereby and that it has not executed, and will not execute, any agreement in conflict herewith.

1.3 Assignor hereby further covenants and agrees that it will communicate to Assignee any facts known to Assignor, its officers and employees respecting the inventions, and testify in any legal proceeding, sign all lawful papers, execute and deliver all papers that may be necessary or desirable to perfect the title to the inventions in Assignee, its successors and assigns, execute all divisional, continuation, continuations-in-part, substitute and reissue applications, make all rightful oaths and generally do everything possible to aid Assignee to obtain and enforce proper patent protection for the inventions in all countries.

ARTICLE II - ASSIGNMENT OF ALL TRADEMARKS

2.1 Assignor hereby assigns irrevocably and in perpetuity to the Assignee any and all right, title and interest Assignor has in and to the trademarks, service marks, trade names, and all other intellectual property rights associated with the marks listed on Schedule B, any and all common law rights in the foregoing, and all goodwill associated therewith (the "Marks"). By executing this assignment, Assignor hereby waives and releases any and all rights that Assignor may have in such Marks and further

acknowledges and agrees that Assignor has no claims against nor will Assignor assert any claims against the Assignee, its affiliates, officers, directors, agents, employees, and attorneys with respect to the Marks or any use of the Marks. Additionally, Assignor represents and warrants that the Assignor has not assigned or attempted to assign any rights in and to the Marks to any party other than Assignee.

2.2 Assignor hereby assigns to Assignee all unsatisfied claims for damages by reason of past infringement of said trademark, with the right to sue for such damages and collect the same for its own use and benefit and for the use and benefit of its successors, assignees or other legal representatives.

ARTICLE III - FURTHER ASSURANCES

3.1 At any time and from time to time from and after the execution of this Assignment, Assignor will, at the request of Assignee, execute, acknowledge and deliver, or cause to be executed, acknowledged and delivered, such instruments and other documents and perform or cause to be performed such acts and provide such information, as may reasonably be required, to evidence or effectuate the purpose of this Assignment by Assignor to Assignee of any and all right, title and interest in and to the intellectual property assigned hereunder.

[Signatures begin on the following page]

IN WITNESS WHEREOF, the parties have hereunto set their hand by their duly authorized agents.

WORLD ACCESS, INC., as Assignor

By: MAGergel
Print Name: MARK A. GERGEL
Title: EXECUTIVE VICE PRESIDENT

Before me this 7th day of April, 2000, personally appeared MARK A. GERGEL, known to me to be the person who executed the foregoing Assignment on behalf of World Access, Inc. and acknowledged to me that he executed the same of his own free will for the purpose therein expressed.

Annette Trippe
Notary Public

[Signatures continued on next page]

ANNETTE TRIPPE NOTARY PUBLIC COBB COUNTY GEORGIA EXPIRES JULY 07, 2003

IN WITNESS WHEREOF, the parties have hereunto set their hand by their duly authorized agents.

WORLD ACCESS, INC., as Assignor

By: MAGersel
Print Name: MARK A. GERGEL
Title: Executive Vice President

Before me this 7th day of April, 2000, personally appeared MARK A. GERGEL, known to me to be the person who executed the foregoing Assignment on behalf of World Access, Inc. and acknowledged to me that he executed the same of his own free will for the purpose therein expressed.

Annette Trippe
Notary Public

[Signatures continued on next page]

ANNETTE TRIPPE NOTARY PUBLIC COBB COUNTY EXPIRES GEORGIA JULY 07, 2003

BATM ADVANCED COMMUNICATIONS LIMITED,
as Assignee

By: _____
Print Name: OFER BAR-NER
Title: CFO

Before me this 29TH day of ~~April~~ MAY, 2000, personally appeared OFER BAR-NER, known to me to be the person who executed the foregoing Assignment on behalf of BATM Advanced Communications Limited, and acknowledged to me that he executed the same of his own free will for the purpose therein expressed.

_____
Notary Public

BATM ADVANCED COMMUNICATIONS LIMITED,
as Assignee

By: _____
Print Name: OFER BAR-NER
Title: CFO

Before me this 29th day of ~~April~~ MAY, 2000, personally appeared OFER BAR-NER, known to me to be the person who executed the foregoing Assignment on behalf of BATM Advanced Communications Limited, and acknowledged to me that he executed the same of his own free will for the purpose therein expressed.

_____
Notary Public

BATM ADVANCED COMMUNICATIONS LIMITED,
as Assignee

By: C/A
Print Name: OFER BAR-NER
Title: CFO

Before me this 21st day of ~~April~~ MAY, 2000, personally appeared OFER BAR-NER, known to me to be the person who executed the foregoing Assignment on behalf of BATM Advanced Communications Limited, and acknowledged to me that he executed the same of his own free will for the purpose therein expressed.

Notary Public

ATLANTA:4190766.2

BATM ADVANCED COMMUNICATIONS LIMITED,
as Assignee

By: _____
Print Name: OFER BAR-NER
Title: CFO

Before me this 29th day of ~~April~~ MAY, 2000, personally appeared OFER BAR-NER, known to me to be the person who executed the foregoing Assignment on behalf of BATM Advanced Communications Limited, and acknowledged to me that he executed the same of his own free will for the purpose therein expressed.

_____
Notary Public

No. 11/2000 מס'

AUTHENTICATION OF SIGNATURE

אימות חתימה

I the undersigned, Arthur Moher, Adv.

Notary at Tel-Aviv, Israel

hereby certify that on 29/5/00
appeared before me Mr. Ofer Bar-Ner

whose identity was proved to me by I.D. No. 058748252 issued by Ministry of Interior
on 30.6.89

and signed of his own free will on the attached document marked "A"

In witness whereof I hereby authenticate the signature of the said Signee.

by my own signature and seal this 29.05.00

I.S. _____ Fees paid.

Notary's Seal and Signature.

אני הח"מ, ארתור מוהר, עו"ד

נוטריון בתל-אביב, ישראל

מאשר כי ביום 29.05.00
ניצב לפני במשרדי
מר עפר בר-נר

שזהותו הוכחה לי ע"י ת.ז.
מס' 058748252
שניתנה מאת משרד הפנים
ביום 30.6.89
וחתם מרצונו החופשי על המסמך
המצורף והמסומן באות א'

ולראיה הנני מאמת את חתימת
החותם הנ"ל

בחתימת ידי ובחותמי, היום 29.05.00

שכר בסך _____ שקל שולם.

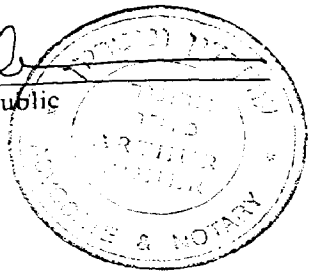
חתימה חותם הנוטריון

BATM ADVANCED COMMUNICATIONS LIMITED,
as Assignee

By: [signature]
Print Name: OFER BAR-NER
Title: CFO

Before me this 29th day of ~~April~~ MAY, 2000, personally appeared OFER BAR-NER, known to me to be the person who executed the foregoing Assignment on behalf of BATM Advanced Communications Limited, and acknowledged to me that he executed the same of his own free will for the purpose therein expressed.

[signature]
Notary Public



SCHEDULE A
(See Attached)

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

Help | Home | Marks | Boolean | Manual | Number | Order Copy | PTDLs

Searching ALL...

[Search Summary]
Results of Search in ALL for:
ON/"Telco Systems": 24 trademarks.
Hits 1 through 24 of 24

[redacted] on/"Telco Systems"

No.	Trademark
1.	2220814 -- EDGELINK
2.	2200340 -- ***TELCO SYSTEMS***
3.	2195021 -- LAN/WAN OPTIMIZER
4.	2165641 -- HYPERSPAN
5.	2075965 -- MICROFOX
6.	1985921 -- HYPERLYNX-50
7.	1936449 -- ***TELCO SYSTEMS***
8.	1924529 -- MICROFOX
9.	1915794 -- FOX T-BOX
10.	1852966 -- ACCESS60
11.	1851901 -- ACCESS30
12.	1796171 -- LAN/WAN OPTIMIZER
13.	1796170 -- HYPERSPAN 150
14.	1794164 -- ACCESS48 MUX
15.	1749260 -- T3-HUB
16.	1616521 -- FOX-3
17.	1591782 -- ROUTE-24
18.	1583359 -- TELTRAC
19.	1568157 -- MUXVIEW
20.	1533998 -- FOX 2
21.	1527891 -- FOX-2
22.	75-775025 -- WDSL
23.	75-679515 -- VOLTEDGE
24.	75-395104 -- RESPONSEEDGE

[redacted] on/"Telco Systems"

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE


(1 of 23)

Check Status

Word Mark	EDGELINK
Pseudo Mark	EDGE LINK
Owner Name	(REGISTRANT) ***Telco Systems, Inc.***
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	CHARLES E WEINSTEIN
Serial Number	75-202895
Registration Number	2220814
Filing Date	11/22/1996
Registration Date	01/26/1999
Section 1(B) indicator	SECTION 1 (B)
Mark Drawing Code	(1) TYPED DRAWING
Register	PRINCIPAL
Published for Opposition	01/20/1998
Type of Mark	TRADEMARK
International Class	009
Goods and Services	multiplexers; DATE OF FIRST USE: 1998.01.00; DATE OF FIRST USE IN COMMERCE: 1998.01.00


(1 of 23)

Thank you for your request. Here are the latest results.

Serial Number: 75202895

Registration Number: 2220814

Trademark (words only): EDGELINK

Current Status: Registered.

Date of Status: 1999-01-26

Filing Date: 1996-11-22

CURRENT OWNERS

1. Telco Systems, Inc.

GOODS AND SERVICES

multiplexers

PROSECUTION HISTORY

1999-01-26 - REGISTERED-PRINCIPAL REGISTER

1998-11-18 - ALLOWED PRINCIPAL REGISTER - SOU ACCEPTED

1998-11-18 - ASSIGNED TO EXAMINER

1998-11-17 - ASSIGNED TO EXAMINER

1998-11-09 - STATEMENT OF USE PROCESSING COMPLETE

1998-11-09 - EXTENSION 1 GRANTED

1998-10-14 - USE AMENDMENT FILED

1998-10-14 - EXTENSION 1 FILED

1998-04-14 - NOTICE OF ALLOWANCE-MAILED

1998-01-20 - PUBLISHED FOR OPPOSITION

1997-12-19 - NOTICE OF PUBLICATION

1997-11-10 - APPROVED FOR PUB - PRINCIPAL REGISTER

1997-11-03 - EXAMINERS AMENDMENT MAILED

1997-07-10 - NON-FINAL ACTION MAILED

1997-07-07 - ASSIGNED TO EXAMINER

1997-07-02 - ASSIGNED TO EXAMINER

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

Telco Systems

Word Mark	TELCO SYSTEMS
Owner Name	(REGISTRANT) *Telco Systems, Inc.*
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	CHARLES E WEINSTEIN
Serial Number	75-214534
Registration Number	2200340
Filing Date	12/17/1996
Registration Date	10/27/1998
Design Search Code	26.01.21; 26.17.09
Description of Mark	The stippling shown is a feature of the mark and is not intended to indicate color.
Section 1(B) indicator	SECTION 1 (B)
Mark Drawing Code	(3) DESIGN PLUS WORDS, LETTERS, AND/OR NUMBERS
Disclaimer	NO CLAIM IS MADE TO THE EXCLUSIVE RIGHT TO USE "SYSTEMS" APART FROM THE MARK AS SHOWN
Register	PRINCIPAL
Other Registration Info.	1936449

Published for Opposition	11/04/1997
Type of Mark	TRADEMARK
International Class	009
Goods and Services	digital lightwave transmission terminals for fiber-optic telecommunications transmission; bridges providing integration for multiple local area networks; multiplexers; transceivers; internetworking data compressors; computer software in the field of network management; fiber-optic telecommunications alarm and performance monitoring, remote control and diagnostic systems comprising a mini-computer operating in conjunction with micro-processors built into other equipment, a panel with CRT display, computer memories, keyboards, maintenance status indicators and computer printers; aluminum wall-mounted cabinets designed to hold fiber-optic telecommunications equipment; and user manuals sold as a unit; DATE OF FIRST USE: 1997.02.00; DATE OF FIRST USE IN COMMERCE: 1997.02.00

(2 of 23)

Thank you for your request. Here are the latest results.

Serial Number: 75214534

Registration Number: 2200340

Trademark (words only): TELCO SYSTEMS

Current Status: Registered.

Date of Status: 1998-10-27

Filing Date: 1996-12-17

CURRENT OWNERS

1. Telco Systems, Inc.

GOODS AND SERVICES

digital lightwave transmission terminals for fiber-optic telecommunications transmission; bridges providing integration for multiple local area networks; multiplexers; transceivers; internetworking data compressors; computer software in the field of network management; fiber-optic telecommunications alarm and performance monitoring, remote control and diagnostic systems comprising a mini-computer operating in conjunction with micro-processors built into other equipment, a panel with CRT display, computer memories, keyboards, maintenance status indicators and computer printers; aluminum wall-mounted cabinets designed to hold fiber-optic telecommunications equipment; and user manuals sold as a unit

PROSECUTION HISTORY

1998-10-27 - REGISTERED-PRINCIPAL REGISTER

1998-08-21 - ALLOWED PRINCIPAL REGISTER - SOU ACCEPTED

1998-08-11 - STATEMENT OF USE PROCESSING COMPLETE

1998-08-11 - EXTENSION 1 GRANTED

1998-07-27 - USE AMENDMENT FILED

1998-07-27 - EXTENSION 1 FILED

1998-01-27 - NOTICE OF ALLOWANCE-MAILED

1997-11-04 - PUBLISHED FOR OPPOSITION

1997-10-03 - NOTICE OF PUBLICATION

1997-08-21 - APPROVED FOR PUB - PRINCIPAL REGISTER

1997-08-19 - EXAMINERS AMENDMENT MAILED

1997-08-08 - ASSIGNED TO EXAMINER

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

(3 of 23)

Check Status

Word Mark	LAN/WAN OPTIMIZER
Owner Name	(REGISTRANT) *Telco Systems, Inc.*
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	CHARLES E WEINSTEIN
Serial Number	75-280067
Registration Number	2195021
Filing Date	04/23/1997
Registration Date	10/13/1998
Mark Drawing Code	(1) TYPED DRAWING
Register	PRINCIPAL-2(F)
Other Registration Info.	1796171
Published for Opposition	07/21/1998
Type of Mark	TRADEMARK
International Class	009
Goods and Services	internetworking data compressors and user manuals sold as a unit therewith; DATE OF FIRST USE: 1992.03.00; DATE OF FIRST USE IN COMMERCE: 1992.03.00

(3 of 23)

Thank you for your request. Here are the latest results.

Serial Number: 75280067

Registration Number: 2195021

Trademark (words only): LAN/WAN OPTIMIZER

Current Status: Registered.

Date of Status: 1998-10-13

Filing Date: 1997-04-23

CURRENT OWNERS

1. Telco Systems, Inc.

GOODS AND SERVICES

internetworking data compressors and user manuals sold as a unit therewith

PROSECUTION HISTORY

1998-10-13 - REGISTERED-PRINCIPAL REGISTER

1998-07-21 - PUBLISHED FOR OPPOSITION

1998-06-19 - NOTICE OF PUBLICATION

1998-05-01 - APPROVED FOR PUB - PRINCIPAL REGISTER

1998-04-10 - COMMUNICATION RECEIVED FROM APPLICANT

1998-01-08 - NON-FINAL ACTION MAILED

1997-12-05 - ASSIGNED TO EXAMINER

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

(4 of 23)

Check Status

Word Mark	HYPERSPAN
Pseudo Mark	HYPER SPAN
Owner Name	(REGISTRANT) *Telco Systems, Inc.*
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	CHARLES E WEINSTEIN
Serial Number	75-280064
Registration Number	2165641
Filing Date	04/23/1997
Registration Date	06/16/1998
Mark Drawing Code	(1) TYPED DRAWING
Register	PRINCIPAL
Other Registration Info.	1796170
Published for Opposition	03/24/1998
Type of Mark	TRADEMARK
International Class	009
Goods and Services	fiber-optic multiplexers and instruction manuals sold as a unit therewith; DATE OF FIRST USE: 1993.04.08; DATE OF FIRST USE IN COMMERCE: 1993.04.08

(4 of 23)

Thank you for your request. Here are the latest results.

Serial Number: 75280064

Registration Number: 2165641

Trademark (words only): HYPERSPAN

Current Status: Registered.

Date of Status: 1998-06-16

Filing Date: 1997-04-23

CURRENT OWNERS

1. Telco Systems, Inc.

GOODS AND SERVICES

fiber-optic multiplexers and instruction manuals sold as a unit therewith

PROSECUTION HISTORY

1998-06-16 - REGISTERED-PRINCIPAL REGISTER

1998-03-24 - PUBLISHED FOR OPPOSITION

1998-03-24 - PUBLISHED FOR OPPOSITION

1998-02-20 - NOTICE OF PUBLICATION

1998-01-25 - APPROVED FOR PUB - PRINCIPAL REGISTER

1998-01-08 - ASSIGNED TO EXAMINER

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

(5 of 23)

Check Status

Word Mark	MICROFOX
Owner Name	(REGISTRANT) *Telco Systems, Inc.*
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	Charles E. Weinstein
Serial Number	74-482641
Registration Number	2075965
Filing Date	01/25/1994
Registration Date	07/01/1997
Section 1(B) indicator	SECTION 1 (B)
Mark Drawing Code	(1) TYPED DRAWING
Register	PRINCIPAL
Other Registration Info.	1527891; 1616521
Published for Opposition	10/25/1994
Type of Mark	TRADEMARK
International Class	009
Goods and Services	fiber-optic telecommunications signal converter and user manuals sold as a unit; DATE OF FIRST USE: 1994.12.01; DATE OF FIRST USE IN COMMERCE: 1994.12.01

(5 of 23)

Thank you for your request. Here are the latest results.

Serial Number: 74482641

Registration Number: 2075965

Trademark (words only): MICROFOX

Current Status: Registered.

Date of Status: 1997-07-01

Filing Date: 1994-01-25

CURRENT OWNERS

1. Telco Systems, Inc.

GOODS AND SERVICES

fiber-optic telecommunications signal converter and user manuals sold as a unit

PROSECUTION HISTORY

1997-07-01 - REGISTERED-PRINCIPAL REGISTER

1997-05-02 - ALLOWED PRINCIPAL REGISTER - SOU ACCEPTED

1997-04-11 - COMMUNICATION RECEIVED FROM APPLICANT

1997-02-12 - ASSIGNED TO EXAMINER

1996-12-27 - NON-FINAL ACTION MAILED

1996-10-22 - ASSIGNED TO EXAMINER

1996-10-15 - STATEMENT OF USE PROCESSING COMPLETE

1996-10-15 - EXTENSION 1 GRANTED

1996-02-26 - USE AMENDMENT FILED

1996-02-26 - EXTENSION 1 FILED

1995-10-31 - NOTICE OF ALLOWANCE-MAILED

1994-11-25 - EXTENSION OF TIME TO OPPOSE FILED

1994-10-25 - PUBLISHED FOR OPPOSITION

1994-09-23 - NOTICE OF PUBLICATION

1994-06-24 - APPROVED FOR PUB - PRINCIPAL REGISTER

1994-06-23 - ASSIGNED TO EXAMINER

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

Check Status

Word Mark	HYPERLYNX-50
Pseudo Mark	HYPER-LYNX-150
Owner Name	(REGISTRANT) ***Telco Systems, Inc.***
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	Charles E. Weinstein
Serial Number	74-272739
Registration Number	1985921
Filing Date	05/04/1992
Registration Date	07/09/1996
Section 1(B) indicator	SECTION 1 (B)
Mark Drawing Code	(1) TYPED DRAWING
Register	PRINCIPAL
Published for Opposition	09/08/1992
Type of Mark	TRADEMARK
International Class	009
Goods and Services	multiplexers; DATE OF FIRST USE: 1994.09.12; DATE OF FIRST USE IN COMMERCE: 1994.09.12

Thank you for your request. Here are the latest results.

Serial Number: 74272739

Registration Number: 1985921

Trademark (words only): HYPERLYNX-50

Current Status: Registered.

Date of Status: 1996-07-09

Filing Date: 1992-05-04

CURRENT OWNERS

1. Telco Systems, Inc.

GOODS AND SERVICES

multiplexers

PROSECUTION HISTORY

1996-07-09 - REGISTERED-PRINCIPAL REGISTER

1996-05-01 - ALLOWED PRINCIPAL REGISTER - SOU ACCEPTED

1996-04-22 - EXAMINERS AMENDMENT MAILED

1996-02-20 - STATEMENT OF USE PROCESSING COMPLETE

1995-12-01 - USE AMENDMENT FILED

1995-07-27 - EXTENSION 5 GRANTED

1995-06-01 - EXTENSION 5 FILED

1994-10-24 - EXTENSION 4 GRANTED

1994-09-22 - EXTENSION 4 FILED

1994-07-08 - EXTENSION 3 GRANTED

1994-05-26 - EXTENSION 3 FILED

1994-01-06 - EXTENSION 2 GRANTED

1993-11-10 - EXTENSION 2 FILED

1993-07-02 - EXTENSION 1 GRANTED

1993-05-21 - EXTENSION 1 FILED

1992-12-01 - NOTICE OF ALLOWANCE-MAILED

1992-09-08 - PUBLISHED FOR OPPOSITION

1992-08-07 - NOTICE OF PUBLICATION

1992-07-09 - APPROVED FOR PUB - PRINCIPAL REGISTER

1992-07-08 - ASSIGNED TO EXAMINER

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

Check Status

TELCO SYSTEMS

Word Mark	TELCO SYSTEMS
Owner Name	(REGISTRANT) *Telco Systems, Inc.*
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	Charles E. Weinstein
Serial Number	74-497981
Registration Number	1936449
Filing Date	03/07/1994
Registration Date	11/21/1995
Design Search Code	26.11.13; 26.11.21
Mark Drawing Code	(3) DESIGN PLUS WORDS, LETTERS, AND/OR NUMBERS
Disclaimer	NO CLAIM IS MADE TO THE EXCLUSIVE RIGHT TO USE "SYSTEMS" APART FROM THE MARK AS SHOWN
Register	PRINCIPAL
Published for Opposition	08/29/1995
Type of Mark	TRADEMARK
International Class	009
Goods and Services	digital lightwave transmission terminals for fiber-optic telecommunications transmission; bridges providing integration for multiple local area networks;

Services

multiplexers; transceivers; internetworking data compressors; computer software in the field of network management; fiber-optic telecommunications alarm and performance monitoring, remote control and diagnostic systems comprising a mini-computer operating in conjunction with micro-processors built into other equipment, a panel with CRT display, computer memories, keyboards, maintenance status indicators and computer printers; aluminum wall-mounted cabinets designed to hold fiber-optic telecommunications equipment; and user manuals sold as a unit with each of the above; DATE OF FIRST USE: 1984.06.00; DATE OF FIRST USE IN COMMERCE: 1984.06.00

(7 of 23)

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

Check Status

MICROFOX

Word Mark	MICROFOX
Owner Name	(REGISTRANT) *Telco Systems, Inc.*
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	Charles E. Weinstein
Serial Number	74-507026
Registration Number	1924529
Filing Date	03/30/1994
Registration Date	10/03/1995
Design Search Code	03.01.11; 03.01.16; 03.01.24; 26.01.21; 26.11.02; 26.11.08; 27.03.01
Section 1(B) indicator	SECTION 1 (B)
Mark Drawing Code	(3) DESIGN PLUS WORDS, LETTERS, AND/OR NUMBERS
Register	PRINCIPAL
Other Registration Info.	1527891; 1533998; 1616521
Published for Opposition	01/24/1995
Type of Mark	TRADEMARK
International Class	009
Goods and Services	fiber-optic telecommunications signal converter and user manuals sold as a unit; DATE OF FIRST USE: 1994.12.01; DATE OF FIRST USE IN COMMERCE: 1994.12.01

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

(9 of 23)

Check Status

Word Mark	FOX T-BOX
Owner Name	(REGISTRANT) *Telco Systems, Inc.*
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	Charles E. Weinstein
Serial Number	74-392042
Registration Number	1915794
Filing Date	05/19/1993
Registration Date	08/29/1995
Section 1(B) indicator	SECTION 1 (B)
Mark Drawing Code	(1) TYPED DRAWING
Register	PRINCIPAL
Other Registration Info.	1527891; 1533998; 1616521
Published for Opposition	12/21/1993
Type of Mark	TRADEMARK
International Class	009
Goods and Services	aluminum wall-mounted cabinet designed to hold fiber optic telecommunications equipment; DATE OF FIRST USE: 1993.07.12; DATE OF FIRST USE IN COMMERCE: 1993.07.12

(9 of 23)

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

(10 of 23)

Check Status

Word Mark	ACCESS60
Owner Name	(REGISTRANT) *Telco Systems, Inc.*
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	Charles E. Weinstein
Serial Number	74-349923
Registration Number	1852966
Filing Date	01/21/1993
Registration Date	09/06/1994
Section 1(B) indicator	SECTION 1 (B)
Mark Drawing Code	(1) TYPED DRAWING
Register	PRINCIPAL
Published for Opposition	06/29/1993
Type of Mark	TRADEMARK
International Class	009
Goods and Services	multiplexers and user manuals distributed therewith; DATE OF FIRST USE: 1993.09.20; DATE OF FIRST USE IN COMMERCE: 1993.09.20

(10 of 23)

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

Check Status

ACCESS30

Word Mark	ACCESS30
Owner Name	(REGISTRANT) ***Telco Systems, Inc.***
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	Charles E. Weinstein
Serial Number	74-349924
Registration Number	1851901
Filing Date	01/21/1993
Registration Date	08/30/1994
Section 1(B) indicator	SECTION 1 (B)
Mark Drawing Code	(1) TYPED DRAWING
Register	PRINCIPAL
Published for Opposition	07/06/1993
Type of Mark	TRADEMARK
International Class	009
Goods and Services	multiplexers and user manuals distributed therewith; DATE OF FIRST USE: 1993.06.00; DATE OF FIRST USE IN COMMERCE: 1993.06.00

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

Check Status

HYPERSPAN 150

Word Mark	HYPERSPAN 150
Pseudo Mark	HYPER-SPAN 150
Owner Name	(REGISTRANT) *Telco Systems, Inc.*
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	Charles E. Weinstein
Serial Number	74-342785
Registration Number	1796170
Filing Date	12/23/1992
Registration Date	09/28/1993
Section 1(B) indicator	SECTION 1 (B)
Mark Drawing Code	(1) TYPED DRAWING
Register	SUPPLEMENTAL
Affidavits	SECT 8 (6-YR)
Type of Mark	TRADEMARK
Amended Supplemental Registration	07/01/1993
International Class	009
Goods and Services	fiber-optic multiplexers and instruction manuals sold as a unit therewith; DATE OF FIRST USE: 1993.04.08; DATE OF FIRST USE IN COMMERCE: 1993.04.08

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

Check Status

ACCESS48 MUX

Word Mark	ACCESS48 MUX
Pseudo Mark	ACCESS 48 MUX
Owner Name	(REGISTRANT) ***Telco Systems, Inc.***
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	Charles E. Weinstein
Serial Number	74-240664
Registration Number	1794164
Filing Date	01/27/1992
Registration Date	09/21/1993
Section 1(B) indicator	SECTION 1 (B)
Mark Drawing Code	(1) TYPED DRAWING
Disclaimer	NO CLAIM IS MADE TO THE EXCLUSIVE RIGHT TO USE "MUX" APART FROM THE MARK AS SHOWN
Register	PRINCIPAL
Published for Opposition	08/04/1992
Type of Mark	TRADEMARK
International Class	009
Goods and Services	multiplexers; DATE OF FIRST USE: 1992.01.00; DATE OF FIRST USE IN COMMERCE: 1992.01.00

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

Check Status

Word Mark	T3-HUB
Owner Name	(REGISTRANT) *Telco Systems, Inc.*
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	Charles E. Weinstein
Serial Number	74-117928
Registration Number	1749260
Filing Date	11/26/1990
Registration Date	01/26/1993
Section 1(B) indicator	SECTION 1 (B)
Mark Drawing Code	(1) TYPED DRAWING
Register	PRINCIPAL
Other Registration Info.	1598399
Published for Opposition	08/27/1991
Affidavits	SECT 15.; SECT 8 (6-YR)
Type of Mark	TRADEMARK
International Class	009
Goods and Services	digital lightwave transmission terminal for fiber optic telecommunications transmission; DATE OF FIRST USE: 1992.06.05; DATE OF FIRST USE IN COMMERCE: 1992.06.05

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

(17 of 23)

Check Status

Word Mark	ROUTE-24
Owner Name	(REGISTRANT) ***TELCO SYSTEMS, INC.***
Owner Address	63 NAHATAN STREET NORWOOD MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	CHARLES E. WEINSTEIN
Serial Number	73-792373
Registration Number	1591782
Filing Date	04/10/1989
Registration Date	04/17/1990
Mark Drawing Code	(1) TYPED DRAWING
Register	PRINCIPAL
Published for Opposition	01/23/1990
Affidavits	SECT 15.; SECT 8 (6-YR)
Type of Mark	TRADEMARK
International Class	009
Goods and Services	MULTIPLEXERS; COMPUTER PROGRAMS FOR NETWORK MANAGEMENT; DATE OF FIRST USE: 1988.08.31; DATE OF FIRST USE IN COMMERCE: 1988.08.31

(17 of 23)

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

(18 of 23)

Check Status

Word Mark	TELTRAC
Pseudo Mark	TEL TRACK TELTRACK
Owner Name	(REGISTRANT) ***TELCO SYSTEMS, INC.***
Owner Address	1040 MARSH ROAD MENLO PARK CALIFORNIA 94025 CORPORATION CALIFORNIA
Attorney of Record	CHARLES E. WEINSTEIN
Serial Number	73-566855
Registration Number	1583359
Filing Date	11/04/1985
Registration Date	02/20/1990
Mark Drawing Code	(1) TYPED DRAWING
Register	PRINCIPAL
Published for Opposition	03/18/1986
Affidavits	SECT 15.; SECT 8 (6-YR)
Type of Mark	TRADEMARK
International Class	009
Goods and Services	FIBER OPTICS TELECOMMUNICATIONS ALARM AND PERFORMANCE MONITORING, REMOTE CONTROL AND DIAGNOSTIC SYSTEM COMPRISING A MINICOMPUTER OPERATING IN CONJUNCTION WITH MICROPROCESSORS BUILT INTO OTHER EQUIPMENT, A PANEL WITH CRT DISPLAY, MEMORY DEVICES, KEYBOARD, ALARMS, AND PRINTER; DATE OF FIRST USE: 1983.01.00; DATE OF FIRST USE IN COMMERCE: 1983.01.00

(18 of 23)

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

(19 of 23)

Check Status

Word Mark	MUXVIEW
Pseudo Mark	MUX VIEW
Owner Name	(REGISTRANT) *TELCO SYSTEMS, INC.*
Owner Address	63 NAHATAN STREET NORWOOD MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	CHARLES E. WEINSTEIN, ESQ.
Serial Number	73-792180
Registration Number	1568157
Filing Date	04/10/1989
Registration Date	11/28/1989
Mark Drawing Code	(1) TYPED DRAWING
Register	PRINCIPAL
Published for Opposition	09/05/1989
Affidavits	SECT 15.; SECT 8 (6-YR)
Type of Mark	TRADEMARK
International Class	009
Goods and Services	COMPUTER PROGRAMS FOR NETWORK MANAGEMENT; DATE OF FIRST USE: 1989.01.17; DATE OF FIRST USE IN COMMERCE: 1989.01.17

(19 of 23)

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

Check Status

Word Mark	FOX 2
Owner Name	(REGISTRANT) TELCO SYSTEMS FIBER OPTICS CORPORATION
Owner Address	63 NAHATAN STREET NORWOOD MASSACHUSETTS 02062 CORPORATION CALIFORNIA
Owner Name	(LAST LISTED OWNER) ***TELCO SYSTEMS, INC.***
Owner Address	1209 ORANGE STREET WILMINGTON DELAWARE 19801 CORPORATION DELAWARE
Attorney of Record	CHARLES E. WEINSTEIN
Serial Number	73-697756
Registration Number	1533998
Filing Date	11/27/1987
Registration Date	04/11/1989
Design Search Code	03.01.11; 03.01.16; 03.01.24
Mark Drawing Code	(3) DESIGN PLUS WORDS, LETTERS, AND/OR NUMBERS
Register	PRINCIPAL
Published for	

Opposition	01/17/1989
Affidavits	SECT 15.; SECT 8 (6-YR)
Type of Mark	TRADEMARK
International Class	009
Goods and Services	DIGITAL LIGHTWAVE TRANSMISSION TERMINALS FOR FIBER OPTIC TELECOMMUNICATIONS TRANSMISSION; DATE OF FIRST USE: 1987.02.17; DATE OF FIRST USE IN COMMERCE: 1987.02.17

(20 of 23)

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

(21 of 23)

Check Status

Word Mark	FOX-2
Owner Name	(REGISTRANT) TELCO SYSTEMS FIBER OPTICS CORPORATION
Owner Address	63 NAHATAN STREET NORWOOD MASSACHUSETTS 02062 CORPORATION CALIFORNIA
Owner Name	(LAST LISTED OWNER) ***TELCO SYSTEMS, INC.***
Owner Address	1209 ORANGE STREET WILMINGTON DELAWARE 19801 CORPORATION DELAWARE
Attorney of Record	CHARLES E. WEINSTEIN
Serial Number	73-697755
Registration Number	1527891
Filing Date	11/27/1987
Registration Date	03/07/1989
Mark Drawing Code	(1) TYPED DRAWING
Register	PRINCIPAL
Published for Opposition	12/13/1988
Affidavits	SECT 15.; SECT 8 (6-YR)
Type of Mark	TRADEMARK
International Class	009
Goods and Services	DIGITAL LIGHTWAVE TRANSMISSION TERMINALS FOR FIBER OPTIC TELECOMMUNICATIONS TRANSMISSION; DATE OF FIRST USE: 1987.02.17; DATE OF FIRST USE IN COMMERCE: 1987.02.17

(21 of 23)

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

Check Status

WDSL

Word Mark	WDSL
Pseudo Mark	WDSL
Owner Name	(APPLICANT) ***Telco Systems*** ,Inc.
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION MASSACHUSETTS
Serial Number	75-775025
Filing Date	09/03/1999
Description of Mark	The mark consists of Wireless Digital Subscriber Loop
Section 1(B) indicator	SECTION 1 (B)
Mark Drawing Code	(1) TYPED DRAWING
Register	PRINCIPAL
Type of Mark	TRADEMARK
International Class	009
Goods and Services	Telecommuncations and networking equipment, including computer hardware and software, user manuals sold as unit therewith Services-- Telecommunications and networking technology using wireless (radio) to provide digital subscriber loop services

Thank you for your request. Here are the latest results.

Serial Number: 75775025

Registration Number: (NOT AVAILABLE)

Trademark (words only): WDSL

Current Status: Newly filed application, not yet assigned to an examining attorney.

Date of Status: 1999-09-03

Filing Date: 1999-09-03

CURRENT OWNERS

1. Telco Systems,Inc.

GOODS AND SERVICES

Telecommuncations and networking equipment, including computer hardware and software, user manuals sold as unit therewith Services-- Telecommunications and networking technology using wireless (radio) to provide digital subscriber loop services

PROSECUTION HISTORY

(NOT AVAILABLE)

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

VOLTEDGE

Word Mark	VOLTEDGE
Pseudo Mark	VOLT EDGE
Owner Name	(APPLICANT) *Telco Systems, Inc.*
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	Charles E Weinstein
Serial Number	75-679515
Filing Date	04/12/1999
Section 1(B) indicator	SECTION 1 (B)
Mark Drawing Code	(5) WORDS, LETTERS AND/OR NUMBERS IN STYLIZED FORM
Register	PRINCIPAL
Type of Mark	TRADEMARK
International Class	009
Goods and Services	battery chargers for use with telecommunications and networking equipment

US PATENT & TRADEMARK OFFICE
TRADEMARK TEXT AND IMAGE DATABASE

(23 of 23)

Check Status

Word Mark	RESPONSEEDGE
Pseudo Mark	RESPONSE EDGE
Owner Name	(APPLICANT) ***Telco Systems, Inc.***
Owner Address	63 Nahatan Street Norwood MASSACHUSETTS 02062 CORPORATION DELAWARE
Attorney of Record	CHARLES E WEINSTEIN
Serial Number	75-395104
Filing Date	11/24/1997
Section 1(B) indicator	SECTION 1 (B)
Mark Drawing Code	(1) TYPED DRAWING
Register	PRINCIPAL
Type of Mark	SERVICE MARK
International Class	037
Goods and Services	Installation and maintenance of telecommunications and telecommunications networking equipment

(23 of 23)

SCHEDULE B
(See Attached)

Section 2.15

US PATENT & TRADEMARK OFFICE
PATENT FULL TEXT AND IMAGE DATABASE

Searching 1976-2000...

Results of Search in 1976-2000 db for:
(AN/"Telco Systems" AND AC/"Norwood"): 7 patents.
Hits 1 through 7 out of 7

[redacted] [ ]

[redacted] an/"Telco Systems" and ac/"Norwood"

	PAT. NO.	Title
1	5,715,260	Method and apparatus for providing a variable reset interval in a transmission system for encoded data
2	5,684,962	Context control block for computer communications
3	5,570,345	Protection switching system with single line control
4	5,526,363	Multicontext compression system with shared data structures
5	5,526,362	Control of receiver station timing for time-stamped data
6	5,325,270	Modular backplane
7	5,237,640	Guide for an optical fiber cable having minimum bend radius

United States Patent **5,715,260**
Black , et al. **February 3, 1998**

Method and apparatus for providing a variable reset interval in a transmission system for encoded data

Abstract

A method and apparatus for reducing the amount of corrupted data in a system for transmitting encoded data across a network, which system requires sychronization between encoding and decoding nodes, the method and apparatus involving (a) providing an indication of the reliability of the channel between the encoding and decoding nodes; (b) performing automatic resets at the nodes at intervals I; and (c) utilizing the indication of channel reliability to control the interval I. The interval I may be determined, for example, by the error rate on the channel for one or more preceding time interval S, and may be determined at either the encoding or decoding node.

Inventors: **Black; Jeffrey T.** (Wellesley, MA); **Weiss; Jeffrey A.** (Smithfield, RI)
Assignee: **Telco Systems, Inc.** (Norwood, MA)
Appl. No.: **489328**
Filed: **June 12, 1995**

U.S. Class: **371/47.1**; 371/5.1; 371/5.4
Intern'l Class: G06F 011/00; H04L 012/00
Field of Search: 371/5.1,5.4,47.2,47.1,37.1,41,32,33,35,37.7,57.1,61,62 341/60,94 380/48 375/364,368,357,358,359

References Cited [Referenced By]

U.S. Patent Documents

3571794	Mar., 1971	Tong	340/146.
3641494	Feb., 1972	Perrault et al.	340/146.
4654480	Mar., 1987	Weiss	380/48.
4701923	Oct., 1987	Fukasawa et al.	371/41.
4841526	Jun., 1989	Wilson et al.	371/32.
4939731	Jul., 1990	Reed et al.	371/32.
5130993	Jul., 1992	Gutman et al.	371/42.

Primary Examiner: Chung; Phung
Attorney, Agent or Firm: Wolf Greenfield & Sack, P.C.

Claims

1. In a system for transmitting encoded data across a network, the encoding being such that synchronization must be maintained between contexts at encoding and decoding nodes to avoid corruption of the data, a method for reducing the amount of corrupted data in the system while maximizing coding efficiency, comprising the steps of:

(a) including error detection information with transmitted encoded data;

(b) receiving at an encoding node an indication of errors detected at the corresponding decoding node;

(c) counting the number of received error indications R at the encoding node during a selected interval S;

(d) automatically resetting the context at at least the encoding node at intervals I of variable duration; and

(e) utilizing the number R for the interval S.sub.n to control the durations of the intervals I for the subsequent interval S.sub.n+1.

2. A method as claimed in claim 1 wherein each indication of error received at the encoding node is a reset request, and including the step of also resetting context at at least the encoding node in response to a reset request.

3. A method as claimed in claim 2 including the step of resetting an interval counter (D) in response to the receipt of a reset request at the encoding node.

4. A method as claimed in claim 1 wherein step (e) includes the step of increasing each interval I by a selected amount if R equals zero for the interval S.sub.n.

5. A method as claimed in claim 4 wherein each interval I cannot be increased beyond a selected maximum M.

6. A method as claimed in claim 4 wherein each interval I can be increased to infinity.

7. A method as claimed in claim 1 wherein step (e) includes the step of decreasing each interval I by a selected amount if R is greater than zero for the interval S.sub.n.

8. A method as claimed in claim 7 wherein each interval I cannot be decreased below a selected minimum L.

9. A method as claimed in claim 8 wherein L is equal to one.

10. A method as claimed in claim 8 wherein, if R is greater than a threshold value T for an interval S.sub.n, each interval I is set to L.

11. A method as claimed in claim 10 wherein L is equal to one.

12. A method as claimed in claim 1 wherein the encoded data is compressed data and the synchronization is to be maintained between compression dictionaries.

13. A method as claimed in claim 1 wherein each interval I is a number of frames of data between automatic resets.

14. A method as claimed in claim 1 including the step of resetting the context at the decoding node in data synchronization with the context at the encoding node.

15. In a system for transmitting encoded data across a network, the encoding being such that synchronization must be maintained between contexts at encoding and decoding nodes to avoid corruption of the data, a method for reducing the amount of corrupted data in the system while maximizing coding efficiency, comprising the steps of:

(a) providing an indication of the reliability of the channel between the encoding and decoding nodes;

(b) automatically resetting the context at the encoding node at intervals I of variable duration; and

(c) utilizing the indication of reliability to control the duration of the intervals I.

16. A method as claimed in claim 15 including the step of resetting the context at the decoding node in data synchronization with the context at the encoding node.

17. A method as claimed in claim 15 wherein the indication of reliability during step (a) is provided at the encoding node; and wherein step (c) is performed at the encoding node.

18. A method as claimed in claim 15 wherein the indication of reliability during step (a) is provided at the decoding node; and wherein step (c) is performed at the decoding node.

19. A method as claimed in claim 15 wherein the indication of reliability is an indication of errors on the channel during a selected interval S, and wherein during step (c) the duration of the interval I is controlled based on the indication of errors for the preceding interval S.

20. A method as claimed in claim 15 wherein the indication of reliability is an indication of errors on the channel during a selected interval S, and wherein during step (c) the value of I is controlled based on the indication of errors for a selected plurality of preceding interval S.

21. In a system for transmitting encoded data across a network, the encoding being such that synchronization must be maintained between contexts at encoding and decoding nodes to avoid corruption of the data, apparatus for reducing the amount of corrupted data in the system while maximizing coding efficiency, comprising:

(a) means for providing an indication of the reliability of the channel between the encoding and decoding nodes;

(b) means for automatically resetting the context at the encoding node at intervals I of variable duration; and

(c) means for utilizing the indication of reliability to control the duration of each interval I.

22. Apparatus as claimed in claim 21 including means for resetting the context at the decoding node in data synchronization with the context at the encoding node.

Description

FIELD OF THE INVENTION

This invention relates to transmission systems for encoded data and more particularly to such a system which reduces the amount of corrupted data in the system while controlling processing overhead and maintaining encoding efficiency by providing variable reset intervals for encoder synchronization, which intervals are based on detected error rate.

BACKGROUND OF THE INVENTION

For reasons including improved bandwidth and/or security, it is common for data being transmitted over various transmission media to be encoded in some way, such encoding normally involving compression, encryption, or both. Many of the more sophisticated compression algorithms, such as Lempel-Ziv 77 (LZ77) and Dynamic Huffman encoding, and many sophisticated encryption algorithms, involve the use of matching data buffers, dictionaries, tables and the like (sometime hereinafter collectively referred to as context) at both the transmitting/encoding node and the receiving/decoding node, which context must be maintained in synchronization in order for the encoded data to be correctly decoded. Any loss of synchronization of the context between the encoding and decoding nodes generally results in the corruption of all data received after the loss of synchronization occurs.

In order to preserve the integrity of received encoded data, various protocols have therefore been developed to maintain the context at the encoding and decoding nodes in synchronization. These protocols have generally involved including an error detection code, such as parity bits or cyclic redundancy code (CRC) with the coded data, with an error detected through one of these techniques being utilized as an indication that a loss of synchronization may have occurred. The error detection coding may be included in the data prior to encoding, with the data then being decoded prior to performing an error detection check at the receiving/decoding node, or the error detection code may be added to the encoded data at the transmitting node, with error detection being performed at the receiving node prior to decoding. In these systems, when an error is detected at a receiving node, a reset request is sent through a back channel to the encoding node. The encoding node, when it receives this request, recognizes that a loss of synchronization has occurred and initiates a resynchronization sequence. This may, for example, involve clearing a history buffer and/or various tables, dictionaries and the like and restarting these context items at, depending on the coding, at least the transmitting node, and frequently both nodes, to restore data synchronization. In environments where loss of data is unacceptable, this may also result in the retransmission of the data in which the error was detected and in all subsequently transmitted data which may have been corrupted by the lack of synchronization. In other environments, an effort may be made to reconstruct all or a part of the corrupted data in some other way, or the corrupted data may merely be discarded.

However, the protocol described above has several limitations. The first limitation is that if the channel is in fact not totally reliable, the reset request on the back channel may for some reason not reach the encoding station, resulting in the transmission of corrupted data for an extended period of time until the situation can be corrected. However, even if the reset request is properly received, the time period between the original message being transmitted by the encoding station and the encoding station receiving the reset request may be substantial, resulting in large amounts of corrupted data being transmitted which must then be either retransmitted or lost. Neither retransmission nor loss of large amounts of data is desirable. The reason for the time delay in receiving reset requests is that the nodes on the network may be widely separated, with there frequently being many intermediate nodes. For example, in a telephony environment, the sending and receiving nodes may be in different states, different countries or even different continents. The message may also pass through various end offices and central offices of the telephone system in its path from one node to the other. Furthermore, transmissions may be made via satellites, requiring propagation delays of hundreds of milliseconds. Even though electronic transmissions are rapid, it can take on the order of milliseconds or more for the encoded message to pass through intermediate nodes to the receiving/decoding node, for the decoding node to recognize the error and produce the reset request and for the reset request to be sent back through the network, including the intermediate nodes, to the original transmitting/encoding node. At the speeds of modern communication systems, dozens or even hundreds of frames of data could be transmitted during such an interval.

In order to correct the first of the problems indicated above, U.S. Pat. No. 5,130,993, issued to Gutman et al on Jul. 14, 1992, teaches the receiving/decoding node starting a timer when it sends a reset request, and sending a second reset request if a reset indication has not been received when the timer times out. The timer would be set for some reasonable number of frames, depending on the

normal time required for a reset request to be responded to. This patent also teaches that the first problem may be dealt with by, in addition to performing resets on the context at the two nodes when a reset request is received as the result of a detected error, also performing periodic resets every N frames. For the embodiment disclosed in the patent, resets are performed every nine frames. This means that regardless of how long it takes for a reset request to be generated and to reach the original transmitting/encoding node, and even if such reset request is not received, no more than nine corrupted frames will be transmitted before a reset occurs, and in most instances less than this number of frames will be transmitted, thereby minimizing the amount of corrupted data which will need to be either retransmitted or lost.

However, this solution is not ideal for two reasons. First, resets impose an overhead burden on the system which reduces the rate at which data can be transmitted. The more often resets are performed, the more the average data rate on the system is reduced. Second, particularly for compression, the degree of compression which can be achieved is a function of the size of a history buffer which is used and of the various dictionaries/tables of the context. Thus, when the context elements are reset, and then regenerated, there is a loss of compression ratio during the transition periods. Thus, the more often the context are reset, the lower the overall compression ratio which is achievable by the system. Frequent reset can also reduce encoding efficiency for other types of encoding.

Thus, there is a critical tradeoff in selecting the interval between automatic resets in such a system, it being desirable that such intervals be short enough so as to minimize the amount of data which either must be retransmitted or lost, while being long enough so as not to adversely affect the data rate and encoding efficiency/compression ratio for the system. In particular, for a real or virtual channel which is experiencing low error rate, it would be desirable for the interval between automatic resets to be relatively long so as to minimize the adverse effects on data rate and encoding efficiency caused by the resets, while for unreliable channels experiencing frequent errors, shorter intervals between automatic resets may be more desirable. A need therefore exists for an improved system which permits substantial optimization of automatic reset intervals to be achieved in response to the current condition of the channel over which the data is being transmitted without requiring outside human intervention.

SUMMARY OF THE INVENTION

In accordance with the above, this invention provides a method and apparatus for reducing the amount of corrupted data in a system for transmitting encoded data across a network while controlling the processing overhead and encoding efficiency (i.e. compression ratio) by adjusting the number of resets which are automatically performed during a given interval based on the detected reliability or error condition of the relevant channel. In particular, error detection information is included with the transmitted encoded data. As previously indicated, this error detection information may be added to the data either before or after encoding. Further, the encoding may be for compression, encryption, or other purposes, but requires that synchronization be maintained between encoding and decoding nodes to avoid corruption of the data. The encoding node may also receive an indication of errors detected at the receiving node. The number of error indications R is counted at the encoding node or decoding node during at least one selected interval S. The encoding node is automatically reset at intervals I with the number R of received error indications for interval S.sub.n being utilized to control the duration of the interval I for the subsequent interval S.sub.n+1. If required, the decoding node may then also be reset in data synchronization with the encoding node (for example when the first reset frame is received). For preferred embodiments, the error indication received at the encoding node is a reset request with appropriate resets also being performed at the nodes in response to such a reset request.

For a preferred embodiment, the interval I is increased by a selected amount if R=0 for the interval S.sub.n. A selected maximum M may be provided beyond which the interval I cannot be increased or I may be permitted to increase to infinity. For the preferred embodiment, the interval I is decreased by a selected amount if R is greater than 0 for the interval S.sub.n. A minimum L may be provided below which the interval I cannot be decreased, with L being one for a preferred embodiment. Further, if R is greater than a threshold value T for an interval S.sub.n, the interval I may be set to the

minimum value L. For a preferred embodiment, the interval I is expressed as a number of frames, with a frame being an encapsulated packet of data.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention as illustrated in the accompanying drawings.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an exemplary system in which the teachings of this invention might be utilized.

FIG. 2 is a flow diagram of the process for maintaining synchronization between the encoder/decoder context at an encoding and decoding node in accordance with the teachings of this invention.

DETAILED DESCRIPTION

Referring to FIG. 1, the exemplary system 10 is shown as having a plurality of nodes 12A-12N which are interconnected through virtual network elements 14. Virtual network elements 14 may include copper and/or fiber optic wires, cables, radio links and other data transmission media, as well as relay stations, end offices, central offices, and other intermediary facilities of the network being used. The network may, for example, be a standard telephony network where the nodes on the network may be in the same building or may be separated by hundreds or even thousands of miles. Thus, the nodes may be in different states, different countries or even different continents. Network elements 14 are referred to as virtual network elements since the actual network from node 1 to node 2 is established in response to a message from node 1 addressed to node 2 and the network ceases to exist when transmission of messages between these two nodes is complete. The various elements of the network may also be of different quality and various links in the network may be subject to spurious noise, traffic overloads and other error sources which can result in significant differences in the error rate between the two nodes over time. Differences in the error rate between two nodes over time may also result from the fact that the virtual network will not necessarily utilize a fixed physical path between two nodes, particularly when the nodes are relatively far apart and there may be an almost infinite number of different ways in which a path may be established between the two nodes. Thus, the virtual path established for a given message or data may depend on line availability based on other traffic in the system and other factors, with the particular path chosen for a given message influencing the error rate for the message. Thus, a system which performs automatic resets at fixed time intervals for the entire system, regardless of path length, path quality and other factors which may contribute to error rate, will inevitably be imposing undue overhead and encoding efficiency burdens on the system, thereby reducing both throughput and available encoding efficiency/compression ratio for some groups of messages, while not resetting often enough to avoid the requirement for significant retransmission of data and/or significant data loss for other traffic through the network. As discussed earlier, this invention overcomes these problems by providing an adaptive interval for the automatic resets.

In practicing the invention, each node 12 includes a control processor 16A-16N, with only the control processor 16A for node 1 being shown in the figure. Each processor includes as part thereof an R counter 18, an S counter 20, an I counter 22, and a T register 24. An interval (D) counter 25 is also provided which tracks the number of frames since the last reset (or automatic reset), and, where appropriate, L and M registers may also be provided (not shown). Each node also includes an encoder/decoder element 26A-26N and an error detection circuit or element 28A-28N (with only the elements 26A and 28A being shown in the figure). Encoder/decoder 26 and error detector 28 may be separate hardware or software devices or the encoder/decoder function and error detection function may be performed in software in the control processor 16. The encoding/decoding function may be for purposes of compressing data, encrypting data or some combination thereof or may be for other encoding purposes known in the art. However, when practicing the teachings of this invention, the encoding and decoding process will be such that synchronization of buffers, dictionaries, tables and/or other context elements are required in order for the encoder data to be properly decoded, so

that any loss of synchronization between the context of the two nodes will result in corrupted, useless data. Where the encoding/decoding is for compression purposes, examples of techniques in which the teachings of this invention could be employed include various Lempel-Ziv 77 compression techniques and various Dynamic Huffman encoding techniques.

In operation, referring to FIG. 2, it is seen that when node 1 has a message to transmit, which message may either be generated by control processor 16A or other equipment at node 1, or may be received at node 1 from another source for transmission, node 1 encodes the data in encoder 26A and causes the error detect information to be added to the message by error detect circuit 28A. The error detect information may be added either before encoding and be encoded with the transmitted message, or may be added to the message after encoding. For the preferred embodiment, messages are sent as encapsulated packets or frames, with each such packet or frame including, in addition to the data being transmitted, the address to which the message is being directed and the error detection information. The length of each frame can vary with the transmission medium and transmission protocol being utilized, being for example as little as 64 bytes in Ethernet applications to over 8,000 bytes in other applications. Frame sizes outside this range are also possible for networks or applications which are not commonly used at this time. Each of these frames of data, which frames are formed in standard ways which do not form part of the present invention, are transmitted during step 40.

During step 42, the encoded message is received at node 2, which may for example be the node 12B in FIG. 1, where the message is decoded by the encoder/decoder circuit 26 at that node, and error detection is performed by the appropriate error detect circuitry 28. If no error is detected during step 44, node 2 continues to receive data. If an error is detected during step 44, the operation proceeds to step 46 to generate a reset request to node 1. While FIG. 2 also indicates that node 2 continues to receive data after an error is detected, it should be realized that this data is corrupted, since it cannot be reliably decoded. Therefore, this data may not in fact be received or, if received, may be discarded. Alternatively, some effort may be made to retrieve what can be retrieved from this data so as to avoid the need for retransmission.

The reset request generated during step 46 is received at node 1 during step 48. The receipt of the reset request at node 1 causes two things to happen. First, during step 50, the context for the encoder at node 1 are reset and, if required, or otherwise desired, an appropriate message is sent to node 2 to reset its context in synchronism with that for node 1. This reset message is received at node 2, causing the decoder context at this node to be reset to restore synchronism between the encoder/decoders at the two nodes during step 52. For some coding, such as LZ77, a resetting at the decoding node is not required since inputs are always clear data or offsets which go only to received data in the reset region. Therefore, for these codes, step 52 may be omitted if desired.

The receipt of a reset request also causes the reset counter 18 for processor 16A at node 1 to be incremented during step 54. Normally the reset counter is incremented by 1 for each reset request received. From step 54, the operation proceeds to step 56 to reset the D or interval counter 25. While step 56 is optional at this point, it is considered preferable since it keeps the number of resets being performed by the system from being significantly increased above the determined reset interval even if some error indications are received. However, since once an error occurs, the likelihood of successive errors occurring as a result of noise, congestion or other spurious error sources is significantly increased, it may be desirable in at least some applications not to reset the interval counter 25 at this point in the operation since a shortened time interval to the next reset after an error is detected may reduce the likelihood of having to either resend significant data or have significant data lost. The tradeoff on whether to include step 56 at this point will be based on a system designer's decision as to whether the likelihood of an additional error occurring after an initial error detection is sufficiently large so as to make a reduced automatic reset interval at this point desirable even though this will result in some slight decrease in throughput and compression/encoding rate.

While the various operations described above are being performed, S counter 20 continues to run. S counter 20 may be a clock, or may be a frame counter, byte counter or the like. The interval of S counter 20 may be in the order of seconds and therefore orders of magnitude longer than the duration

of a typical frame. During step 58, a determination is continuously or periodically made as to whether the S counter has timed out. If the S counter has not timed out, the counter continues to run and continues to be monitored during step 58.

When S counter 20 does time out, a "yes" output is obtained from step 58 which causes a number of operations to be performed. In particular, during step 60, S counter 20 is reset to start another S count interval. Depending on the nature of counter 28, this step may not be required. At this time, determinations are also made as to whether R (i.e. the count in the R counter 18, which count is indicative of the number of reset requests during the just completed S interval) is equal to zero during step 62, whether R is between zero and a threshold value T during step 64 and whether R is equal to or greater than T during step 66. If R is equal to zero at the end of the time interval S, it means that no errors were detected during the preceding time interval S so that the virtual network between the two nodes is substantially error free. When this occurs, the operation proceeds to step 67, which step is optional, to determine if I is equal to some maximum value M. Without step 67, there is no maximum and I may theoretically go to infinity. From step 67 if a "no" output is obtained, or from step 66 if step 67 is not performed, the operation proceeds to step 68 to increment the value for I (i.e. the interval between automatic resets) in counter 22 by a selected amount. For a preferred embodiment, I is an indication of the number of frames between automatic resets and the value of I is incremented by one during step 68.

If the value of R is between zero and T, there is a "yes" output from step 64 indicating that at least one error was detected during the preceding time interval S, but that the number of errors detected is less than the threshold value T. For the preferred embodiment, the threshold value T for a time interval S of 5 sec is ten. A "yes" output during step 64 results in step 69 being performed to determine if I is already at its minimum value, which value is one for a preferred embodiment. If a "no" output is obtained during step 69, the value of I is decremented by a selected amount during step 70, this amount being by one frame for the preferred embodiment. Finally, if there is a "yes" output during step 66, this means that there were substantial errors on the line during the preceding time interval S (i.e. ten or more for a preferred embodiment) so that the virtual network is not very reliable. Under these circumstances, the operation proceeds to step 72 to set I to a predetermined minimum value L which, for the preferred embodiment, is one frame. Thus, for a very noisy virtual link between two nodes, resets occur between each frame until a determination is made that the line has become more reliable. From steps 68, 70 or 72, the operation proceeds to step 74 to reset the R counter 18 in preparation for the beginning of the next S interval.

As the steps indicated above are being performed, processor 16A is also monitoring to determine if a frame has been transmitted (step 75). When, at the end of a frame, a "yes" output is obtained during step 75, step 76 is performed to determine if the interval counter 25 is equal to the current value stored for the interval I in counter 22. If a "no" output is obtained during step 76, then step 77 is performed to increment the interval counter 25 and, for the preferred embodiment, another frame of data is transmitted and step 76 is again performed to see if the interval I has passed. When, during step 76, a "yes" output is obtained, two operations occur. First, step 56 is performed to reset interval counter 25. Second, step 50 is performed to reset the encoder context and to send a reset message to node 2 to cause the decoder context at this node to be reset during step 52 in data synchronism with the transmitting node. Further, from a "yes" output during step 76, the operation returns to step 75 to test for the transmission of a frame, and to steps 76 and 77 to increment the interval counter and to test the D value against I until a determination is again made that the interval counter is equal to I and another automatic reset is performed.

A system is thus provided which optimizes the performance of automatic resets in a transmission system for encoded data based on the experienced error rate in the virtual channel interconnecting the nodes. More generally, the interval for performing automatic resets is controlled as a function of the reliability of the channel interconnecting the encoding and decoding nodes. Thus, while variations in the value I are made based solely on the number of detected errors during a preceding interval S for the preferred embodiment, these variations could be controlled in response to a finite input response filter or an infinite input response filter so as to be responsive to what occurs during a larger number of prior intervals. Further, while the interval determination is made at the transmitting/encoding node

for the preferred embodiment in response to error indications received from the decoding node, the automatic reset intervals could also be determined at the decoding node, with all resets from the encoding node being in response to reset requests received from the decoding node, these reset requests being either in response to detected errors, as is currently the case, or automatic reset requests. One potential advantage of determining automatic reset interval at the decoding node is that lost resets do not affect the determined interval. However, it may be desirable to store a determined reset interval at the encoding node to avoid potential loss of automatic reset signals. Particularly if the determination of automatic reset interval I is performed at the receiving node, any of a variety of error indication protocols currently employed, or which may be developed in the future, for providing an indication of channel reliability, including, but in no way limited to, redundancy or CRC codes included with data packets, sequence codes which detect a missing packet, etc. Further, in areas where high reliability is required, the threshold for setting I to one may be very low, for example a single error during a given interval S, while in other, less secure applications, the threshold feature may be eliminated completely. The amount by which incrementing and decrementing is done, and whether such incrementing or decrementing occurs at the end of each interval S, are based on two or more consecutive intervals which are, for example, error free, etc. are also design choices which may vary with application and environment. Thus while a particular implementation has been shown for incrementing, decrementing and resetting the automatic reset intervals, this implementation is by way of example only for a particular environment and is not to be considered a limitation on the invention. The specific way in which the reset interval will be incremented, decremented, set or reset will depend on the environment in which the system is being utilized and on desired performance criteria and will therefore vary with the application and environment for the system. However, in accordance with the teachings of the invention, the intervals for the resets will be varied at selected intervals based on a detected or otherwise determined error rate/channel reliability for the channel over which the data is being transmitted.

Thus, while the invention has been particularly shown and described above with reference to preferred embodiments, the foregoing and other changes in form and detail may be made therein by one skilled in the art without departing from the spirit and scope of the invention.

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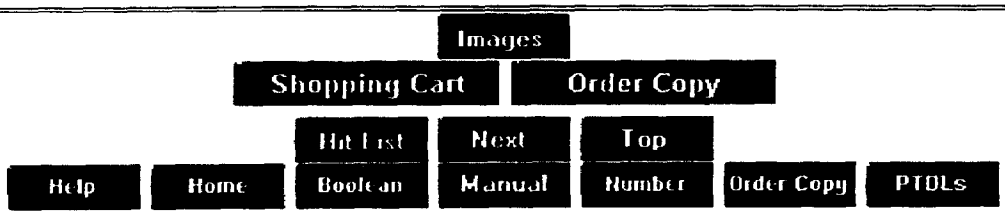

United States Patent **5,684,962**
Black , et al. **November 4, 1997**

Context control block for computer communications

Abstract

A single queue or descriptor ring references several context control blocks, each of which corresponds to a different data path in a communications system. An entry in the descriptor ring references an appropriate context control block and a source packet representing a packet locations prior to processing. The descriptor ring may include a destination packet representing the packet locations after processing. The descriptor ring is particularly suitable for communications between a main processor and a coprocessor.

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Claims

1. A method for communicating between a first processor and a second processor with respect to data associated with a plurality of data paths, comprising the steps of:

creating a plurality of context control blocks, each of the plurality of context control blocks corresponding to one of the plurality of data paths;

receiving an input data packet associated with a first data path of the plurality of data paths, and placing the input packet into a first input packet location;

creating a descriptor entry corresponding to the input data packet, the descriptor entry including a context control block pointer that references the context control block corresponding to the first data path, and an input packet pointer that references the first input packet location; and

processing the input data packet, using the context control block corresponding to the first data path, to create an output data packet and placing the output data packet in an output data packet location.

2. The method of claim 1, wherein the step of creating a descriptor entry includes creating a status block, the method further including the steps of:

writing, by the first processor, a command to the status block of the descriptor entry to command the second processor to process the input data packet;

reading, by the second processor, the command from the status block of the descriptor; and

updating, by the second processor, the status of the descriptor entry to notify the first processor that the input data packet has been processed.

3. The method of claim 1, wherein one of the plurality of context control blocks references compression data, and wherein the step of processing includes compressing the input data packet according to the compression data.

4. The method of claim 3, wherein one of the plurality of context control blocks further references encryption data, and wherein the step of processing further includes encrypting the input data packet according to the encryption data.

5. The method of claim 1, wherein one of the plurality of context control blocks references encryption data, and wherein the step of processing includes encrypting the input data packet according to the encryption data.

6. The method of claim 1, further including the step of creating a descriptor ring, and wherein the step of creating a descriptor entry includes creating the descriptor entry in the descriptor ring.

7. The method of claim 6, wherein the descriptor ring is associated with data of a first physical data path, the method further including the step of creating a second descriptor ring that is associated with data of a second physical data path that is different from the first physical data path.

8. The method of claim 6, wherein the descriptor ring is associated with data of a first virtual data path, the method further including the step of creating a second descriptor ring that is associated with data of a second virtual data path that is different from the first virtual data path.

9. The method of claim 1, wherein the step of creating a descriptor entry includes defining an output packet pointer that references the output data packet location, and wherein the step of processing

includes placing the output data packet in the output data packet location defined in the step of creating.

10. The method of claim 1, wherein the step of processing further includes creating a destination descriptor entry including an output packet pointer that references the output data packet location.

11. The method of claim 1, wherein the step of processing the input data packet includes generating new data for the context control block, and wherein the method further includes a step of updating the context control block to include the new data.

12. An apparatus for communicating between a first processor and a second processor with respect to data associated with a plurality of data paths, comprising:

a shared memory coupled to the first processor and the second processor, the shared memory having an input packet location for an input data packet and an output packet location for an output data packet; and

a descriptor ring having a plurality of descriptor entry locations, the descriptor ring including at least one descriptor entry located in one of the plurality of descriptor entry locations, each descriptor entry including:

a context control block pointer that references the context control block corresponding to one of the plurality of data paths; and

an input packet pointer that references the input packet location;

wherein the output data packet represents the input data packet that has been processed by the second processor in accordance with information identified by the context control block.

13. The apparatus of claim 12, wherein the descriptor entry further includes a status block that stores a command from the first processor to the second processor.

14. The apparatus of claim 12, wherein the context control block references compression control variables.

15. The apparatus of claim 14, wherein the context control block further references encryption control variables.

16. The apparatus of claim 12, wherein the context control block references encryption control variables.

17. The apparatus of claim 12, wherein the descriptor ring is associated with data of a first physical data path, the apparatus further including a second descriptor ring that is associated with data of a second physical data path that is different from the first physical data path.

18. The apparatus of claim 12, wherein the descriptor ring is associated with data of a first virtual data path, the apparatus further including a second descriptor ring that is associated with data of a second virtual data path that is different from the first virtual data path.

19. The apparatus of claim 12, wherein the descriptor ring is stored in the shared memory.

20. The apparatus of claim 12, wherein each descriptor entry further includes an output packet pointer that references the output packet location.

21. The apparatus of claim 12, further including a destination descriptor entry that includes an output packet pointer that references the output packet location, the destination descriptor entry being entered by the second processor.

22. The apparatus of claim 12, wherein the second processor generates new status and updated control variables for the context control block by processing the input data packet, the context control block further including the new status and a reference to the updated control variables generated by the second processor.

23. An apparatus for communicating between a first processor and a second processor with respect to data associated with a plurality of data paths, the apparatus comprising:

a plurality of context control blocks, each of the plurality of context control blocks corresponding to one of the plurality of data paths;

an input data packet associated with a first data path of the plurality of data paths, the input data packet being stored in a first input packet location; and

a descriptor entry corresponding to the input data packet, the descriptor entry including a context control block pointer that references the context control block corresponding to the first data path, and an input packet pointer that references the first input packet location;

wherein the second processor uses the context control block corresponding to the first data path to create an output data packet and places the output data packet in an output packet location.

24. The apparatus of claim 23, wherein the descriptor entry includes a status block that stores a command from the first processor to the second processor.

25. The apparatus of claim 23, wherein the context control block references compression control variables.

26. The apparatus of claim 25, wherein the context control block further references encryption control variables.

27. The apparatus of claim 23, wherein the context control block references encryption control variables.

28. The apparatus of claim 23, further including a descriptor ring that contains the descriptor entry.

29. The apparatus of claim 28, wherein the descriptor ring is associated with data of a first physical data path, the apparatus further including a second descriptor ring that is associated with data being of a second physical data path that is different from the first physical data path.

30. The apparatus of claim 28, wherein the descriptor ring is associated with data of a first virtual data path, the apparatus further including a second descriptor ring that is associated with data being of a second virtual data path that is different from the first virtual data path.

31. The apparatus of claim 23, wherein the descriptor entry further includes an output packet pointer that references the output packet location.

32. The apparatus of claim 23, further including a destination descriptor entry including an output packet pointer that references the output packet location.

33. The apparatus of claim 23, wherein the second processor generates new status and updated control variables for the context control block by processing the input data packet, the context control block further including the new status and a reference to the updated control variables generated by the second processor.

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to computer systems, and more particularly to communication between two processors.

2. Discussion of the Related Art

Communication of data from one processor to another processor may be performed using a variety of techniques. Several techniques use shared memory, in which both processors have read and write access to the same memory. Thus, if one of the processors writes data to the shared memory, the other processor may read the data from such memory.

In order to implement a shared memory technique, both processors must have information defining the content of the shared memory. For example, one location of the shared memory may represent a command location, which contains a command or several commands from one processor to the other. Additionally, a location may reference other locations in the shared memory, so that the processor reading this location will know where to read for the appropriate data.

Queues may also be established within the shared memory in order to support data such as communications data. For example, communications controllers which support multiple paths provide a separate queue or set of queues for each path. The Motorola MC68606 LAPD controller is one example of such a communications controller. However, when separate queues are provided, a processor must poll the status of each queue in order to determine whether the queue contains data for the processor. A disadvantage to this technique is that the polling requires substantial resources, such as processing time and memory bus bandwidth. It is therefore desirable to provide a communications technique that reduces the resources required.

SUMMARY OF THE INVENTION

In order to reduce the resources for communicating between two processors, one embodiment of the invention provides a single queue or descriptor ring which references several context control blocks, each of which corresponds to a different logical or physical data path in a communications system. An entry in the descriptor ring references an appropriate context control block and a source packet representing a packet location prior to processing. The entry may also reference a destination packet representing the packet locations after processing. In one embodiment, a destination entry references the destination packet. The context control block may include new data generated by one of the two processors.

One embodiment of the invention is directed to a method for communicating between a first processor and a second processor with respect to a plurality of data paths. A plurality of context control blocks is created, each corresponding to one of the plurality of data paths. An input data packet, associated with one of the plurality of data paths is received and placed into a first input packet location. A descriptor entry is created, preferably in a descriptor ring, that corresponds to the input data packet. The descriptor entry includes a context control block pointer and an input packet pointer. The input data packet is then processed, using the appropriate context control block, and the resulting output data packet is placed in an output data packet location. The descriptor entry may also reference the output data packet location. In one embodiment, a destination descriptor entry references the output data packet location. The context control block may reference new or updated compression or encryption control variables generated by one of the two processors.

Another embodiment is directed to an apparatus for communicating between a first processor and a second processor with respect to data associated with a plurality of data paths. The apparatus includes a shared memory having an input packet location and an output packet location, and a descriptor ring including at least one descriptor entry. The descriptor entry includes a context control block pointer

and an input packet pointer. In one embodiment, the descriptor entry also includes an output packet pointer. Alternatively, a destination descriptor entry may be provided which includes the output packet pointer.

A further embodiment is directed to an apparatus for communicating between a first processor and a second processor with respect to data associated with a plurality of data paths, comprising a plurality of context control blocks, an input data packet stored in a first input packet location, a descriptor entry including a context control block pointer and an input packet pointer that references the first input packet location. The apparatus may also include an output packet pointer. In this embodiment, the second processor uses the appropriate context control block to create an output data packet from the input data packet. The second processor may also create new or updated compression or encryption control variables, and update the context control block to reference these variables.

In any of these embodiments, the descriptor entry may include a command block which may be written to and read from to further facilitate communications. In alternate embodiments, the context control block references compression data, encryption data, or both. In further embodiments, a second descriptor ring may be created which is associated with another physical data path or another virtual data path.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the present invention shall appear from the following description of an exemplary embodiment, said description being made with reference to the appended drawings, of which:

FIG. 1 is a block diagram of a communications router within which several data paths may exist;

FIG. 2 is a diagram illustrating a descriptor ring in accordance with an embodiment of the invention, which may reside within the communications router;

FIG. 3a shows detail of a descriptor entry, contained within a descriptor ring, in accordance with an embodiment of the invention;

FIG. 3b shows detail of a bottom descriptor entry also contained within a descriptor ring, in accordance with an embodiment of the invention;

FIG.4 shows detail of a context control block in accordance with an embodiment of the invention;

FIG. 5 is a flow diagram of a process in accordance with the teachings of the invention;

FIG. 6 shows an alternate embodiment which includes several descriptor rings;

FIG. 7 shows detail of an exemplary source descriptor entry within one of the source rings shown in FIG. 6;

FIG. 8 shows detail of an exemplary destination descriptor entry within one of the destination rings in FIG. 6; and

FIG. 9 illustrates an alternate form of a context control block, which may be compared with FIG. 4.

DETAILED DESCRIPTION

FIG. 1 shows an illustrative system in which a main processor 1 communicates with a coprocessor 6 via a shared memory such as RAM 7. The elements shown have access to interface bus 8. In particular, FIG. 1 illustrates an architecture of a communications bridge or router for receiving data traffic from a Local Area Network (LAN) segment and transporting the data traffic across an appropriate Wide Area Network (WAN). Additionally, the router may support data traffic to and

from any of the LAN or WAN interfaces. LAN interface 2 provides the LAN interface functions, for example Ethernet protocol processing if the LAN is an Ethernet network. Additionally, when a communications packet is received by LAN interface 2, LAN interface 2 places the packet into Random Access Memory (RAM) 7. One of the WAN interfaces 3, 4, 5 may then read the packet from RAM 7 and transport the packet to the appropriate WAN. Direct Memory Access Controller (DMA) 9 may also be provided to support memory transfer functions for the main processor 1 and coprocessor 6. In one embodiment, the DMA 9 is embedded within coprocessor 6. A system such as that shown in FIG. 1 may include any number of interfaces and is not limited to either the number or the type of interfaces shown. Additionally, when a packet is received by a WAN interface 3, it will be placed in RAM 7 to be transported to the appropriate WAN or LAN.

In such a system, it is often desirable to either compress or encrypt the data packet before transporting the data packet out of the router. For example, the bandwidth available across a WAN may be much smaller than the bandwidth of a LAN. Accordingly, compression of a packet before transmission on a WAN will save transmission time on the WAN. Additionally, networks have varying degrees of security. For example, a WAN may be less secure than a LAN. Accordingly, it is often desirable to encrypt the packet prior to transmission on a WAN. Compression and encryption may be performed serially or simultaneously on a single packet.

Compression and encryption techniques frequently require maintenance of associated data. This data, which normally contains a collection of variables associated with a given data path, is called a context.

The nodes for a data path are generally a source and destination computer defined for a particular packet. For example, a data path may define the routing performed when a data packet is transmitted from a first communications node to a second communications node. A path that defines the actual communications nodes that the packet will pass through is called a physical data path. A virtual data path is defined by other parameters, such as simply source and destination, or some other classification of the data within the packet. Additionally, a physical data path may have many virtual data paths, each of which will result in a packet being transmitted from a first communications node to a second communications node. With respect to a system such as the router shown in FIG. 1, a first physical data path may be defined by a path in which a packet is received by the LAN interface 2 to be provided to WAN interface 3, whereas a second physical data path may be defined by a path in which a packet is received by the LAN interface 2 to be provided to WAN interface 4. Additionally, however, different data packets may have different virtual data paths even though they are destined to both travel from LAN interface 2 to WAN interface 3, for example. This may be due to the fact that they originate from different communications nodes, or simply are associated with data which requires different compression or encryption.

In compression techniques, the context for a given data path typically includes an adaptive dictionary dependent upon previously processed data, as well as pointers used for the maintenance of the adaptive dictionary. Additionally, error detection variables and buffers may be maintained for each context.

In encryption techniques, the context for a data path typically includes encryption keys and initialization vectors associated with the data path, and other variables used for maintenance of the data path.

Furthermore, since compression and encryption techniques are often very specialized, the compression and encryption functions may often be performed more efficiently using a coprocessor 6 which may be designed specifically to perform compression, encryption, or both. Coprocessor 6 may also have its own RAM 8. In a system such as that shown in FIG. 1, the coprocessor 6 performs most of the processing associated with compression and encryption. Alternatively, several coprocessors may perform this processing. Main processor 1 communicates with coprocessor 6 in order to, for example, command the coprocessor 6 to perform encryption on a received packet, or to indicate the manner in which the encryption should be performed. The coprocessor 6 performs the encryption using the context associated with the data path of the received packet, and provides completion and

error status back to main processor 1. The appropriate WAN interface 3 may then transport the encrypted packet.

As described above, the communications between the main processor 1 and coprocessor 6 may be performed using a shared memory, such as RAM 7. In such an instance it may not be desirable to have several queues, each for one of the possible data paths having an associated context.

A descriptor ring is a particular type of queue which contains data within the shared memory. A pointer is used to identify the appropriate entry in the descriptor ting. For example, the main processor 1 may set a pointer to reference the next packet which the coprocessor 6 is to compress or encrypt. The main processor 1 may then increment this pointer to reference the next location when a new packet is received. Generally, a descriptor ring contains an entry, at the bottom location, which references the top entry. In this manner, when the main processor 1 reaches the bottom entry, the main processor 1 knows to put the next packet or descriptor data for the next packet into the top location.

A queue or a descriptor ring for such a communications technique may be implemented by providing a separate queue or descriptor ting for each data path, since the context may be different for each data path. Referring to FIG. 1, one descriptor ting would be associated with the physical data path from the LAN to the WAN connected to WAN interface 3, and another descriptor ring would be associated with the physical data path from the LAN to the WAN connected to WAN interface 4. This arrangement may result in processing inefficiencies since both the main processor 1 and the coprocessor 6 must poll each descriptor ring.

In one embodiment of this invention, a descriptor ring is provided which supports more than one context, and can therefore support more than one data path. FIG. 2 is a block diagram of such a descriptor ring, which may reside within RAM 7 and be controlled by main processor 1. As shown in FIG. 2, an entry in descriptor ring 12 is referenced by pointer 14. Several context control blocks 16A-16N may be associated with descriptor ring 12. An entry in the descriptor ring 12 generally includes three pointers. One pointer references a location in RAM 7 which contains a packet which was received, referred to as source packet 18. Another pointer references the appropriate context control block 16, for example the context control block that is associated with the data path of the packet. A third pointer references a location referred to as the destination packet location 20, which represents the location where coprocessor 6 will store the results of the encryption or compression. Several entries may reference the same context control block 16, for example if several packets were received with the same data path. If implemented as a ring, the bottom entry 22 may reference the top entry 24. In one embodiment the descriptor ring 12 may be implemented in a memory such as RAM 7 and controlled by main processor 1.

However, as will be readily apparent to those skilled in the art, the descriptor ring 12 and associated pointer 14 may be implemented in special purpose hardware. For example, descriptor ring 12 could be implemented in a First In First Out (FIFO) memory, with pointer 14 being a pointer circuit which tracks access by main processor 1 and coprocessor 6.

A more detailed view of a descriptor entry in descriptor ring 12 is illustrated in FIG. 3a. In this embodiment, each descriptor entry has a status field 32, an error detection field 34 such as a Longitudinal Check Byte (LCB) field, destination packet length 36, source packet length 38, context control block offset 40, pointer to source packet 42, and pointer to destination packet 44. In this embodiment, the status field 32 may be used to communicate commands and replies between main processor 1 and coprocessor 6. The destination packet length 36 and source packet length 38 define the size, respectively, of the destination and source packets. Context control block offset 40 references the location of the appropriate context control block 16, and pointer 42 and pointer 44 reference the respective locations of the source and destination packet.

As depicted in FIG. 3b, the bottom descriptor of descriptor ring 12 contains wrap status 46 (8 bits for a preferred embodiment), and pointer to first descriptor 48 (i.e., points to descriptor entry 24).

FIG. 4 shows detail of a context control block 16 for encryption. A context control block for compression is similar, but instead of information regarding encryption such as encryption keys, a compression context control block references compression information such as an adaptive dictionary. Context status field 94 provides information regarding the status of the context control block 16. Error correction field 34 is also provided, along with insert and check pointer field 95. Context type field 96 is used to establish the type of context, in order to allow unique control over each context without real time processing intervention. Context pointer 97 may reference a location of any other data relevant to encryption, such as a history buffer. Since FIG. 4 is an example of an encryption context control block, it contains search depth field 98, along with encryption key fields 99A and 99B.

Since each source packet is associated with a particular data path, it will be processed according to the context associated with that particular data path. As discussed above, each data path may have its own particular context, for example state information and compression history. This context is used by coprocessor 6 when a source packet is processed to create a destination packet, and may be updated when the process is completed. In a preferred embodiment, context control block 16 also references other locations that contain control variables such as a dictionary, history information, or encryption keys, instead of the context control block containing the dictionary itself.

FIG. 5 is a flow chart showing a method according to an exemplary embodiment of the invention. In step 62, context control blocks are created. If the data for these context control blocks 16A-16N previously exists, the appropriate data or referencing information is simply stored in an appropriate location. As new information is received, context control blocks 16A-16N may be updated. The information for a context control block may be received from an external device such as a network controller, or may be stored in memory associated with main processor 1. In step 64, an input packet is received, for example a source packet received by LAN interface 2. In step 66, a corresponding context control block 16 is determined. If a corresponding context control block 16 does not exist, one may be created in step 68. Alternatively, the lack of a corresponding context control block 16 may be indicative of an error. If so, an appropriate error message may be generated. From step 66 or step 68, the process continues to step 70. In step 70, an entry for the input packet is created in the descriptor ring. As described above, the entry includes a context control block pointer, an input packet pointer, and an output packet pointer. Additionally, it may include a status entry or other information.

In step 72, a command is written to RAM 7, in order to command coprocessor 6 to perform a function, and in step 74 the command is received and read by the coprocessor 6. The coprocessor 6 performs the function by processing the entry, and creates an output packet in step 76. The output packet is stored in a location defined by the entry created in step 66. In step 76, the status is updated, generally by coprocessor 6, to inform the main processor 1 that the processing has been completed. Additionally, the main processor 1 may update pointer 14.

FIG. 5 also depicts step 80, in which the contents of the corresponding context control block is updated. This is an optional step, which is performed if the step 76 of processing the entry resulted in a modification of the compression or encryption control variables referenced by the context control block. For example, if the step of processing the entry 76 was a compression which used an adaptive dictionary, then pointers pertaining to the adaptive dictionary may be updated as a result. If the step of processing the entry 76 was an encryption, the initialization vectors within the context control block 16 may be updated as a result of the encryption.

In another embodiment, status block 32 may include two or more status blocks, for example one command block which can contain commands from main processor 1 to coprocessor 6, and one response block which contains responses from coprocessor 6 to main processor 1.

Alternatively, instead of utilizing a status block 32 for command and status information communicated between the main coprocessor 1 and coprocessor 6, known communications techniques may be used. In such an embodiment, steps 72, 74, and 78 may be achieved in any manner, for example the main processor 1 may modify a register within coprocessor 6 to provide a

command.

By using a descriptor ring 12 which can reference several context control blocks, less polling is required by the main processor and coprocessor than would otherwise be required. Accordingly, the processing may be performed more efficiently and may result in an increase in throughput.

As described above, a single descriptor ring 12 may be provided to support an entire router system as shown in FIG. 1. However, it may be advantageous to provide two or more descriptor rings 12, for example, if processing efficiency might be improved. This may be the case if communications in one direction have an equal or higher priority than communications in another direction. An example of this would be one descriptor ring 12 for data in one direction, for example from the LAN to any one of the WANs, and another for the opposite direction, for example from any one of the WANs to the LAN. Furthermore, it is possible to provide several descriptor rings. Even in such an instance, the advantage is that each descriptor ring may reference several context control blocks. Moreover, instead of allocating descriptor rings based on direction as described above, it also may be advantageous to allocate descriptor rings based on the function being performed on the source packet. An example of such an allocation is described below.

In one embodiment, a coprocessor 6 supports four descriptor rings. The rings are allocated depending upon the operating mode of the coprocessor 6. In one operating mode the rings are allocated as two independent descriptor rings for compression, and two independent descriptor rings for decompression. Alternatively, in a mode referred to as fragmentation mode, the rings are allocated as source and destination ring pairs for compression and decompression.

An example of four rings in fragmentation mode is illustrated in FIG. 6, which shows compression source descriptor ring 82, compression destination descriptor ring 84, decompression source descriptor ring 86, and decompression destination descriptor ring 88. Associated with each ring is one of the buffers 90A-90D. Also associated with the source rings 82, 86 are context control blocks 16A-16N. In FIG. 6 only one arrow is shown going to each buffer 90A-90D and to context control blocks 16A-16N for simplicity, but as in the previous embodiments, each ring may contain several entries, each of which has such a pointer. As in the embodiment shown in FIG. 2, a pointer or pointers 81 may be provided to track the descriptor entry to be processed.

In operation, entries within the source tings 82, 86 reference the appropriate context control block 16 as well as a location within the associated buffer 90A, 90C which contains the source packet. In this manner, coprocessor 6 processes the source packet using data referenced by the appropriate context control block 16, to generate a destination packet.

Entries within the destination rings 84, 88 point to free locations (locations that do not contain current data) within buffers 90B, 90D. Then, when a destination packet is prepared by coprocessor 6, a location within buffer 90B or 90D may be appropriated. This appropriation may be performed by DMA 9, which may also provide other memory transfer functions.

FIG. 7 shows detail of an exemplary source descriptor entry within one of the source rings 82, 86. FIG. 8 shows detail of an exemplary destination descriptor entry within one of the destination rings 84, 88. FIGS. 7 and 8 may be compared with FIG. 3A, and similar elements are given similar reference designations. In FIG. 7, however, no information is needed regarding the location of the destination packet, because this information is provided by destination descriptor rings 84, 88. Similarly, the destination entry of FIG. 7 does not need information regarding the source packet. Instead, the destination entry provides destination packet pointer 44 and destination packet length 94.

FIGS. 7 and 8 also show Channel ID/Sequence number field 92. This field provides identifying information which may associate a number of locations within one of the buffers 90A-90D. For example, complete communications packets received for processing may be of varying size. Therefore, it may be advantageous to segment a complete packet into several source packets which are more appropriate for processing. Once these complete packets are segmented, the channel ID/Sequence number field 92 provides an identifier which would associate the source packets which

together make up the complete packet.

An alternate form of a context control block 16 is depicted in FIG. 9, which may be compared with FIG. 4. Instead of encryption key fields 99A and 99B, encryption variables pointer 101 references a location in memory that contains the appropriate encryption key, as well as the initialization vectors to be used with the context control block. FIG. 9 also shows a frame relay control field 100, which contains a command to DMA 9 to copy some of the data of the source packet directly into a destination packet without compression or encryption. This field may be used when, for example, a packet contains a header which identifies routing information. Since other nodes along the route which the packet will take will use the routing information, it may be preferred to leave the routing information in an uncompressed mode.

Having thus described several embodiments of the invention, various alterations, modifications, and improvements will readily occur to those skilled in the art. For example, the invention may be applied to other functions which lend themselves to coprocessing, such as signal processing or sorting functions in which different sort techniques are used depending upon the data to be sorted. In such examples, files of information are processed instead of the packets as described above. Furthermore, the context control blocks may be used to communicate between any two devices, such as two processors, or even among several devices. Such alterations, modifications, and improvements are intended to be within the spirit and scope of the invention. Accordingly, the foregoing description is by way of example only, and not intended to be limiting. The invention is limited only as defined in the following claims and the equivalents thereto.

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United States Patent **5,570,345**
Kaprielian , et al. **October 29, 1996**

Protection switching system with single line control

Abstract

The invention performs very fast switching between a main module and a standby module in the event of module failure. A single control line has different logic level signals applied thereto in the event of a main module failure and a standby module failure, with the signals on the control line being utilized to efficiently switch the on-line status of the modules to a desired state.

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Parent Case Text

This application is a Continuation-in-Part of application Ser. No. 08/220,975 filed Mar. 31, 1994 and the content of this application are incorporated herein by reference.

Claims

1. In a system having a main module and a standby module, only one of which is to be on-line at any given time, a circuit for controlling the one of said modules which is on-line comprising:

a single control line extending between the modules and receiving inputs from both modules;

means at the main module for applying a first signal to said control line when the main module fails;

means at the standby module for applying a second signal, different from the first signal, to the control line when the standby module fails; and

means responsive to a signal on the control line for selectively switching the on-line status of said modules in a manner such that only one of said modules is on-line at a time.

2. A circuit as claimed in claim 1 wherein said modules are communications modules through which the same traffic is simultaneously passed, and including a switch responsive to one of said modules being on-line for passing traffic outputted by the on-line module to a system output line.

3. A circuit as claimed in claim 1 wherein each of said modules may be in a good or a failed condition, and wherein said means for selectively switching is responsive to a signal on the control line to assure that where at least one of said modules is good, the module on-line in a good module.

4. A circuit as claimed in claim 3 wherein when both modules are good, said means for selectively switching does not change the one said modules which is on-line.

5. A circuit as claimed in claim 4 including means at each module for applying a signal to the control line to take the module off-line regardless of the condition of the module.

6. A circuit as claimed in claim 5 including at least one processor for said modules, and wherein said at least one processor causes signals to be applied to the control line to take a module off-line regardless of its condition.

7. A circuit as claimed in claim 3 wherein said means for selectively switching is operative, where both modules have failed, to cause the standby module to be on-line.

8. A circuit as claimed in claim 1 wherein said means for selectively switching including a switch for each module, the on-line status of each module being controlled by the state of the corresponding switch, and a gate for applying a control input to each switch, the gates both receiving the signal on the control line as an input and generating outputs to control their respective switches to opposite states in response to a given signal on the control line.

9. A circuit as claimed in claim 8 wherein said gates are exclusive-OR gates, wherein said signals are voltage levels, and wherein a voltage level which is the same as that for the second signal is applied as a second input to the exclusive-OR gate for the main module, and a voltage level which is the same as that for the first signal is applied as a second input to the exclusive-OR gate for the standby module.

10. A circuit as claimed in claim 1 including a processor for each module, and wherein both processors cause the second signal to be applied to the control line when the main module is on-line and good, while the processor for the standby module causes the first signal to be applied to the control line after the main module fails.

11. In a system having a main module and a standby module, only one of which is to be on-line at any given time, a circuit for controlling the one of said modules which is on-line comprising:

a single control line extending between the modules and receiving inputs from both modules;

a circuit at the main module which applies a first signal to said control line when the main module fails;

a circuit at the standby module which applies a second signal which is different than the first signal to the control line when the standby module fails;

a gate for each module, the control line being connected as one input to each gate, the gates generating different outputs in response to a given signal on the control line; and

a switch for each module which control the on-line states of the module, each of said switches being responsive to one of the outputs from the corresponding gate for being enabled and to the other output from the corresponding gate for being disabled.

12. A circuit as claimed in claim 11 wherein said gates are exclusive-OR gates, wherein said signals are voltage levels, and wherein a voltage level which is the same as that for the second signal is applied as a second input to the exclusive-OR gate for the main module, and a voltage level which is the same as that for the first signal is applied as a second input to the exclusive-OR gate for the standby module.

Description

FIELD OF THE INVENTION

This invention relates to systems for controlling the on-line status of a main and a protection or standby module in a system where only one such module is on-line at any given time, and more particularly to such a system which utilizes a single control line for the modules to effect more rapid switching if one of the modules fails or if it is otherwise desired to switch between modules.

BACKGROUND OF THE INVENTION

In systems where high reliability is required, such as in telephony or other communication systems where a significant loss of traffic is unacceptable, it is common to provide redundant modules in the system which operate in parallel on the same inputs. Normally the output from only one such module is utilized, with the system switching to utilize outputs from the other module in the event of a failure in the original module. Since once a module fails, data outputted from that module is unreliable, it is desirable to get a failed module off-line as quickly as possible. Further, since a delay in getting the standby module on-line can result in data being lost, it is also desirable to get The standby module on-line as quickly as possible. However, there has heretofore been a relatively complicated protocol, particularly in communications applications, to communicate a failure to both modules and to then effect the necessary switching to get the failed module off-line and a good module on-line. This has resulted in either excessive switching delay, due to slow message oriented communication protocols on a shared hardware resource, or an unreasonably large number of backplane connections to control switching between the working or main and protection or standby modules. Often the number of backplane connections dictate the number of features a given module can offer. Therefore, while dedicated hardware allows for very fast switching, it also limits the modules features. However, with the high speed data transmission lines currently being utilized, this excessive delay can result in the loss of substantial data. Further, since once a module fails, it is assumed to be unreliable, any switching to a replacement module must be done without involvement of the failed module, main and standby modules should also be identical so as to be interchangeable.

It is therefore desirable that a technique be developed which substantially reduces the time delay between the detection of a module failure and the completion of a replacement module being brought on-line, while requiring a minimum number of backplane connections, and without requiring involvement of a failed module in the switching process.

SUMMARY OF THE INVENTION

In accordance with the above, this invention performs very fast switching through a dedicated single hardware connection per switched circuit. A background message oriented communication scheme is also required to update the state models in each module, but this update can be quite slow. More specifically, the invention provides a single control line which has different signals applied thereto in the event of a main module failure or a standby module failure. These signals are utilized to selectively switch the on-line status of the modules to a desired state.

More particularly, a circuit is provided for controlling which one of a main module and a standby module are on-line at any given time. The single control line extends between the modules and receives inputs from both modules. The main module applies a first signal to the control line when the main module fails or is otherwise taken off-line, and the standby module applies a second signal to the control line when the standby module fails or is otherwise to be taken off-line. Circuitry is provided which is responsive to the signal on the control line for selectively switching the modules such that only one of the modules is on-line at a time. For a preferred embodiment, when only one of the modules is good, the good module is the one which is on-line; where both modules are good, the current on-line status of the modules is maintained; and where both modules have failed, the system can cause either of the modules to be on-line (for the preferred embodiment, the standby module is chosen to be on-line in this circumstance).

Each module may also apply a signal to the control line to take the module off-line regardless of the condition of the module. Thus, the module may be taken off-line for preventive maintenance or for other purposes. In particular, at least one processor may be included which causes signals to be applied to the control line to take a module off-line. There may be a separate processor associated with each module or the signals may be derived from a background processor.

A switch may also be provided for each module with the on-line status of each module being controlled by the state of the corresponding switch. A gate may also be provided for each module for applying a control input to the corresponding switch, the gate receiving the signal on the control line as an input and generating outputs to control their respective switches to opposite states in response to a given signal on the control line. For a preferred embodiment, the gates are exclusive-OR gates, their signals are binary voltage levels, a voltage level which is the same as that of the second signal is applied as a second input to the exclusive-OR gate for the main module and a voltage level which is the same as that for the first signal is applied as a second input to the exclusive-OR gate for the standby module. With a processor for each module, both processors cause the second signal to be applied to the control line when the main module is on-line and good while the processor for the standby module causes the first signal to be applied to the control line after the main module fails.

The foregoing other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention as illustrated in the accompanying drawings.

IN THE DRAWINGS

FIG. 1 is a schematic semi-block diagram of a system in accordance with the teaching of this invention.

FIG. 2 is a chart illustrating the value on the control line and the module on-line for the various status conditions of the modules.

DETAILED DESCRIPTION

Referring first to FIG. 1 a system 10 is shown which includes a main module 12A and a standby module 12B. For preferred embodiments, the main and standby modules are identical and are interchangeable, the difference being, as will be discussed later only in their location with respect to backplane/background circuitry. Each module receives traffic derived from a common input source

14, which traffic may be data, voice, video or other information depending, on the nature of the system. Lines 14 may be wire or fiber optic telephone lines, or may be lines or cables of some other communications network. Modules 12 would typically be located at a control unit, an end office, a central office, or the like for a telephony system (see parent application) or some other appropriate control station for other types of communications system. Each module contains a microprocessor 16A, 16B which may communicate with a background/backplane processor (not shown) over bidirectional lines 17A, 17B respectively, and which, either alone or in conjunction with other circuitry not shown, may perform selected operations on the received data. For example, each module 12 may also receive additional data from other sources over additional lines and may multiplex such received data before outputting the data on output lines 18A, 18B from the module, or the module may perform other operations on the data which are known in the art. The exact function of the modules is not part of the present invention. What is important is that the operations performed on incoming data by both main module 12A and standby module 12B are identical, so that the outputs appearing on output lines 18A and 18B are also identical. The outputs on lines 18A and 18B are applied through switches 20A and 20B respectively to a common system output line 21. The module 12 which is on-line at any given time is determined by which of the switches 20 is enabled or closed. The system is designed so that only one of the switches 20 will be enabled at a time.

Each switch 20 receives an enable input from a corresponding exclusive-OR gate 22A, 22B with each switch 20 being closed or enabled when the corresponding exclusive-OR gate 22 generates a ZERO or ground output and being opened or disabled when the corresponding exclusive-OR gate 22 generates a ONE or V+ output.

One input to each exclusive-OR gate 22 is the output from an inverter 24A, 24B respectively. The input line 25A, 25B to each inverter is connected to a terminal T.sub.A, T.sub.B respectively. These terminals connect to corresponding terminals 27A and 27B on the backplane for the slot position in which the module is mounted, the terminal 27A for the main module position having a voltage V+ applied thereto, which voltage is the same as that of a logical ONE level. This voltage on the terminal 27A defines the slot as a main module slot. Similarly, the backplane terminal 27B has a ground or ZERO level applied thereto, this level on terminal 27B defining the slot as a standby module slot. Thus, a module 12 becomes a main or standby module depending on the potential on terminal 27 for the slot in which the module is mounted. Line 28 is connected as the second input to gate 22A through a resistor 30A and as the second input to gate 22B through a resistor 30B.

The effect of the inputs to exclusive-OR gate 22A is that it does not alter the signal on common control line 28, the logical output from this gate being the same as The logical input received by this gate on line 28. However, exclusive-OR gate 22B inverts the signal on common control line 28. Thus, while switch 20A is closed, switch 20B is open, and while switch 20A is open, switch 20B is closed. Therefore, only one of the modules can be on-line at any given time.

The portion 28A, 28B of control line 28 on the module side of each resistor 30 has a number of connections thereto. In particular, there is a noise filter 32A, 32B connected to control line portions 28A, 28B, respectively, each noise filter consisting of a resistor 34A, 34B respectively, and a capacitor 36A, 36B respectively. An AND gate 38A, 38B is connected to each corresponding common line portion through a corresponding diode 40A, 40B. One input to gate 38A is line 25A from terminal T.sub.A (i.e., a V+ or logical ONE level) and one input to gate 38B is line 25B from terminal T.sub.B (i.e., a ground or logical ZERO level). The other input to gate 38A is a signal on line 42A which is indicative of failure in main module 12A/main processor 16A, while the second input to gate 38B is a signal on line 42B which is indicative of a failure in standby module 12B/standby processor 16B. For the preferred embodiment the signals on lines 42A and 42B, are obtained from a background computer (not shown) which periodically interrogates the microprocessors and/or other portions of the modules and generates an output on the appropriate line 42 if a suitable response is not received to the interrogation.

A signal on a line 42 is also applied through a corresponding inverter 44A, 44B as a logical ZERO "clear" input to a corresponding write register 46A 46B. In normal operation the write register receives outputs from the corresponding microprocessor 16. Appropriate outputs from the write

14, which traffic may be data, voice, video or other information depending, on the nature of the system. Lines 14 may be wire or fiber optic telephone lines, or may be lines or cables of some other communications network. Modules 12 would typically be located at a control unit, an end office, a central office, or the like for a telephony system (see parent application) or some other appropriate control station for other types of communications system. Each module contains a microprocessor 16A, 16B which may communicate with a background/backplane processor (not shown) over bidirectional lines 17A, 17B respectively, and which, either alone or in conjunction with other circuitry not shown, may perform selected operations on the received data. For example, each module 12 may also receive additional data from other sources over additional lines and may multiplex such received data before outputting the data on output lines 18A, 18B from the module, or the module may perform other operations on the data which are known in the art. The exact function of the modules is not part of the present invention. What is important is that the operations performed on incoming data by both main module 12A and standby module 12B are identical, so that the outputs appearing on output lines 18A and 18B are also identical. The outputs on lines 18A and 18B are applied through switches 20A and 20B respectively to a common system output line 21. The module 12 which is on-line at any given time is determined by which of the switches 20 is enabled or closed. The system is designed so that only one of the switches 20 will be enabled at a time.

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A signal on a line 42 is also applied through a corresponding inverter 44A, 44B as a logical ZERO "clear" input to a corresponding write register 46A 46B. In normal operation the write register receives outputs from the corresponding microprocessor 16. Appropriate outputs from the write

register 46 are applied through a corresponding diode 48A, 48B to the corresponding common control line portions, 28A, 28B. Finally, signals on the control line at each module are applied through a corresponding read register 50A, 50B to the corresponding microprocessor.

In operation, assume that main module 12A is initially on-line, that standby module 12B is initially off-line, and that both modules are initially good. This is the situation illustrated on the third line in FIG. 2 which indicates that the control line is at ZERO or ground potential under this situation. Thus, in order to maintain a main module in an on-line condition, a ground potential or logical ZERO must be applied to control line 28 by both microprocessors 16A and 16B through their respective write registers 46A and 46B. Microprocessor 16A will normally provide a logical ZERO to its write register when the module is good. However, microprocessor 16B, knowing from its backplane inputs that it is part of a standby module, would normally apply a +V or logical ONE level to its write register when the module is good and the standby module is on-line. However, when the main module is on-line, this information is communicated through a background communication path and through line 17B to microprocessor 16B. This input causes microprocessor 16B to generate a ZERO output to its write register even though the module is good. Thus, all inputs to the control line are at a logical ZERO level, resulting in a logical ZERO output from exclusive-OR gate 22A to enable switch 20A and resulting in a logical ONE output from exclusive-OR gate 22B (this gate inverting the level on control line 28) to disable switch 20B thereby rendering the standby module off-line. Thus live traffic passes through switch 20A and is blocked by switch 20B.

The condition described above continues to exist so long as main module 12A remains good, and, referring to the first line of FIG. 2, will continue to exist even if standby module 12B fails, so long as main module 12A remains good.

However, if main module 12A fails, then the signal on the control line goes to +V or ONE. This may be accomplished in at least two ways. First, it may be accomplished by processor 16A either determining that for some reason such as a local fault, the main module should be taken off-line or, more likely, by a signal on line 17A from the background control processor ordering processor 16A to take module 12A off-line. When this occurs, the processor puts a logic level ONE signal through write register 46A onto the control line, causing the line to go to a logic ONE level. A second option is that the background processor does not receive a proper response to an interrogation of the module and, as a result, puts a signal on line 42A which, since there is always a logic ONE on line 25A, is passed by AND gate 38A and diode 40A to put a logic ONE on the control line. Read registers 50A and 50B detect the ONE on the control line and provide inputs to their respective microprocessors that a failure has occurred in the main module. The signal on line 42A is also inverted by inverter 44A to clear write register 46A to generate a logic ZERO.

Following a switch from main to standby on-line switch positions, the standby microprocessor by interrogating read register on port 50B also writes a logical ONE on its write register or port output 48B, and then sends a message through lines 17B and the system control bus (not shown) that it is on-line. If the main microprocessor 16A is subsequently operating successfully, and the conditions forcing the initial switch action passes, or is otherwise corrected, the main microprocessor puts a ZERO on its write register 46A output. However, a logical ONE level remains on the control line as a result of the logical ONE output onto the control line from write register 46B. Note that the system state has changed from main and standby good, main on-line to main and standby good, standby on-line. Also the main module microprocessor has positioned itself such that a single switch command from the on-line standby microprocessor will simultaneously force both main and standby switch actions.

It should again be noted that the main module may be taken off-line for reasons other than failure. For example, the main module may be taken off-line to permit routine maintenance to be performed on the main module card, to permit replacement of the card, or for other reasons, The decision to take the main module off-line can be made at microprocessor 16 or can be made by the microprocessor in response to instructions from a background processor.

However the ONE signal on control line 28 originates, the ONE on this line, in conjunction with the

ZERO input from inverter 24A into exclusive-OR gate 22A, causes the gate output to go to a ONE or +V, thereby disabling switch 20A and taking main module 12A off-line. Simultaneously with this occurring, the ONE on the control line, in conjunction with the one output from inverter 28B causes exclusive-OR gate 22B to generate a ZERO output on line 26B which enables switch 20B putting standby module 12B on-line. Since the two switches operate simultaneously in response to the same signal on a single control line, the switching can occur very quickly, for example within 50 milliseconds, thereby minimizing loss of data. Once the switching has occurred, The switches are maintained with switch 20B enabled and switch 28A disabled.

The system remains in a condition with the standby module on-line until either the standby module fails at a time when the main module is good or until a decision is made by standby microprocessor 16B, the background processor, a system operator or otherwise to take the standby module off-line. In particular, referring to the fourth line in FIG. 2, even if the main module becomes good while the standby module is on-line, the logic ONE continues to exist on the control line so that the system remains with the standby module on-line. When the standby microprocessor 16B detects an internal fault (or is instructed to take the module off-line) or when the background processor does not receive a proper response to an interrogation of module 16B, a ZERO is set on the output of register 46B either by processor 16B or by a fail signal on line 42B being inverted by inverter 44B to clear the write register. The later operation is required since a failed processor 16B cannot be relied upon to take itself off-line. Together with the ZERO potential existing on the good main module microprocessor's write register, this forces the standby switch 20B off-line and the main switch 20A on-line. (Note that unlike the AND gate 38A for the module positioned in the main slot, AND gate 38B for the standby module is unable to pass the standby processor fail signal on line 42B to the common control line because line 26B is permanently held at ZERO.)

On the simultaneous occurrence of both main and standby module failures, the system will be positioned to standby on-line. This is because a standby failure generates a ZERO at write register 46B while a main failure generates a ONE at either write register 46A or diode 40A. Since all driving signals are diode applied to the common line, a ONE on any source for the control line overrides all other ZERO'S, forcing the system to standby mode.

While the invention has been described above with respect to a communications application, and that is the application where main and standby modules are most frequently utilized, the single line control concept of this invention might also be utilized in other applications where high reliability is required, where such reliability is achieved by use of redundant modules, and where a need exists to rapidly switch a new module on-line in the event the module currently being used fails. Further, while specific circuitry has been shown in FIG. 1 for implementing the invention, such implementation is provided for purposes of illustration only and other circuitry capable of implementing the concepts of this invention may be utilized to implement the invention. In particular, depending on applications, the level or logical state on the control line which is used to bring the main and standby modules on-line may be varied, default conditions when both modules are good or when both modules fail may be altered, and the specific circuitry/controls for putting required potentials on the control line and for switching modules in response to such potential may also vary.

Thus, while the invention has been particular shown and described with reference to a preferred embodiment, the foregoing and other changes in form and detail may be made therein by one skilled in the art without departing from the spirit and scope of the invention.

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United States Patent **5,526,363**
Weiss , et al. **June 11, 1996**

Multicontext compression system with shared data structures

Abstract

A system for transmitting compressed data for multiple channels or contexts from a single node which system reduces memory utilization without significant adverse effect on compression ratio by providing a separate history buffer for each channel, with a single hash table being provided for generating potential match addresses in the history buffer for at least selected ones of the channels. A single chain table may also be provided, the chain table having a single offset address for the corresponding offset addresses in the buffers for the selected channels. Collisions in the common hash table may be reduced by including channel address or the like as an additional input to the hash table, thereby biasing the address outputs therefrom.

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Claims

1. In a system for transmitting compressed data for multiple contexts from a single node, apparatus for facilitating reduced memory utilization comprising:

a history buffer for each of said contexts; and

a single hash table for generating potential match addresses in the history buffers for at least selected ones of the contexts, the hash table including means for overwriting address entries for one context in the hash table with address entries for a succeeding context when collisions occur in the hash table.

2. Apparatus as claimed in claim 1 including a single chain table having a single address location for

substantial loss in compression ratio caused by the resetting of data structures, and in particular history buffers, at frame or channel transitions.

SUMMARY OF THE INVENTION

In accordance with the above, this invention provides a system for transmitting compressed data for multiple channels or contexts from a single node, which system reduces memory utilization by sharing at least some data resources while minimizing the adverse effects on compression ratio resulting from such sharing. In particular, a separate history buffer is provided for each channel or context, with a single hash table being provided for generating potential match addresses in the history buffers for at least selected ones of the channels. Where the number of channels is more than can be served from a single hash table/chain table without excessive collisions, two or more shared tables may be provided, with each shared table serving selected channels. Rather than being reset at each frame or channel transition, address entries in the hash table for one context are overwritten with address entries for a succeeding context when collisions occur in the hash table. A single chain table may also be provided, the chain table having a single offset address for the corresponding offset addresses in the buffers for the selected channels. Address entries for one context in the chain table are also overwritten with chain address entries for a succeeding context when collisions occur in the chain table.

Since the overwriting indicated above will result in some searches for a given context being performed at invalid addresses, the depth of searches in the chain table is limited so as to reduce the processing penalty caused by such invalid searches. The likelihood of collisions occurring in the hash table, and thus the likelihood of a search being attempted at an invalid entry, is reduced by having a hashing element or circuit for generating addresses in the single hash table, which element receives as inputs both the data for the channel or context currently being transmitted and an input indicative of the channel or context for the given input. The hashing element is responsive to the input indicative of context for generating a different hash table address for each context for at least selected input character combinations. Thus, by statistical selection of these biased entries, the likelihood of collisions occurring in the hash table can be significantly reduced.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention as illustrated in the accompanying drawings.

IN THE DRAWINGS

FIG. 1 is a block diagram of an exemplary system in which the teachings of this invention may be employed.

FIGS. 2A, 2B and 2C are diagrams of memory allocation for three different embodiments of the invention.

FIG. 3 is a flow diagram of a method for transmitting multichannel, multicontext data frames in accordance with the teachings of this invention.

DETAILED DESCRIPTION

FIG. 1 illustrates a data transmission system of the type in which the teachings of this invention might be utilized. The system has a plurality of nodes 12A-12N which communicate with each other through a data transmission network 14. Data transmission network 14 may, for example, be a telephony network which may include copper and/or fiber optic wires, cables, microwave or radio transmissions, or the like, with the data, depending on the length of the virtual channel between nodes, also being adapted to pass through various end stations, central stations and other intermediate nodes in completing a virtual channel. Further, particularly where the nodes being connected by a virtual channel are separated by a substantial distance, there may be an almost infinite number of ways in which the channel interconnecting the two nodes may be formed. However, the nature of the

network 14 is such that, as for most telephone systems, any node on the system may communicate with just about any other node on the system. Further, each node may be simultaneously sending messages, which messages may use substantially different vocabularies, to two or more nodes through multiple channels, with the messages for the various nodes being interleaved at the output from the node.

For purposes of illustration, each node 12 is shown as including a processor 16 and a memory 18 (only the processor and memory for node 1 being shown in the figure). Each node may also include substantial additional circuitry for performing various functions, which circuitry and functions will depend on application and environment. The processor 16 for this embodiment performs, among other functions, the function of data compression for the data being transmitted from the node, it being assumed that the data compression algorithm utilized employs string search algorithms so as to require history buffers and at least a hash table. Various Lempel-Ziv 77 algorithms are example of such string search algorithms.

As has been indicated earlier, in the prior art memory 18 has either had a separate history buffer, hash table and, where employed, chain table for each active channel or has used a single shared history buffer for a selected number of channels, with at least a hash table, and generally a chain table as well, also being shared for the same selected channels. These approaches can be combined with some channels having dedicated buffers et al. (i.e. contexts) while other channels share one or more contexts. Limitations for these approaches have been discussed earlier. In particular, they require a trade-off between a requirement for significant, expensive memory and substantial loss of compression ratio.

A memory 18 in accordance with the invention having a shared hash table is shown in FIG. 2A. This memory has a separate history buffer 20A-20D for each of four channels to which the node 12 is transmitting. For an illustrative embodiment, each of the buffers contains 8K bytes of eight bits each. A shared hash table 22 is also provided which for an illustrative embodiment may contain 32K eight-bit bytes, the memory 18 thus being a 64K byte memory. FIG. 2B illustrates the memory 18 for an alternative embodiment of the invention which also contains a shared chain table 24. For this embodiment of the invention, the four 8K byte history buffers 20A-20D are also provided, with hash table 22' being reduced to 16K bytes and chain table 24 being the same size. Thus, the memory 18 in FIG. 2B is also 64K bytes for the illustrative embodiment. FIG. 2C shows another embodiment of the invention where eight channels are serviced by two sets of tables, with one set of tables servicing channels A-D and the other set of tables services channels E-H. With all data structures being the same size as for the FIG. 2B embodiment, memory 18 for FIG. 2C would be 128K bytes. However, the memory size and the allocation of bytes to the various data resources within the memory for each of the embodiments are for purposes of illustration only and can vary substantially depending on the application and environment in which the system is used. Further, dedicated data resources may be provided for one or more channels in addition to the shared resources shown, and procedures may be provided for reallocating channels between shared resources and/or dedicated resources.

Referring to FIG. 3, in operation input characters for a selected channel are initially either received or generated at a node, for example node 1, during step 30. M characters of this input are then hashed along with the channel address or some other suitable indication of the channel in a suitable hash generator to generate a hash table address (step 32). For a preferred embodiment, M is three. Since the hashing is not only on the input characters, but also involves the channel address, the result of the hash step may be a different location in the hash table for the same character string for each of the channels. This means that common three letter combinations such as the letters "THE" or "ING" may be hashed to different addresses in the hash table for each channel to minimize the occurrence of collisions in the hash table for the varying channels. Thus, by selecting the letter combinations hashed to the same hash table address from the various channels so that a common letter combination such as "THE" for one channel is hashed to the same address as rarely occurring letter combinations from other channels, the incidence of collisions in the hash table can be kept low enough so as to minimize the adverse effect which such collisions would otherwise have on system throughput and, more important, on compression ratios achieved from the system. The biasing may be accomplished statistically, empirically, or by some combination of the two.

During step 34, the input characters are compared to characters in the history buffer for the selected channel, starting at the address from the hash table, to find the longest match. This is a standard procedure in Lempel-Ziv 77 algorithms for data compression and is performed in standard fashion.

Once step 34 has been completed, either resulting in a longest match being found, or in no match being found, the operation proceeds to step 36 to determine if there is a chain table address for the entry. If only a hash table is provided as for FIG. 2A, step 36 might not be performed, or if performed, would always yield a "NO" output. If there is a chain table address in chain table 24 for the entry, the operation proceeds to step 38 to determine if a fixed depth for chain searching has been reached. Fixed depth chain searches are frequently employed in the art and are of particular value in this application since, notwithstanding the biasing of the hash table entries, collisions in the hash table and/or chain table are still possible, so that an address obtained from the common hash table or common chain table may not be a valid address at which a possible match might occur in its channel history buffer for the given input. Under these circumstances, to minimize processing overhead, it is desirable that excess processing not be performed, and limiting the depth of search in the chain table is one way of controlling the amount of processing performed. The penalty for limiting the depth of chain searches is a slight decrease in compression ratios; however, since maximum length matches generally occur early in the chain, this decrease is normally not significant. Further, while the occurrence of collisions results in a modest decrease in compression ratios from what can be achieved with individual hash tables and chain tables for each channel, the compression ratios achieved are significantly better than those achieved with common history buffer. The reason for this is that, particularly with the biasing of the hash table addresses, the number of collisions is not that great, so that many of the hash table entries encountered by a new channel will be valid entries and any invalid, collision-altered entries are corrected to valid entries the first time they are used.

If during step 38 it is determined that the fixed depth search has not been reached, then search step 34 is repeated, starting at the address indicated by the chain table, and steps 36 and 38 are repeated for successive chain entries until either a "NO" output is obtained during step 36 or a "YES" output is obtained during step 38. When one of these events occurs, the longest match found during the search is encoded in standard fashion, generally as an offset and length, and is transmitted through the virtual channel to the receiving node (step 40). It is noted that only a history buffer is required at the receiving node since the coded message indicates the offset address position where the longest match occurred and neither a common hash table nor a common chain table are required to search for this address. Therefore, the teachings of this invention are employed only at a transmitting node.

The address in the common hash table 22 is then overwritten during step 42 with the address at which the first input character matched on is stored in history buffer 20 for the selected channel and, during step 44, the chain table entry at the address which corresponds to the address written in the hash table is overwritten with the address which was previously in the hash table. As indicated above, to the extent a conflict had previously occurred, so that the hash and chain table entries were invalid entries, steps 42 and 44 result in these entries now being valid entries for the selected channel through which messages are now being sent.

From step 44, the operation proceeds to step 46 to determine if there are more input characters from the selected channel. If a "YES" output is obtained during step 46, the operation returns to step 30 to receive the additional input characters for the selected channel and steps 32-46 are repeated with the new input characters to, if possible, match on and encode such characters. This sequence of operations is repeated for successive input characters for the selected channel until, during step 46, a "NO" output is obtained. When this occurs, the operation proceeds to step 48 to select a new transmission channel and the operation then returns to step 30 to start receiving input characters for this new channel. No housekeeping operations on the hash and chain tables are required at this time, with any collisions which may have occurred in the common hash and chain tables for the new selected channel since the last transmission for this channel being dealt with in the manner previously discussed. More important, the dedicated history buffer 20 for the channel is not reset at this time so that an extended history is available to match on the next time the channel is used. Where there are multiple shared tables, as for the embodiment of FIG. 2C, steps such as steps 32 and 36 which

involve the table would be performed in the appropriate shared tables 22', 24 for the given channel.

A system is thus described which significantly reduces memory requirements in string search data compression applications with virtually no increase in overhead operations and with only a modest decrease in system compression ratios. While the system has been described above with reference to preferred embodiments, which embodiments are assumed to be implemented in software on a general purpose processor at the transmitting node, the invention could also be practiced using special purpose hardware or a selected combination of hardware and software. Further, while specific implementations have been discussed above, the exact procedure will vary with the compression algorithm being utilized and with other factors. Thus, while the invention has been particularly shown and described above with reference to preferred embodiments, the foregoing and other changes in form and detail may be made therein by one skilled in the art without departing from the spirit and scope of the invention.

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United States Patent **5,526,362**
Thompson , et al. **June 11, 1996**

Control of receiver station timing for time-stamped data

Abstract

The invention provides a method and apparatus for controlling the timing at a receiving station for the receipt of asynchronous data transmitted with a time-stamp. The received data is passed through a buffer to the remainder of the station. A decoder at the receiving station generates an indication of buffer fill level and a local time-stamp is also generated. The output timing for the buffer is controlled by a circuit which is responsive to both a difference value off, received and locally generated time-stamps and to the fill level indication.

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Field of Search: 370/100.1,103,105.3,60,60.1,94.1 375/371,372,373,376

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Parent Case Text

RELATED APPLICATION

This application is a continuation-in-part of application Ser. No. 08/220,975 filed Mar. 3, 1994, the contents of which are incorporated herein by reference.

Claims

1. A device for controlling the timing at a receiving station for the receipt of asynchronous data transmitted with a time-stamp comprising:

a buffer through which the received asynchronous data is passed;

a decoder for generating an indication of the buffer fill level;

a local time-stamp generator at the receiving station for providing locally generated time-stamps; and

a circuit for controlling output timing for the buffer, said circuit being responsive to both a difference value of received and locally generated time-stamps and to an indication of fill level from said decoder.

2. A device as claimed in claim 1 wherein said fill level indication is proportional to the difference between the fill level of the buffer and a selected optimum fill level.

3. A device as claimed in claim 2 wherein the difference between current and optimum fill level is modified by a selected centering error gain to generate the fill level indication.

4. A device as claimed in claim 2 wherein said circuit includes means for generating a first difference between the time-stamp for the asynchronous data being received and the time-stamp for the most recent prior received asynchronous data, for generating a second difference between the locally generated time-stamp currently being generated and a previously generated local time-stamp, and for generating a third difference which is the difference between the first and second differences.

5. A device as claimed in claim 1 wherein the buffer is a FIFO buffer.

6. A device as claimed in claim 1 wherein the circuit includes a phase locked loop (PLL).

7. A device as claimed in claim 6 wherein an output from said PLL is obtained from a numerically controlled oscillator, a control input to the oscillator being a function of the time-stamp difference values and the fill level indication.

8. A device as claimed in claim 7 including means for indicating that a time-stamp is missing, and means responsive to said means for indicating for controlling the oscillator to move toward a selected nominal value, thereby preventing walking of the oscillator.

9. A device as claimed in claim 1 wherein said data is received in asynchronous packets, each of which packets includes a time-stamp, and wherein said buffer smooths out the received packets.

10. A method for controlling timing at a receiving station for the receipt of asynchronous data transmitted with a time-stamp comprising the steps of:

(a) passing the received data through a buffer;

(b) generating an indication of fill level for the buffer;

(c) generating a local time-stamp at the receiving station; and

remainder of the receiving station to smooth the received data. Optimally, this buffer is maintained at a selected fill level, for example approximately half full, so as to be able to continuously output at a lower speed the high speed asynchronously received input packets without loss of data due to buffer underflow or overflow.

One potential problem is that time-stamps may be missing for some reason, causing the buffer to "walk" (i.e., the buffer will either become overfilled or will empty preventing the smooth flow of data into the receiving station). This can cause aberrations in the received data and could result in received data being lost. A time-stamp may be missing from received data either because the time-stamp for some reason did not get added to the data at the transmitting station, the time-stamp somehow got lost in the transmission, the time-stamp was missed at the receiving station, or one or more data packets are not received at the receiving station. In any of these events, it is desirable that appropriate remedial action be taken at the receiving station to maintain an acceptable fill level in the buffer and to maintain an acceptable output rate for data from the buffer into the remainder of the receiving station.

SUMMARY OF THE INVENTION

In accordance with the above, this invention provides a method and apparatus for controlling the timing at a receiving station for the receipt of asynchronous data transmitted with a time-stamp. The received data is passed through a buffer to the remainder of the station. A decoder or other suitable means at the receiving station generates an indication of the buffer fill level, and a local time-stamp is also generated. The output timing for the buffer is controlled by a circuit or other suitable means which is responsive to both a difference value of received and locally generated time-stamps and to a fill level indication related to the buffer fill level. The fill level indication is preferably proportional to the difference between the current fill level of the buffer and a selected optimum fill level, for example roughly half full. This difference between current and optimum fill level may be modified by a selected centering error gain to generate a final error or fill level indication. The centering error gain can control the selection of optimum fill level and the effect of deviations from this optimum fill level on buffer output rate. The difference value may be obtained by generating a first difference between the currently received time-stamp and the last received time-stamp, a second difference between the current locally generated time-stamp and a previously generated local time-stamp, and generating a third difference which is the difference between the first and second differences.

The buffer is preferably a FIFO buffer and the control of output timing for the buffer is preferably done by a phase locked loop (PLL). For a preferred embodiment, the output from the PLL is obtained from a numerically controlled oscillator. The control input to the oscillator is preferably obtained from a phase detector which compares the received time-stamp error term-and current buffer fill indication as one set of inputs and the locally generated time-stamp and optimum buffer fill level as the other set of inputs.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention as illustrated in the accompanying drawings.

IN THE DRAWINGS

FIG. 1 is a schematic block diagram of a system in which the teachings of this invention may be utilized.

FIG. 2 is a schematic block diagram of a circuit for controlling timing at a receiving station in accordance with the teaching of this invention.

FIG. 3 is a schematic block diagram of a phased locked loop circuit suitable for use as the PLL circuit in FIG. 2.

DETAILED DESCRIPTION

Referring first to FIG. 1, an illustrative system 10 is shown which includes remote stations 12A and 12B, each of which may either transmit or receive data, with a transmission network 14 interconnecting the remote stations. Transmission network 14 may, for example, be a telephone network and, as described in much greater detail in the parent application, there may be a large number of control units, end offices, central offices and the like between a given pair of stations 12, which stations may be located thousands of miles apart. However, the invention is not limited to telephony systems and might also be employed with other types of communications networks, such as cable networks, for connecting remote IO stations or terminals.

For networks providing constant bit rate services to its users, information, "bits", can not be long stored or borrowed. The frequency information that leaves a network element at a receiving or destination station must be made exactly equal to the frequency which the information entered the network element at the source or transmitting station. As indicated earlier, modern telecommunications networks often provide a network timing reference which can be used to derive internal reference signals. However, not all signals that enter the network are derived from this system timing reference. When the source and destination network elements share a common network clock, it is customary for a time-stemp to be included with the data, such time-stamp being an indication of the frequency difference (error) between the incoming signal from the source station and the network timing reference. For systems operating in ATM, such time-stamps may be generated in accordance with Bellcore specification TA-NWT-00113, the time-stamp in such case being referred to as the synchronous residual time-stamp (SRTS). However, for simplicity in the following discussion, the time-stamp will be referred to either as "time-stamp" or the letters "TS" may be utilized.

FIG. 2 is a block diagram of a circuit 16 which may be used at each station 12 for retrieving and utilizing the time-stamp on asynchronously received packeted data such as that provided for ATM operation. Data received on the station's input lines 18, which may for example be byte parallel, are stored in a FIFO memory buffer 20. Buffer 20 is intended to match (rate de-couple) the high speed received data coming in on lines 18 with a continuous lower speed demand for data on output lines 22 from circuit 16 which lines lead into utilization equipment at station 12. Such equipment may, for example, include video displays, a smooth flow of data into the display device being desirable to prevent aberrations from appearing in the display. In order for the FIFO buffer 20 to operate properly, the buffer should never be empty so that it has no data to provide to its utilization device, and the buffer should never be full so that incoming data can not be stored, which could result in the loss of data. Therefore, in most situations, it is desirable that the buffer be maintained roughly half full, although the optimum fill level for the buffer will vary with application, and can be programmed for a given application.

Input lines 18 are also applied to a time-stamp detect circuit 24. Time-stamps may be detected by looking for time-stamp bits at selected locations in each packet of data, or by other techniques known in the art. When a time-stamp is detected in the input, it is applied as one input to a subtractor 26, the other input to which is obtained from a register or other suitable storage device 28 in which the last received time-stamp is stored. Once the differencing operation in subtractor 26 has been completed, the new time-stamp detected by circuit 24 is stored in store 28.

The output from subtractor 26 is applied as one input to subtractor or difference circuit 30. The other input to circuit 30 is the output from subtractor or difference circuit 32. One input to circuit 32 is the local time-stamp being generated at the receiving station 12. The circuitry 34 for generating such a time-stamp, which may be hardware, software, or a combination thereof, is known in the art and, as indicated earlier, is a function of the difference between the local clock and a standard system clock. The other input to circuit 32 is the output from last local TS store 36, which is a register or other suitable store for the local time-stamp which was generated during the preceding time step interval. Once circuit 32 generates an output, the new local time-stamp generated by circuit 34 is transferred into and stored in store 36. Thus, while the output on line 27 from circuit 26 represents the frequency difference due to originating station or source timing variations, the output from circuit 32 on line 31 represents a frequency difference due to local timing variations at the receiving station. The output

from difference circuit 30 is connected as one input to summing circuit 38. A fill level decoder 40 is provided which generates an output indicative of a fill level in FIFO 20. The magnitude of the output from decoder 40 is modified by a centering error gain circuit 42, the output from which is applied as the other input to summing circuit 38. The function of circuit 42 will be described later.

Circuits 26, 30, 32 and 38 form a phase detector 50, with the output from summing circuit 38 on line 43 is an error signal which is applied to phase lock loop (PLL) 44. The output from PLL 44 is utilized to control or clock the reading out of data by readout control 46 from FIFO 20. In particular, referring to FIG. 3, the error output on line 43 from phase detector 50 is connected through a filter 52, which circuit is optional, for reasons to be discussed later, to the numerical control input of a numerically controlled oscillator (NCO) 54. The output from oscillator 54 is connected as a clocking input to read out control 46 and is also fed back through a divide-by-N circuit 56 to phase detector 50 such that the PLL is closed through the locally generated time-stamp. The locally generated time-stamp causes the PLL to look for a new received time-stamp in detector 24, this detector including a small FIFO. This accommodates variations in,the received time-step arrival. In normal operation, there is a one-to-one correspondence between received and locally generated time steps. As will be discussed later, should there be no new time-stamp when the PLL expects one (i.e.,FIFO empty), then that condition forces the NCO toward its nominal value (i.e., 24.704 MHZ/16). Finally, line 62, which has a signal on it when a time-stamp has not been detected for a given clock interval, is connected as a input to NCO 54.

For a preferred embodiment the output timing is obtained by first dividing a 24.704 MHZ oscillator signal applied to the NCO on line 55 by a value M (M being 15, 16, or 17 for the preferred embodiment) and dividing that result by N. 24.704 MHZ/M represents a single output clock cycle and 24.704 MHZ/M/N represents the number of output clock cycles between 2 time-stamps (i.e., 3008 clock cycles). Frequency adjustment is obtained by selecting, at more or less evenly spaced intervals, occurrences when M is changed from its nominal value of 16, to 15 in the case where data must be read out of the FIFO faster or to 17 where data must be read out of the FIFO slower. The number of occurrences where M is changed in one time-stamp interval is constrained between +10 and -9. This number is contained in an NCO accumulator register 60, with M being 17 for the indicated number of occurrences when a plus number is in register 60, M being 15 for the indicated number of occurrences when a negative number is in the register, and M always being 16 when the value in register 60 is zero. The NCO accumulator register is compared with the new error term as modified by filter 52, (i.e., the signal on line 59) and the result is reintroduced into accumulator register 60.

In operation, for the preferred embodiment shown in the figures, a complete time-stamp should be received and detected at circuit 24 after each 3008 clock cycles. At the same time that the time-stamp is being received and stored at detect circuit 24, a local time-stamp is also being generated by circuit 34. The newly received time-stamp is compared in circuit 26 against the last time-stamp which was received and the newly generated local time-stamp is compared in circuit 32 against the last local time-stamp which was generated. The difference outputs as a result of the comparisons in circuits 26 and 32 are applied to circuit 30, with the difference output from circuit 30 being the time-stamp error output for the given time interval.

This error signal is applied as one input to summing circuit 38. The coded FIFO fill level from circuit 40 is modified by centering error gain circuit 42 to form the other input to this summing circuit. The function of circuit 42 is to control how much the centering error influences the FIFO read out rate. For a preferred embodiment, it is desired that the read out rate be primarily controlled by the time-stamp error, and circuit 42 therefore attenuates the output from decoder 40, However, the gain characteristic of circuit 42 may vary with application to achieve any desired objective with respect to fill level for FIFO 20 and the PLL characteristics. For example, the circuit could assure that the FIFO will never become empty or full by amplifying the outputs when the FIFO approaches either of these conditions to make this the controlling factor in determining the readout rate from the FIFO. Further, the gain characteristic in circuit 42 can also permit any selected fill level in the FIFO to be the desired level for which no output is generated by circuit 42, with positive levels being generated above this value and negative values below.

The error signal on line 43 is applied to PLL 44. The resulting error signal is preferably filtered by filter 52 to slow down the response of oscillator 54 to input changes. This makes the output clock as smooth as possible, rendering the circuit less responsive to jitter or other noise introduced into the signal at the sending station in the transmission network or at the receiving station. The filtered error signal is then applied to NCO 54 to control the number stored in register 60, and thus the average read-out rate from the FIFO during its succeeding time stamp interval.

As discussed earlier, one potential problem with synchronizing on time-stamps is that a time-stamp may be lost for a variety of reasons, including the fact that a time-stamp was not provided on the data initially, the time-stamp was lost in transmission, detector 24 failed to detect a time-stamp on the data, or data itself is missing. The cumulative effect of such missing time-stamps can cause the FIFO buffer to walk, and may result in the buffer becoming empty or full. This problem is corrected by comparing the actual FIFO fill level to some threshold fill level. It is often desirable to force the output clock frequence toward its nominal frequency level, for example to facilitate PLL lock and capture characteristics, or to employ the nominal frequency as a source for alarm indication signal, (AIS). (AIS signals for the preferred embodiment must be held within 32 PPM). When a new time-stamp is not detected at the time a new local TS is generated, line 62 directs the NCO accumulator to increment or decrement toward O resulting a move toward nominal frequency from the NCO. In particular, if the count in register 60 is positive, the count is decremented by one count, while if the count in register 60 is negative, it is incremented by one count. Thus, in the absence of a time-stamp, the output clock frequency moves towards the nominal 1.544 MHz which is the output frequency of the NCO when the count in register 60 is zero.

The signal on line 62 may be derived in a variety of ways. For example, TS detector 24 may generate an output when a complete time-stamp is assembled therein. The absence of this output could produce the signal on line 62. Station 12 could also have circuitry for detecting a missing time-stamp or a missing data packet, with the output from these various detectors being ORed to provide the signal on line 62.

While the invention has been described above with reference to a preferred embodiment, it is apparent that the circuitry described is for purposes of illustration only and that other suitable circuitry for performing the various functions could be utilized. In particular, while special purpose circuitry is shown for performing various functions, a special purpose or programmed general purpose processor could be utilized to perform various ones of the function, or the functions could be performed by some combination of hardware and software.

Thus, while the invention has been particularly shown and described above with respect to a preferred embodiment, the foregoing other changes in form and detail may be made therein by one skilled in the art without departing from the spirit and scope of the invention.

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United States Patent **5,325,270**
Wenger , et al. **June 28, 1994**

Modular backplane

Abstract

A flexible backplane assembly is provided wherein removable backplane modules are mounted in a platform in a manner such that the backplane modules may be removed and replaced to accommodate different types of circuit modules. Coacting guides are provided on the platform and the backplane modules to define a travel path for module insertion and removal which prevents contact with adjacent circuit and backplane modules and maneuvers around platform structural members. Connectors at the rear of each backplane module for mating withy circuit module connectors may be electrically connected to I/O boards at the front of the module to permit wiring of the backplane modules from the front of the platform.

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Claims

1. A platform for mounting a plurality of replaceable circuit modules, each having at least one circuit connector extending from the rear thereof, the platform comprising:

at least one replaceable backplane module, said backplane module having a plurality of sliders, at least one backplane connector which is matable with the circuit connector, and means for making electrical connections to said at least one backplane connector; and

rails positioned on opposite sides of each replaceable backplane module in which rails said sliders ride during at least a portion of a travel path for the backplane module during insertion and removal thereof.

2. A platform as claimed in claim 1 wherein said platform has a plurality of replaceable backplane modules.

3. A platform as claimed in claim 2 wherein each of said circuit modules has two circuit connectors, wherein each replaceable backplane module has one backplane connector for mating with one of the circuit connectors of a corresponding circuit module, and wherein said platform includes an additional, non-replaceable backplane connector for each circuit module positioned to mate with the other circuit connector when the circuit module is properly positioned in the platform.

4. A platform as claimed in claim 1 wherein each backplane connector is toward the rear of the platform when the circuit module is positioned in the platform, and wherein each backplane module includes means for making electrical connection to each said backplane connector from the front of the platform.

5. A platform as claimed in claim 4 wherein said means for making electrical connection includes an I/O board mounted to the front of each backplane module, and electrical conductors interconnecting the I/O board and said at least one backplane connector.

6. A platform as claimed in claim 1 including at least one first alignment element on each backplane module, and at least one second alignment element on the platform which mates with a corresponding said first alignment element when the backplane module is properly positioned in the platform.

7. A platform as claimed in claim 6 wherein one of said first and second alignment elements is a pin and the other of said alignment elements is a mating hole.

8. A platform as claimed in claim 1 including means for releasably fastening the backplane module to the platform when the backplane module is properly positioned therein.

9. A platform as claimed in claim 1 including a cage assembly for mechanically supporting each circuit module in the platform, said rails being positioned below said cage assembly.

10. A platform as claimed in claim 9 wherein said backplane module has a main section with an end section containing said backplane connector extending at a generally right angle from the back end of said main section, and wherein there is at least one slider on either side of said main section and at least one slider on either side of said end section.

11. A platform as claimed in claim 10 wherein both slider on each side of the module ride in a corresponding said rail during a forward portion of the backplane module travel path, and including an opening in a rear portion of each rail through which said end section sliders may project when such sliders are in said rear portion.

12. A platform as claimed in claim 11 wherein said main section is substantially parallel to said rails when the backplane module is properly positioned, the backplane module being pivotable to so orient the main section during module insertion when the end section slider is in said rear portion, the backplane module when rotated being forward of its proper position in the platform, continued rearward movement of the main section sliders in the rails permitting mating of the first and second alignment elements to properly position the backplane module in the platform.

13. A platform as claimed in claim 10 wherein each backplane module also has an end section

extending at a generally right angle from the front end thereof, the front end section extending in the opposite direction from the rear end section, an I/O board mounted to each front end section, and electrical conductors interconnecting the I/O board and a backplane connector of the backplane module.

14. A platform as claimed in claim 1 wherein each backplane module includes a runner assembly for mechanically guiding and supporting a said circuit module.

15. A platform as claimed in claim 1 wherein each backplane module includes a main section with an end section containing said backplane connector extending at a generally right angle from the back end of said main section, and wherein there are at least a forward and a rear slider on either side of said main section.

16. A platform as claimed in claim 15 wherein the forward one of said sliders on each side of said main section rides in a corresponding rail to a predetermined position on the rail, with the back-end section above the proper position, the back-end section being pivotable downward about the forward sliders when at said predetermined position until the rear slider on each side is positioned on a corresponding rail, both sliders on either side of the main section riding in a corresponding rail as the backplane is moved rearward during backplane module insertion until the first and second alignment elements mate to properly position the backplane module in the platform.

17. A platform as claimed in claim 15 wherein each backplane module also has a section extending at a substantially right angle from a forward position on the main section, the forward section extending in the opposite direction from the end section, an I/O board being mounted to each forward section, and electrical conductors interconnecting the I/O board and a second connector of the backplane module.

18. A platform for mounting a plurality of replaceable circuit modules, each having at least one circuit connector extending from the rear thereof, the platform comprising:

at least one replaceable backplane module, said backplane module having guide means, at least one backplane connector which is matable with a said circuit connector, and means for making electrical connection to said at least one backplane connector; and

means for coacting with the guide means to control a travel path for the replaceable backplane module during insertion and removal thereof.

19. A platform as claimed in claim 18 wherein said travel path includes at least two path segments, a pivot segment during which the module is pivoted at a pivot position between the module orientation when in its fully inserted position and an angled orientation for facilitating insertion and removal of the backplane module with respect to the platform, and a lateral segment performed with the backplane module generally in the angled orientation during which the backplane module is moved between a forward end of the platform and the pivot position, said means for coacting controlling movement of the backplane module during both path segments.

20. A platform as claimed in claim 19 wherein said travel path includes a second lateral segment during which the module is oriented in its fully inserted orientation and is moved laterally to or from a fully inserted position, said means for coacting controlling movement of the backplane module during all three segments.

21. A backplane module which may be removably mounted in a platform having backplane guide means and which may when mounted in the platform support at least one removable circuit module having a circuit connector, the backplane module comprising:

a module body;

a backplane connector, matable with the circuit connector, mounted to a rear portion of the module

body;

guide means on said module body for interfacing with the platform guide means to define a travel path for the backplane module during insertion and removal of the module;

means for making electrical connection to the backplane connector, and

wherein said means for making electrical connection includes an I/O board mounted to a front portion of said module body, and electrical conductors interconnecting said I/O board and said backplane connector.

22. A backplane module as claimed in claim 21 wherein said platform has first alignment means, and wherein said module includes second alignment means for coacting with the first alignment means to properly align the module in the platform.

23. A backplane module as claimed in claim 21 wherein the platform guide means are rails, and wherein the module guide means are sliders which are adapted to selectively ride in said rails during at least selected portions of said travel path.

24. A backplane module as claimed in claim 21 wherein said module body has a main section, a rear section extending at a generally right angle in a first direction from the rear of said main section, the backplane connector being mounted on said rear-end section, and a forward section extending at a generally right angle from a forward portion of said main section, the I/O board being mounted to said forward section.

25. A method for permitting replaceable backplane modules to be maneuvered around platform structural elements during insertion and removal of the modules in the platform comprising the steps of:

(a) pivoting the module at a pivot position, rearward of a point where the module would contact said platform structural elements if the module were in its fully inserted orientation, between said fully inserted orientation and an angled orientation where the module will not contact said structural elements when moved forward of the pivot point; and

(b) guiding the module through a lateral section of its travel path with the module generally in the angled orientation, the second lateral section being between the pivot point and the forward end of the platform;

steps (a) and (b) being performed in that order for removal of a backplane module from the platform and in reverse order for the insertion of a module into the platform.

26. A method as claimed in claim 25 including the step of:

(c) guiding the module through a second lateral section of its a travel path with the module oriented in its fully inserted orientation, the second lateral section being between a fully inserted position for the module and said pivot position;

steps (c), (a) and (b) being performed in that order for removal of a backplane module and in reverse order for insertion.

Description

FIELD OF THE INVENTION

This invention relates to electrical backplanes used for connection to electronic circuit modules and more particularly to such backplanes which may have their configuration easily altered for use with

different types or classes of circuit modules.

BACKGROUND OF THE INVENTION

Electronic backplanes are utilized in circuit platforms for telephony, computer and other electronic systems to permit various circuit boards, cards or other circuit modules to be interconnected or to be connected to external circuitry. In the following, a circuit platform or platforms will be considered to be a backplane and associated card cage or other circuit module support elements. In some instances, the term may also encompass the circuit modules mounted in the support. A platform may accommodate a varying number of circuit modules depending on application.

Typically, such backplanes have one or more connectors for each circuit module, each connector having a plurality of terminals which on one side mate with matching terminals on the corresponding circuit board and which are hard-wired on the other side to terminals in the backplane or through other connectors to external circuitry. Multiple connectors may be provided for each circuit module. A runner in the platform facilitates insertion and removal of the circuit modules, the connector(s) of the circuit module mating with the backplane connector(s) when the circuit module is fully inserted.

Platforms of this type are useful for permitting circuit modules of a particular type to be easily removed and replaced for preventive maintenance, to replace a defective circuit module, or to replace an existing module with an updated or improved module. However, such backplane platforms offer little flexibility where it is desired or required to use circuit modules of different types, having circuitry interconnects which are sufficiently different so as to require different connectors and different wiring on the backplane. In particular, where the circuit modules are switching circuits which are part of a central office telephone switching system, the I/O connections for the circuits may use T1 cable with 56 connections per cable and two cables per module, each cable being formed of twisted pair 22 gauge wire, may use DS3 signal cables which involve six coaxial cables per module, may utilize fiber optic cables with, for example, six fiber optic cables per module, or may utilize some other type of connector and wiring. Further, it may be desired, to have mixed circuit modules on a single platform, with some modules being of one type and some of another type.

In any event, when changes are to be made, it is preferable that it be possible to effect such changes on line without causing an interruption in service for other modules on the same platform. However, it is very difficult to change the backplane wiring for a hard-wired backplane because of space limitations in both the front and the rear of the platform, and it is virtually impossible to change to a different type of I/O connector. Performing such backplane rewiring in the field without interrupting service on adjacent circuits is also very difficult, but is desirable since any contact with adjacent circuits could cause failures in such circuits and might also result in shock, burns or other injuries to a person doing such replacement.

Heretofore, the difficulty of running new cables of a different type into a backplane once the backplane has been installed has been dealt with in some instances by running cables of different types into the backplane, connecting the cables to be utilized, and tying off the remaining cables until such time as their use may be required. However, this procedure only partially simplifies the field replacement problem and results in a significantly more expensive and time-consuming initial installation, both in terms of labor and materials. Further, too many unterminated lines in a backplane may degrade signals and thus performance. There are also space limitations in a backplane which may make installation of extra cables difficult and complicate working on the backplane with the extra cables. Finally, since platforms may be used for many years, frequently in excess of ten years, desired cables, for example fiber optic cable, may not have existed at the time the backplane was installed.

A need, therefore, exists for a more flexible backplane system which permits connectors to be easily replaced in the field to accommodate different types of circuit modules, and which permits any rewiring to be done from the front of the platform where wires can be gotten at easily and without danger of damaging adjacent circuits or of injury to a person doing the installation. Such a technique should permit the path for any replaceable backplane elements or modules to be carefully controlled

so as not to cause damage to adjacent circuit modules which are in use, while assuring that replacement components maneuver around structural portions of the platform and that replacement backplane modules are accurately positioned when fully installed.

SUMMARY OF THE INVENTION

In accordance with the above, it is an object of this invention to provide a flexible backplane system which permits at least selected backplane modules to be replaced so as to permit circuit modules with different types of connectors and/or wiring to be utilized with the backplane. Another object of the invention is to permit such replacement to be made without interrupting operation of other backplane and circuit modules in the same platform and, more specifically, without causing contact with such circuit modules or backplane modules. A more specific object of the invention is to permit rewiring of backplane modules to be accomplished in at least some embodiments without requiring access to the rear of the module and without the necessity for running extra wiring into the backplane during initial installation.

In accordance with the above and other objects, this invention provides a platform for mounting circuit modules having at least one circuit connector extending from the rear thereof, which platform has at least one replaceable backplane module. The module may include guide means such as a plurality of sliders on either side of the module, one or more alignment elements, at least one connector which is matable with the circuit module connector and some means for making electrical connection to the backplane module connector. The platform also contains a means which coacts with the guide or sliders on the backplane module to control a travel path for the replaceable backplane module during insertion and removal thereof. More specifically, at least two rails may be provided, which rails are positioned on opposite sides of each replaceable backplane module. The sliders ride in the rails for at least a portion of the travel path for the backplane module during insertion and removal. The platform may also contain at least one alignment element which mates with a corresponding alignment element on the backplane module when the module is properly positioned in the platform.

For some embodiments, each circuit module has two connectors and each replaceable backplane module has one connector for mating with one of the circuit module connectors, the platform including an additional non-replaceable second connector for each circuit module positioned to mate with the other circuit module connector when the circuit module is properly positioned in the platform. The backplane platform connector is preferably toward the rear of the backplane module and an I/O board or other means is preferably mounted to the front of each backplane module for making electrical connection to the backplane module connector from the front of the module.

Alignment between a backplane module and the platform is preferably provided by having a pin on one such element with a mating hole on the other element, the pin and hole fully mating when the backplane module is properly positioned in the platform. For a preferred embodiment, there are a pair of mating alignment elements on the platform and backplane module, and a means is provided for releasably fastening the backplane module to the platform when the backplane module is properly positioned therein.

For various embodiments of the invention, the travel path for a backplane module during insertion and removal includes at least two path segments. One segment is a lateral segment during which the module is oriented in its fully inserted orientation and is moved laterally to or from a fully inserted position. The second path segment is a pivot segment during which the module is pivoted to or from the lateral segment orientation to an angled orientation for facilitating insertion and removal of the backplane module with respect to the platform. A second lateral path segment may also be provided which is performed with the backplane module generally in the angled orientation. During this second lateral segment, the backplane module is moved between a forward end of the platform and a pivot position where the pivot segment is performed. Various guide elements, such as rails and sliders, coact during the various path segments to control and limit movement of the backplane to the selected travel path, assuring that undesired contact is not made with adjacent modules which may be active and that the backplane module is guided around various structural members of the platform.

More specifically, for one embodiment, the platform includes runners for mechanically supporting each circuit module in the platform with the rails for each backplane module being positioned below the runners for the corresponding circuit module, facilitating insertion and removal of a backplane module from below platform structural members.

The backplane module preferably has a main section with an end section containing the backplane connector extending at a generally right angle from the back end thereof. For this embodiment, there is at least one slider on either side of the main section and on either side of the end section. Both sets of sliders may ride in corresponding rails during the second lateral section of the travel path with an opening being provided in a rear portion of each rail through which the end section slider may pass during the pivot section of the travel path. Each backplane module for this embodiment preferably has an end section extending at a generally right angle from the front end thereof, the front end section extending in the opposite direction from the rear end section and having an I/O board mounted thereto. Electrical conductors are provided for interconnecting the I/O board and the backplane module connector. External circuit connections may be made to the I/O board, the board being at the front of the platform when the backplane module is properly positioned and thus easily reached.

For another embodiment, the runners for mechanically guiding and supporting circuit modules may be on the backplane module Each backplane module also has a main section, the runners being attached to this section, and a connector-containing end section extending at a right angle from the back end of the main section. At least a forward and a rear slider are provided on either side of the main section. For this embodiment, the backplane module is initially oriented during insertion with the back end section elevated above its proper position and the forward slider on each side of the main section in a rail. The backplane module is moved in this general orientation through the second lateral segment of its travel path until the pivot point in the travel path is reached, at which point the lateral position of the module is preferably temporarily locked and the rear end of the backplane module is lowered by being pivoted about the forward sliders until a desired final orientation for the backplane module is reached. At this point, the rear slider on each module engages a corresponding rail. The backplane module is then moved into its final position through the first segment of its travel path with all of the sliders riding in corresponding rails. The procedure described above is reversed for backplane module removal. This module also preferably has a downwardly-extending forward section with an I/O board electrically coupled to the backplane module connector.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention as illustrated in the accompanying drawings.

IN THE DRAWINGS

FIG. 1 is a front elevation view of a portion of a platform in accordance with a first embodiment of the invention.

FIGS. 2A-2C are partially broken away side elevation views taken generally along the line 2--2 in FIG. 1 illustrating various stages in the insertion of a backplane module for this embodiment.

FIG. 3 is a front-top perspective view of a portion of a platform for an alternative embodiment of the invention.

FIG. 4 is a front elevation view of the platform portion shown in FIG. 3.

FIGS. 5A-5D are partially broken away side elevation views taken generally along the line 5--5 in FIG. 4 at various stages of insertion for a backplane module.

DETAILED DESCRIPTION

The various embodiments of this invention relate to an electronic circuit platform 10 which may have a plurality of circuit boards or other circuit modules 12 mounted therein. In addition to having electronic circuitry for switching or other purposes, each circuit module 12 has an upper connector 14U and a lower connector 14L extending from its rear surface, and has upper and lower guides 16U and 16L, respectively, which are adapted to ride in corresponding runners 18U,18L (only the lower ones 18L of which are shown) Of the platform to physically support circuit module 12 in the platform.

Platform 10 has two connectors 20U and 20L for each circuit board module. For the preferred embodiments shown in the figures, upper connectors 20U may be hard-wired as part of the backplane and may be utilized for interconnecting circuit modules in the platform. Changes in external wiring therefore do not affect these connectors. In accordance with the teachings of this invention, lower connectors 20L are part of a removable backplane module 22, which modules are somewhat different for the two embodiments of the invention. The lower connectors interface with external circuits and are therefore the I/O connectors for the circuit module. These are the connectors which need to be changed for different types of circuit modules.

Referring first to the embodiment of the invention shown in FIGS. 1 and 2A-2C, each backplane module 22 has a center section 24, a front end section 26, and a rear end section 28. End sections 26 and 28 each project at a right angle from center section 24 with section 26 projecting downward and section 28 projecting upward. A connector 20L is mounted in rear section 28 of the backplane module for each circuit module to be serviced by the backplane module and an I/O board 30, having a plurality of connector pins 32 extending therefrom, is mounted to the forward section 26. Connector 20L and I/O board 30 are interconnected by electrical cable 34. Where, as shown in the figures, each backplane module supports two circuit modules, I/O board 30 may have two sections and a separate cable 34 may be provided to connect each section of the I/O board to the corresponding connector 20L.

A slider 36 extends from each side of backplane module 22 at approximately the junction of sections 24 and 26. Additional sliders 38 and 40 extend from each side of middle section 24 at points along this section and a slider 42 extends from each side of back section 28 at a point near the top thereof.

The sliders 36, 38, 40 and 42 on each side of backplane module 22 are adapted to ride in a corresponding rail 44 mounted to platform 10 on either side of the module. Each rail has a pair of openings 46 and 48 formed in its lower surface and an opening 49 formed in its upper surface near the rear thereof. The functions of these openings will be described later.

Each backplane module 22 also has a clip 50 attached to the top of center section 24 at roughly the midpoint thereof, the function of which will also be described later. At least one, and preferably two, alignment holes 52 are formed in the back of rear section 28 near the top thereof and a hole or holes 54 are provided near the bottom of board 30 through which a suitable platform fastener 56 may extend to secure backplane module 22 in platform 10. Where I/O board 30 is shorter than front section 26, hole 54 for fastener 56 will be provided in front section 26.

Platform 10 has runner 18L mounted to cage assembly 60. Cage assembly 60 includes hollow bars 62 and 64 which extend across platform 10 to support the cage assembly and which bars the backplane module 22 must be maneuvered past for insertion and removal. The rear of platform 10 includes a housing member 66 to which connectors 20U are mounted. There is a pin 68 extending from housing member 66 for each hole 52 in backplane module 22, a pin 68 and hole 52 mating to properly align the backplane module in the platform so that the connectors 14 of a circuit module will mate with the corresponding connectors 20 of the backplane. A bar 70 extends across the bottom of platform 10 with a hole 72 being provided in bar 70 for each fastener 56.

In operation, a backplane module is initially positioned in platform 10 by fitting the slider 42 on either side of the module into the front end of corresponding rails 44. The backplane module 22 is then moved backward, with sliders 42 riding in rails 44 and module 22 preferably oriented generally as shown in FIG. 2A until sliders 36 are adjacent to the front end of rails 44. The sliders 36 on each

side of module 22 are then fitted into the corresponding rails 44 and the rearward movement of module 22 is continued with both sliders 42 and 36 riding in rails 44 until the module reaches approximately the position shown in FIG. 2A. At this point, the module 22 has cleared both rails 62 and 64 and has completed an initial lateral segment of its travel path.

At this point, the module is pivoted upward about the sliders 36 in rails 44, with each slider 42 passing up through the corresponding opening 49 in the top of the rails. This pivoting continues with slider 38 passing into rail 44 through opening 46 and slider 40 passing into rail 44 through opening 48, until the module reaches the orientation shown in FIG. 2B. At this point, the backplane module has completed a second pivot segment of its travel path.

The final lateral segment of the backplane module's travel path involves moving the module laterally backward with sliders 36, 38 and 40 on each side of module 22 riding in the corresponding rail 44. As this rearward motion continues, the forward portion of clip 50 rides over a rear lip 70 of cage assembly 60 and the one or more openings 52 in the rear of backplane module 22 fit over the corresponding pins 68 to assure proper alignment of the backplane module in the platform.

When this lateral section of the travel path is completed, the backplane module is properly positioned in platform 10 in the position shown in FIG. 2C. At this point, fastener 56 is engaged with rail 70 of the platform housing through opening 72 to secure the backplane module in platform 10. The final step in providing a new backplane module in platform 10 is to attach suitable wiring to pins 32 of I/O board 30 for the circuit modules 12 to be used with the backplane module. While the I/O boards shown in the figures are for TI cable, backplanes for other types of wiring, such as coaxial cables terminated in multipin plugs or fiber optic cables, would have suitable I/O boards 30 with suitable connector elements in lieu of the pins 32. Connections made to I/O board 30 are electrically coupled to connector 20L through cable 34. Once a backplane module is fully installed, a circuit module 12 or circuit modules may be installed in the platform position(s) of the new backplane module.

When it is desired to remove a backplane module 22 so that it may be replaced with a new module, the sequence of operations described above is reversed. In particular, circuit modules 12 are removed, electrical connections to I/O board 30 are disconnected, fastener 56 is released and the I/O module is slid forward to the position shown in FIG. 2B. The backplane module then undergoes the pivot portion of its travel path with the platform being pivoted downward about the sliders 36 until the sliders 42 pass through hole 49 and engage the bottom of rail 44. At this point, the backplane module is in the position shown in FIG. 2A. The I/O module is then removed from the platform by sliding the module forward under rails 62 and 64 until first sliders 36 and then sliders 42 exit the forward end of rail 44. The platform is then ready to receive a new backplane module 22 for a new type of circuit module.

FIGS. 3, 4 and 5A-5D illustrate a second embodiment of the invention which differs from the embodiment described above in that the backplane modules 22' are lowered into platform 10 from above rather than being raised into the platform from below to maneuver around bars 62 and 64, and in that runners 18L are mounted on the backplane module rather than being part of the platform cage. In particular, module 22' has a main section 24, a front end section 26 and a rear end section 28 the same as for the earlier embodiment. Connectors 20L1 and 20L2 are mounted to a plate 80 attached to rear section 28, which plate also has alignment openings 82 formed therethrough for mating with alignment pins 68. I/O board 30 having connector pins 32 is mounted to forward section 26. Cabling 34 selectively interconnects connectors 20 and pins 32. Runners 18L1 and 18L2 are secured together by interconnect plates 84 with the rear two interconnect plates 84 being secured to a collar 86 which fits around and is secured to center section 24. An end bracket 88 is attached to and extends from the front underside of each runner 18, the bracket having a projection 89 extending down from its forward end. Each bracket 88 has a forward slider 90 and a rear slider 92 extending from each side thereof.

A forward rail assembly 94 is mounted to forward bar 62 of platform 10 and a rear rail assembly 96 is mounted atop rear bar 64. Rail assembly 94 has a track formed therein with a forward horizontal section 98 and a rear horizontal section 100 interconnected by a vertical section 102. As is discussed

in greater detail later a stop or detent may be provided at the junction of sections 100 and 102. Rail assembly 96 has a horizontal track 104 formed therein with an opening 106 formed in the top of the rail.

In operation, when a backplane module 22' is to be installed, the module is initially positioned and oriented generally as shown in FIG. 5A and sliders 90 on either side of the module are fitted in the front end of section 98 of the track in the corresponding rail assembly 94. The backplane module is then moved rearward with sliders 90 riding in track section 98, and with the backplane module oriented generally as shown in FIGS. 5A and/or 5B until the sliders 98 reach section 102 of the track. At this point, the sliders drop down in section 102 of the track so that the module 22' is generally in the position and orientation shown in FIG. 5B. This completes the initial lateral portion of the modules-travel path.

When the module is in the position shown in FIG. 5B, it is preferable that the sliders 90 be locked or detented in the position shown as the rear end of the module is pivoted downward about the sliders 90 until rear slider 92 passes through opening 106 in the top of track 104 and comes to rest in the track as shown in FIG. 5C. At this time, the module is oriented as shown in FIG. 5C. The locking or detenting of sliders 90 may be accomplished in a number of ways. For example, each slider may have an elliptical shape or may have a fin or other extension such that, with track section 98 being slightly wider than track section 100, the slider is too wide to fit in track section 100 when oriented as shown in FIG. 5B, but can fit into track section 100 when oriented as shown in FIG. 5C. Alternatively, a piece of spring material can extend across the forward end of track section 100, the forward section of this track may have an elastomer collar, or some other means may be provided, to inhibit entry of slider 90 into track section 100 as module 22' is being pivoted, but which can permit the slider to enter track section 100 when the module is oriented as shown in FIG. 5C and the module is pressed rearward with enough force to overcome the detent.

The final portion of the module travel path involves moving the module rearward, with slider 90 riding in track section 100 and slider 98 riding in track 104, until the pins 68 on housing plate 66 pass through holes 82 in connector support plate 80 to properly orient the module in its final position. This position is shown in FIG. 5D. While not shown for this embodiment of the invention, a fastener 56 could be provided to secure backplane module 22' to the platform in the same manner shown for the earlier embodiment, or other suitable means could be provided for performing this function. The final steps in the operation are to make electrical connections as appropriate to pins 32 of I/O board 30 and to insert appropriate circuit modules 12.

When it is desired to remove a backplane module so that different types of circuit boards may be used therewith, the process described above is reversed. In particular, any circuit modules in the backplane module are removed, electrical connections to I/O board 30 are removed, a fastener 56, if present, is opened and the module is moved forward, by for example hooking a finger under forward projection 89 at the end of bracket 88, to the position shown in FIG. 5C. The rear end of the module is then pivoted upward by, for example, pressing down on the forward end of bracket 88 until the module is in the position shown in FIG. 5B, and the module is then lifted slightly to move sliders 90 into-track section 98. Module 22' is then pulled forward until sliders 90 leave the forward end of the tracks. The platform is then ready to have another backplane module inserted therein, for example, for a different type of circuit module, in the manner described above.

A flexible backplane suitable for use with various types of circuit modules is thus provided where the travel path of each replaceable backplane module is fully controlled during insertion and removal to prevent any contact with adjacent circuit modules. Backplane modules may thus be replaced while adjacent circuits are in operation without risk of damage or injury. All wiring to the backplane modules may also be made from the front of the module, simplifying the procedures for rewiring a platform in the field and eliminating the need for running additional cables into the backplane to provide for future use of different circuit types.

While two different embodiments are shown in the drawings to illustrate controlled insertion and removal of backplane modules from either above or below structural support bars or other structural

elements of a platform, it is apparent that these embodiments are for purposes of illustration only, and that many variations in rail and slider configuration in particular, and in the guidance mechanism for the travel path of the backplane modules in general, are possible. For example, a greater or lesser number of guide rails could be provided which coact with appropriate sliders or other elements on the backplane module to control the module travel path; or guide grooves could be provided in the modules which coact with sliders or other elements on the platform to guide the travel path.

The alignment elements shown, the I/O boards utilized and the fasteners where employed are also for purposes of illustration and other suitable elements known in the art could be utilized for performing these functions. With suitable tolerances on the guides, the alignment elements might also be dispensed with.

In addition, while the travel path for the preferred embodiments to maneuver around platform structural members is in three sections, a first section to move past the structural members with the module in an angled orientation, a pivot section to bring the module to the desired orientation, and a final section to move the properly oriented module to its final position, with proper tolerances, it may be preferable to eliminate the final section of the travel path. In particular, for the embodiment shown in FIGS. 3, 4 and 5A-5D, the lock discussed above for the sliders 90 at the pivot point might be a precise lock so that, when the module 22' completes the pivot section of its travel path, it is in the final position shown in FIG. 5D. For this embodiment, alignment pins 68 would be eliminated and either the lock on slider 90 would be relied on for alignment or some other suitable alignment mechanism used.

While each backplane module has been illustrated as servicing two circuit modules for the illustrated embodiments, each backplane module may be designed to accomodate a selected one or more circuit modules. All or only selected ones of the backplanes in a given platform may be replacable. Also, while runners have been shown for the two embodiments as being placed either on the platform or on the replaceable backplane module, the runners may be positioned either way for various embodiments of the invention.

Further, while for the preferred embodiments shown in the drawings, each circuit board has two connectors with only one of the mating connectors on the backplane being replaced, the invention could be practiced with circuit boards having only a single connector, or replaceable backplane modules having two connectors could be used. In addition, while for most applications it is preferable to have I/O board 30 permitting electrical connections to be made from the front, in some applications, there may be sufficient space behind the backplane so that connections can be made from the rear. In such applications, I/O boards 30 may be eliminated and at least part of the portion 26 of the backplane module for supporting the I/O board may also be eliminated. Thus, while the invention has been particularly shown and described above with reference to preferred embodiments, the foregoing and other changes in form and detail may be made therein by one skilled in the art without departing from the spirit and scope of the invention.

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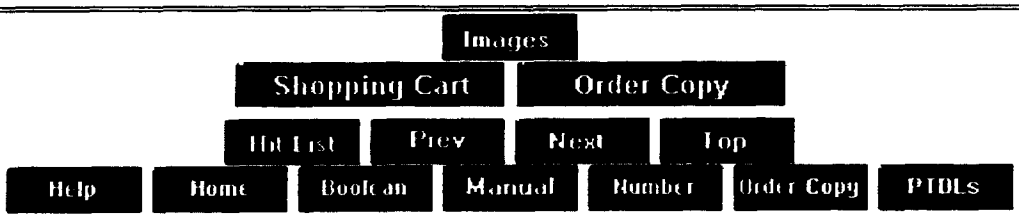

United States Patent **5,237,640**
Pedraza , et al. **August 17, 1993**

Guide for an optical fiber cable having minimum bend radius

Abstract

A cable guide assembly for use with a panel which has a plurality of adjacent mounted circuit members, such as panel mounted telephone switching circuits, with a plurality of fiber optic or other cable whose performance would be impaired if bent beyond a minimum bend radius extending therefrom. The guide assembly manages the running of the cable toward either end of the panel from each circuit member in a manner such that the cable cannot be bent beyond its minimum bend radius. In particular, an effective curve surface is provided at each point where the cable changes direction, with the cable passing over such surface and such surface having a radius which is not less than the minimum bend radius of the cable.

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Claims

1. A cable guide for use with a panel having a plurality of adjacent mounted circuit members, each of which has a plurality of cables extending therefrom in at least a first direction, said cables having a minimum bend radius below which performance of the cable may be impaired, the cable guide comprising:

means for mounting the cable guide to the panel on the first direction side of the circuit members;

a first guide for each circuit member, which guide is spaced from a point on the circuit member from which said cables extend; and

a second guide positioned on either side of each first guide, there thus being a second guide between each pair of adjacent first guides, each second guide being space from each adjacent first guide by a distance greater than the thickness of said cable, being closer to said circuit members than adjacent first guides, and having two sides, each of which extends from a point on the second guide adjacent the cable extension point of a circuit member toward the first guide for the adjacent circuit member at a curve having a radius not less than said minimum bend radius, the position of the first guide for the adjacent circuit member relative to the second guide being such that said first guide is generally an extension of said curve for cable being guided by the side.

2. A cable guide as claimed in claim 1 including means for retaining cable between the first guide for the circuit member from which the cable extends and a selected one of the adjacent second guides.

3. A cable guide as claimed in claim 2 wherein said means for retaining cable includes an enlarged end portion on at least one of the first guides and the second guides.

4. A cable guide as claimed in claim 3 wherein said enlarged end portions are enlarged heads on the ends of the first guides.

5. A cable guide as claimed in claim 1 wherein the depth of each first guide and each second guide are such that a plurality of cables may lay adjacent each other when passing thereover.

6. A cable guide as claimed in claim 5 wherein there are N cables extending from each of said circuit members, and wherein the depth of each guide is such that N cables may pass thereover.

7. A cable guide as claimed in claim 1 wherein each first guide is in the form of a substantially cylindrical dowel.

8. A cable guide as claimed in claim 1 wherein each second guide has a generally triangular cross section with the side adjacent the circuit members being of a selected shape and the other two sides having said curve.

9. A cable guide as claimed in claim 1 wherein said first and second guides extend from a wall of the cable guide, and including a shelf extending above and behind said wall, cable being positionable on said shelf after passing between a selected first guide and second guide, and wherein the corner at the junction of the wall and the shelf has a curve with a radius greater than said minimum bend radius.

10. A cable guide as claimed in claim 1 wherein said cables are fiber optic cables with a minimum bend radius of approximately one inch, and wherein said curve radius is approximately one inch.

One of the most likely locations for a break or other degradation in a fiber optic cable as a result of overbending is at the switching panels of a telephone central office. Typically, a large number of interconnect switching circuits or other types of circuits are mounted adjacent each other in a panel with cables extending from a selected side or sides of each of the circuits. In one application, there are six fiber optic cables extending from each circuit. Some of these cables maybe inputs and others outputs for the circuit and it is desirable that cables leaving a given circuit be able to extend toward either end of the panel to interconnect with other circuits on the panel or with circuits and locations external to the panel. However, to avoid undesirable signal degradations or breaks occurring in the cables, it is important in running the cables from the circuit board through the panel that the cables not be overbent at any point in their travel path. Existing systems for managing and controlling the running of fiber optic cables in a switching panel do not provide specific guides for assuring that cables are not overbent as they are run through the panel while allowing for multiple cables and multiple routing directions. Similar problems, also unresolved, may exist in various coaxial cable systems where characteristic impedance may be changed or wire or shielding cracked or broken if overbending occurs.

A need therefore exists for a cable guide for use with telephone central office switching panels and other circuit panels using fiber optic or other cables which may be damaged if overbent to manage and control the running of such cables in a manner so as to protect against overbending.

SUMMARY OF THE INVENTION

In accordance with the above, this invention provides a cable guide assembly for use with a panel which has a plurality of adjacent-mounted, possibly removable, circuit members, such as panel mounted telephone switching circuits, with a plurality of fiber optic cables or other cables whose performance would be impaired if bent beyond a minimum bend radius extending therefrom. The guide assembly manages and guides the running of the cable toward either end of the panel from each circuit member in a manner such that the cable cannot be bent beyond its minimum bend radius. Protection against costly and difficult to detect breaks or other degradations in performance in the cables is thus provided.

More particularly, the cable guide is mounted to the panel on the side or sides of the circuit members from which cables are extending. The cable guide has a first guide for each circuit member, which guide is spaced from a point on the circuit member from which cables extend. A second guide is positioned on either side of each first guide, there thus being a second guide between each pair of adjacent first guides. Each second guide is spaced from each adjacent first guide by a distance greater than the thickness of the cable and is closer to the circuit member than the adjacent first guide. Each second guide has two sides, each of which extends from a point on the second guide adjacent a cable extension point of a circuit member toward the first guide for the adjacent circuit member at a curve having a radius which is not less than the minimum bend radius for the cable. The position of the first guide for the adjacent circuit member relative to the second guide is such that the first guide is generally an extension of the curve of the second guide side for cable being guided by such side.

A means is also provided for retaining cable between the first guide for the circuit member from which cable extends and a selected one of the adjacent second guides. For a preferred embodiment, the means for retaining cable includes an enlarged end portion on at least one of the first guides and/or second guides. For the preferred embodiment, the enlarged end portions are enlarged heads on the ends of the first guides.

The depths of each first guide and each second guide are preferably such that a plurality of cables may lay adjacent each other when passing over the guides. In particular, where there are N cables extending from each circuit member, the depth of each guide should be such that the N cables may lay adjacent each other when passing over the guide.

For the preferred embodiment, each first guide is in the form of a substantially cylindrical dowel and each second guide has a generally triangular cross section with the side adjacent the circuit members being substantially flat or having some other selected shape, and the other two sides having the

indicated curve. The second guides at the ends of the cable guide preferably have a generally semicircular cross section with a radius greater than the minimum bend radius. A suitable means may be provided for retaining the cable on such end guides.

A shelf may be provided which extends above and behind a wall from which the first and second guides extend, cable being positionable on the shelf after passing between a selected first guide and second guide. The corner at the junction of the wall and the shelf preferably has a curve with a radius greater than the minimum bend radius. A ledge corner having substantially the same radius is provided above the point where cable exits the cable guide assembly at each end to limit the bend radius on upwardly exiting cables. For the preferred embodiment, where the cables are fiber optic cables, which cables may have their performance degraded or break if bent beyond a radius of approximately 1 inch, the curve radius for the second guide sides and for the shelf and ledge corners is preferably approximately one inch.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention as illustrated in the accompanying drawings.

In the Drawings

FIG. 1 is a partially broken front elevation view of a portion of a circuit panel having a cable guide for a preferred embodiment of this invention mounted thereto.

FIG. 2 is a top plan view of the cable guide shown in FIG. 1.

FIG. 3 is an enlarged front elevation view of a portion of the cable guide shown in FIG. 1.

FIG. 4 is a side elevation view of the cable guide shown in FIGS. 1 and 3.

FIG. 5 is a side sectional view taken along the line 5--5 in FIG. 3.

DETAILED DESCRIPTION

Referring to the figures, a panel 10 has the guide assembly 12 of this invention mounted on top thereof. Panel 10 has positions therein for a plurality of circuit elements 14A-14N, which elements may all be of the same size or may be of different sizes as shown in the figures. Panel 10 may, for example, be a telephone switching panel with each of the circuit elements 14 being a telephone switching circuit.

Each circuit element 14 has a plurality of fiber optic cables 16 extending from the top thereof, only a few exemplary ones of such cables being shown in the figures. Cables may also extend from the bottom of each circuit element. For one telephony application in which the invention may be utilized, there are six cables 16 extending from the top of each circuit 14. For purposes of this invention, cables 16 will be assumed to each be made of a plurality of optical fibers, which fibers are brittle and may crack or break, or may have their performance degraded as a result of defractions within the leads, if the cable is bent beyond some minimum bend radius. Such a crack, break or defraction could block or otherwise interfere with the proper flow of data through the cable. Since in many instances only some of the fibers in a cable would break for a given overbending, and since the cable may be covered, such a break may go undetected until there is a loss of information of erroneous information passed through the cable. At that point, it may be difficult to localize the break in the cable and replacing the cable, particularly if the cable has a long run, may be difficult and extensive.

It is, therefore, desirable to avoid overbending of the cable during the installation and wiring of a circuit element 14 and of the fiber optic cables connected thereto. In managing the running of cables 16 in a manner so as to prevent overbending, account must be taken of the fact that each cable 16 may need to run toward either end of the panel 10 from a given circuit element and that such output cables may connect either to other circuit elements 14 on the same panel 10 or to circuits or devices

external to panel 10.

Guide assembly 12 performs the function of guiding and managing the running of cables 16 so as to avoid overbending. While assembly 12 is shown mounted to the top of panel 10, where cable 16 exits from the bottom of at least some of the circuit elements 14, a guide assembly could also be mounted to the bottom of the panel.

Assembly 12 has a wall 18 with a plurality of first dowel-shaped guides 20A-20N and a plurality of second guides 22A-22N having a generally triangular cross section extending therefrom. Wall 18 terminates at each end in an end guide 24A, 24B. The upper corner 28 of wall 18 is curved for reasons to be discussed later with a curve having a radius of curvature R, where R is at least equal to the minimum curve radius for the fiber optic cables. Extending rearward from wall 18 at corner 20 is a generally horizontal shelf 30 having a rear wall 32 extending upward therefrom. A plurality of screw holes 34 are formed through shelf 30, each of which mates with a corresponding screw hole 36 in panel 12 (FIG. 5). A screw 38 passes through each hole 34 and corresponding hole 36 to hold guide assembly 12 in place on panel 10. Screws 38 are flush mounted with shelf 30 when the guide assembly and panel are fully screwed together. Suitable elements may be provided, if required, to further secure the guide assembly and panel together. The guide assembly and panel may also be molded or otherwise formed together, may be glued together, or may be held together in other suitable ways, either in addition to or instead of screws 38.

Each first guide 20 has an enlarged oval head 48 formed at its distal end. The spacing between each dowel 20 and the adjacent guide 22 at each point along such spacing is preferably at least twice the thickness of diameter of each cable 16 to allow removal of inner cables without removing outer adjacent cables. The spacing between each head 48 and the distal end of each adjacent guide 22 is slightly greater than the thickness of cable 16 at all points along such spacing. Each second guide 22 has a generally triangular cross section with the bottom of a second guide being substantially flat and the two side walls extending upward with a radius R' which is not less than (i.e. at least equal to) the minimum bend radius of the cable. For a preferred embodiment, the radius R and the radius R' are substantially the same. In particular, assuming the fiber optic cable utilized has a minimum bend radius of approximately one inch the radiuses R and R' would be approximately one inch for a preferred embodiment. However, the radiuses R and R' could be different so long as each of these radiuses is at least equal to the minimum bend radius for the particular cable being used.

Further, as may be best seen in FIGS. 1 and 3, the guide 20 on the side of a guide 22 to which cable 16 extends when passing over a given side of a guide 22 is generally positioned so as to form an extension at the radius R', or at another radius not less than the minimum bend radius, of the second guide side. Thus, cable 16C1 passes over the right side of guide 22C and over guide 20C, guide 20C forming an extension of the right side of guide 22C at the radius R'. As may be best seen in FIGS. 2 and 5, each guide 20 and 22 has a depth sufficient such that N cables may pass over the guide laying side-by-side of the preferred embodiment, where N is the number of cables exiting a given circuit element 14. This, if six cables (i.e. three input and three output cables) exit each given element 14, the length of each guide (i.e. the distance the guide extends from the wall 18) would be sufficient so that six cables could lay adjacent each other on each of the guides.

However, since there are many circuit members 14 in each panel, and the cables from each of these circuit members may extend in either direction for a substantial distance across the panel, there may not be enough space across the guides for cables to pass thereover. Shelf 30 is therefore provided on which cables may be moved after passing between the appropriate guides 20 and 22. As previously discussed, some of the cable may extend along guide assembly 12 to another circuit element on the panel, while other cables extend to the end of the panel to interconnect with other panels or circuitry. The latter cables are the ones most advantageously put on shelf 30.

Since cables exiting guide assembly 12 on either end, from either the end first guide 20A or 20N or from shelf 30, pass over the adjacent end guide 24A or 24B, these guides should also be radiused with a radius not less than the minimum bend radius in order to prevent excessive bending of the cable. An oval projection 50A, 50B is attached to project above the top surface of the distal end of

guides 24A and 24B, respectively, at substantially the highest point on such guides to keep cable passing over guides 24 from slipping off the ends thereof.

Where the enlarged end circuit elements 14A and 14N have cables extending from an additional point near the center thereof, rather than only from the right side, the end guides 24A and 24B may be segmented as shown in dashed lines in FIG. 1 to form a guide 20A', 20N' over such central exit point with a guide 22A', 22N' on either side thereof. The projections 50 could be mounted to the guide sections 20 or the heads 48 on these guides could be extended to perform the function of these projections. The segmenting of guides 24 would only extend to wall 18 and the segmented guides would still perform the same function described for these guides above.

In the figure, a ledge 54 is shown above the guides 20 and 22 and shelf 30, the ledge having rounded corners 56A, 56B at its ends, the radius for the rounded corners also being not less than the cable minimum bend radius. Corners 56A, 56B prevent overbending of cable exiting upward from the guide assembly. Corners 56A, 56B may substitute for guides 24A, 24B where cables 16 only exit assembly 12 upward. Ledge 54 may be present only on the end of the guide assembly 12 or may extend as shown over the entire guide assembly.

In operation, each first guide 20 is positioned over substantially the point of the corresponding circuit element 14 where cable 16 exits. Cable 16 exiting the circuit element may thus be run to either side of guide 20, running to the left side of guide 20 if the cable is to extend to the left and to the right side of guide 20 if cable is to run to the right. Each cable is manually or automatically run through the space between head 48 of the guide 20 and the guide 22 on the side of the guide 20 in which the cable is to extend. For the preferred embodiment, this space is greater than the diameter of the cable to avoid damage to the cable when being fitted therein. However, if this space is smaller to hold cable in place, and to the extent the cable is not elastic enough to be fit between head 48 and the adjacent guide 22 without damage to the cable, head 48 or the adjacent distal end of guide 22 may be formed of a slightly resilient material, or the guides may flex slightly with respect to rear wall 18, so that cable may be fit between an enlarged end portion or head 48 and the distal end of the adjacent guide 22 without damage to the cable.

Once fitted into the spacing on the proper side of the corresponding guide 20, the cable extends in the direction it is being run over the next adjacent guide 20, which, as previously indicated, is generally an extension of the radius of the side of guide 22 over which the cable is passed, and then continues in the direction it is being run either passing over the tops of successive guides 20 or being pushed back onto shelf 30. Since the cable is relatively compliant, it tends to straighten after being run so as to bear against guide 20 rather than 22 and to thus be behind head 48. This assures that the cable remains on the guides.

If the cable is to exit from the panel, the cable ultimately passes over the appropriate one of the guides 24 or corners 56 before exiting the guide assembly. If the cable is to interconnect to one of the circuit elements 14, the cable at some point, as shown for the cable 16C1, passes over a first guide (i.e. guide 20B for cable 16C1) and over, for example, the left side of guide 22A, passing between this guide and guide 20A into circuit element 14A.

A guide assembly for managing the running of cable from a panel is thus provided, which assembly assures against excessive bending of the cable during the running thereof. While for the preferred embodiment, an enlarged head 48 has been shown on each first guide 20 to assure against cable slipping off the end of the guides, this objective could be achieved by providing an enlarged end for either one or both of the guide members, although for reasons discussed, the embodiment shown is preferred. Other shapes for the enlarged ends and other suitable means for preventing cable from coming off the end of the guides could also be utilized. Further, while the guide assembly 12 for the preferred embodiment is configured to operate with a particular panel configuration, various modifications in the design could be made to permit the invention to be practiced with other types of panels. In particular, as mentioned, where cables exit the bottom or from another location on the circuit members 14, guide assemblies 12 could be provided adjacent such location, either in addition to or instead of the location shown. The radiuses R and R' could also be different for different types

of cable, so long as all radiuses are not less than the minimum bend radius for the cable utilized.

Thus, while the invention has been particularly shown and described above with reference to a preferred embodiment, the foregoing and other changes in form and detail may be made therein by one skilled in the art without departing from the spirit and scope of the invention.

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