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10-17-00

RECORDATION FORM COVER TRADEMARKS ONLY

TO: THE COMMISSIONER OF PATENTS AND TRADEMARKS: *Please record the attached original document(s) or copy(ies).*

SUBMISSION TYPE

- [X] New
- [ ] Resubmission (non-recordations) Document ID #_____
- [ ] Correction of PTO Error Reel #_____ Frame #_____
- [ ] Corrective Document Reel #_____ Frame #_____

CONVEYANCE TYPE

- [X] Assignment
- [ ] License
- [ ] Security Agreement
- [ ] Nanc Pro Tunc Assignment
- [ ] Merger — 09/27/00 Effective Date
- [ ] Change of Name
- [ ] Other_____

CONVEYING PARTY(IES) [ ] Mark if additional names of conveying parties attached.

Name: Staktek Corporation — 09/27/00 Execution Date

Formerly: _____

- [ ] Individually
- [ ] General Partnership
- [ ] Limited Partnership
- [X] Corporation
- [ ] Association
- [ ] Other _____
- [ ] Citizenship/State of Incorporation/Organization: Texas

RECEIVING PARTY(IES):

Name: Staktek Group L.P.
DBA/AKA/TA: Staktek
Composed of:
Address (line 1): 8900 Shoal Creek
Address (line 2):
Address (line 3): Austin (City) — TX (State/Country) — 787758 (Zip Code)

- [ ] Individually
- [ ] General Partnership
- [X] Limited Partnership
- [ ] Corporation
- [ ] Association
- [ ] Other _____
- [ ] Citizenship/State of Incorporation/Organization: Texas

[ ] If document to be recorded is an assignment and the receiving party is not domiciled in the United States, an appointment of a domestic representative is attached. (*Designation must be a separate document from Assignment.*)

FOR OFFICE USE ONLY

Domestic Representative Name and Address Enter for the first Receiving Party only.

Name
Address (line 1)
Address (line 2)
Address (line 3)
Address (line 4)

CORRESPONDENT NAME AND ADDRESS Area Code and Telephone No.

Name: J. Scott Denko
Address (line 1): George & Donaldson, L.L.P.
Address (line 2): 114 West 7th Street
Address (line 3): 1100 Norwood Tower
Address (line 4): Austin, Texas 78701

PAGES

Enter the total number of pages of the attached conveyance document including any attachments. 9

TRADEMARK APPLICATION NUMBER(S) OR REGISTRATION NUMBER(S) ☐ Mark if additional numbers attached.

Enter either the Trademark application number or the registration number (DO NOT ENTER BOTH numbers for the same property)

Trademark Application No(s).:	Registration No(s).:
	1,877,493
	1,790,187
	1,987,882

NUMBER OF PROPERTIES

Enter the total number of properties involved: Three (3)

FEE AMOUNT For Amount for Properties Listed (37 CFR 3.41): $90.00

Method of Payment:
☒ Enclosed **(included in the check covering the filing fee)**, or
☐ Deposit Account
(Enter for payment by deposit account or if additional fees can be charged to the account.)

☐ Debit Account No.:
☒ Authorized to charge additional fees to Deposit Account No. 501031, under Order No. 0254-078.

STATEMENT AND SIGNATURE

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document. Charges to deposit account are authorized, as indicated herein.

J. Scott Denko
Name of Person Signing

Signature

Oct. 17, 2000
Date

ASSIGNMENT OF INTANGIBLE PROPERTIES

WHEREAS, Staktek Corporation, a Delaware corporation, having a principal place of business at 8900 Shoal Creek, Suite 125, Austin, Texas 78758, owns certain intellectual properties consisting of inventions, patents, and patent applications (enumerated on attached and incorporated Exhibit 1.1), and trademarks (enumerated on attached and incorporated Exhibit 1.2) and trade secrets and know-how (listed on attached and incorporated Exhibit 1.3) (the intellectual properties being collectively, "Staktek Intangibles");

WHEREAS, Staktek Group L.P., a Texas limited partnership, desires to acquire and Staktek Corporation desires to assign to Staktek Group L.P., all of the Staktek Corporation rights in the Staktek Intangibles;

NOW, THEREFORE, Staktek Corporation, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, does hereby ASSIGN to Staktek Group L.P., all its right, title and interest, subject to any third party licenses before the EFFECTIVE DATE, in the Staktek Intangibles, this assignment including, but not being limited to:

1. The ASSIGNED INVENTIONS enumerated on Exhibit 1.1 whether created by Staktek Corporation, its legal representatives or its assigns in the United States or any other country or place anywhere in the world;

2. The ASSIGNED PATENTS enumerated on Exhibit 1.1;

3. The ASSIGNED PATENT APPLICATIONS enumerated on Exhibit 1.1;

4. The ASSIGNED TRADEMARKS and ASSIGNED TRADEMARK REGISTRATIONS enumerated on Exhibit 1.2;

5. The ASSIGNED KNOW HOW listed on Exhibit 1.3;

6. All rights of action on account of past, present, and future unauthorized use or infringement of said Staktek Intangibles including, but not limited to all rights to damages so accrued;

7. The right, where allowed by law, to file in the name of Staktek Group L.P. applications for patent and like protection for any Staktek Intangibles in any country or countries foreign to the United States;

8. All international rights or priorities associated with the Staktek Intangibles; and

9. As to all ASSIGNED TRADEMARKS, the right of inurement to Staktek Group L.P. of any prior use of any of said marks by Staktek Corporation.

This Assignment shall be binding upon and shall inure to the benefit of the successors, assigns, and legal representatives of the parties.

EXECUTED on the EFFECTIVE DATE indicated below:

Assignor: Staktek Corporation

Date: Sept. 27, 2000

By: James W. Cady
James Cady, President

THE STATE OF TEXAS §
§
COUNTY OF TRAVIS §

This instrument was acknowledged by James Cady on this the 27th day of September, 2000.

Jane Wiley
Notary Public in and for the State of Texas

(Seal)

JANE WILEY
Notary Public, State of Texas
My Commission Expires
JAN. 6, 2001

My commission expires: Jan 6. 2001

EXHIBIT 1.1 TO INTANGIBLES ASSIGNMENT

ASSIGNED INVENTIONS	First Named Inventors	ASSIGNED PATENTS (Issue Date)	ASSIGNED PATENT APPS (Filing Date)
1. Ultra High Density Integrated Circuit Packages Method and Apparatus	Burns	5,566,051 10/15/96	08/298,544 08/30/94
2. Ultra High Density Integrated Circuit Packages Method	Burns	5,279,029 01/18/94	08/059,401 05/11/93
3. Ultra High Density Modular Integrated Circuit Package	Burns	5,420,751 05/30/95	08/133,397 10/08/93
4. Ultra High Density Integrated Circuit Package	Burns	5,543,664 08/06/96	08/375,747 01/20/95
5. Ultra High Density Integrated Circuit Packages	Burns	5,550,711 08/27/96	08/436,902 05/08/95
6. Ultra High Density Integrated Circuit Packages Method	Burns	5,367,766 11/29/94	08/043,196 04/05/93
7. Ultra High Density Integrated Circuit Packages	Burns	5,446,620 08/29/95	08/133,395 10/08/93
8. Ultra High Density Integrated Circuit Packages	Burns	6,025,642 02/15/00	08/937,200 09/22/97
9. Ultra High Density Integrated Circuit Packages	Burns	6,049,123 04/11/00	08/935,380 09/22/97
10. Ultra High Density Integrated Circuit Packages Method and Apparatus	Burns	5,337,077 12/27/94	08/168,354 12/17/93
11. Method of Assembling Ultra High Density Integrated Circuit Packages	Burns	5,475,920 12/19/95	08/206,311 03/04/94
12. High Density Integrated Circuit Module with Snap-On Rail Assemblies	Burns	5,499,160 03/12/96	08/380,543 01/30/95
13. Multi-Signal Rail Assembly with Impedance Control for a Three-Dimensional High Density Integrated Circuit Package	Burns	5,561,591 10/01/96	08/289,468 08/12/94

ASSIGNED INVENTIONS	First Named Inventors	ASSIGNED PATENTS (Issue Date)	ASSIGNED PATENT APPS (Filing Date)
14. Lead-on-Chip Integrated Circuit Fabrication Method	Burns	5,221,642 06/22/93	07/746,268 08/15/91
15. Lead-on-Chip Integrated Circuit Apparatus	Burns	5,448,450 09/05/95	07/783,737 10/28/91
16. Lead-on-Chip Integrated Circuit Apparatus	Burns	5,528,075 06/18/96	08/375,874 01/20/95
17. Lead-on-Chip Integrated Circuit Apparatus	Burns	5,654,877 08/05/97	08/516,848 08/18/95
18. Hermetically Sealed Ceramic Integrated Circuit Heat Dissipating Package	Burns	5,572,065 11/05/96	08/328,338 10/24/94
19. Hermetically Sealed Ceramic Integrated Circuit Heat Dissipating Package Fabrication Method	Burns	5,702,985 12/30/97	08/325,719 10/19/94
20. Hermetically Sealed Integrated Circuit Lead-on Package Configuration	Burns	5,804,870 09/08/98	08/380,541 01/30/95
21. Method of Forming a Hermetically Sealed Circuit Lead-on Package	Burns	5,783,464 07/21/98	08/798,556 02/11/97
22. Simulcast Standard Multichip Memory Addressing System	Cady	5,371,866 12/06/94	07/891,609 06/01/92
23. Simulcast Standard Multichip Memory Addressing System	Cady	RE 36,229 06/15/99	08/510,729 11/20/95
24. Impact Solder Method and Apparatus	Roane	5,236,117 08/17/93	07/903,056 06/22/92
25. High Density Lead-on-Package Fabrication Method and Apparatus	Burns	5,484,959 01/16/96	07/990,334 12/11/92
26. High Density Lead-on-Package Fabrication Method	Burns	5,631,193 05/20/97	08/497,565 06/30/95

ASSIGNED INVENTIONS	First Named Inventors	ASSIGNED PATENTS (Issue Date)	ASSIGNED PATENT APPS (Filing Date)
27. Apparatus and Method of Manufacturing a Surface Mount Package	Burns		09/222,263 12/28/98
28. Warp-Resistant Ultra-Thin Integrated Circuit Package Fabrication Method	Burns	5,369,056 11/29/94	08/037,830 03/29/93
29. Warp-Resistant Ultra-Thin Integrated Circuit Package	Burns	5,581,121 12/03/96	08/280,968 07/27/94
30. Warp-Resistant Ultra-Thin Integrated Circuit Package Fabrication Method	Burns	5,864,175 01/26/99	08/644,491 05/10/96
31. Warp-Resistant Ultra-Thin Integrated Circuit Package Fabrication Method	Burns	5,369,058 11/29/94	08/206,301 03/04/94
32. Ultra-High Density Warp-Resistant Memory Module	Burns	5,644,161 07/01/97	08/473,593 06/07/95
33. Method of Manufacturing an Ultra-High Density Warp-Resistant Memory Module	Burns	5,843,807 12/01/98	08/686,985 07/25/96
34. Ultra-High Density Warp-Resistant Memory Module	Burns	5,828,125 10/27/98	08/758,839 12/02/96
35. Three-Dimensional Warp-Resistant Integrated Circuit Module Method and Apparatus	Burns	5,801,437 09/01/98	08/514,294 08/11/95
36. Three-Dimensional Warp-Resistant Integrated Circuit Module Method and Apparatus	Burns	5,895,232 04/20/99	08/888,850 07/07/97
37. Capacitive Coupling Configuration for an Integrated Circuit Package	Roane	5,498,906 03/12/96	08/153,511 11/17/93
38. Bus Communication System for Stacked High Density Integrated Circuit Packages	Burns	5,455,740 10/03/95	08/206,829 03/07/94
39. Bus Communication System for Stacked High Density Integrated Circuit Packages with Trifurcated Distal Lead Ends	Burns	5,479,318 12/26/95	08/440,500 05/12/95

ASSIGNED INVENTIONS	First Named Inventors	ASSIGNED PATENTS (Issue Date)	ASSIGNED PATENT APPS (Filing Date)
40. Bus Communication System for Stacked High Density Integrated Circuit Packages	Burns	5,552,963 09/03/96	08/506,309 07/24/95
41. Bus Communication System for Stacked High Density Integrated Circuit Packages	Burns	5,586,009 12/17/96	08/630,083 04/09/96
42. Bus Communication System for Stacked High Density Integrated Circuit Packages with Bifurcated Distal Lead Ends	Burns	5,493,476 02/20/96	08/445,848 05/22/95
43. Bus Communication System for Stacked High Density Integrated Circuit Packages Having an Intermediate Lead Frame	Burns	5,541,812 07/30/96	08/526,470 09/11/95
44. Integrated Circuit Packages Having an Externally Mounted Lead Frame Having Bifurcated Distal Lead Ends	Burns	5,978,227 11/02/99	08/645,319 05/13/96
45. Method of Manufacturing a Bus Communication System for Stacked High Density Integrated Circuit Packages	Burns	5,605,592 02/25/97	08/445,895 05/22/95
46. High Density Integrated Circuit Module with Complex Electrical Interconnect Rails	Roane	5,592,364 01/07/97	08/377,578 01/24/95
47. Method of Manufacturing a High Density Integrated Circuit Module Having Complex Electrical Interconnect Rails	Burns	5,588,205 12/31/96	08/523,201 09/05/95
48. Integrated Circuit Package with Overlapped Die on a Common Lead Frame	Burns	5,585,668 12/17/96	08/601,880 02/15/96
49. Method of Manufacturing an Integrated Circuit Package Having a Pair of Die on a Common Lead Frame	Burns	5,615,475 04/01/97	08/517,485 08/21/95
50. Method of Manufacturing a High Density Integrated Circuit Module with Complex Electrical Interconnect Rails Having Electrical Interconnect Strain Relief	Burns	5,778,522 07/14/98	08/650,721 05/20/96

ASSIGNED INVENTIONS	First Named Inventors	ASSIGNED PATENTS (Issue Date)	ASSIGNED PATENT APPS (Filing Date)
51. Method of Making High Density Integrated Circuit Module	Burns	5,960,539 10/05/99	09/021,744 02/11/98
52. High Density Integrated Circuit Module with Complex Electrical Interconnect Rails Having Electrical Interconnect Strain Relief	Burns		09/343,432 06/30/99
53. Apparatus and Method of Manufacturing a Warp-Resistant Thermally Conductive Integrated Circuit Package	Burns	5,945,732 08/31/99	08/815,537 03/12/97
54. Apparatus and Method of Manufacturing a Warp-Resistant Thermally Conductive Integrated Circuit Package	Burns		09/115,293 07/14/98
55. Apparatus and Method of Manufacturing a Hybrid Memory Module	Cady		09/075,424 05/08/98
56. Rambus Stakpak	Cady		PCT/US98/27873 03/23/98
57. Clock Driver with Instantaneously Selectable Phase and Method for Use in Data Communication Systems	Rapport		09/133,297 08/12/98
58. Stacked Micro Ball Grid Array Packages	Burns		09/221,350 12/28/98
59. Flexible Circuit Connector for Stacked Chip Module	Burns		09/406,015 09/24/99

EXHIBIT 1.2 TO INTANGIBLES ASSIGNMENT

ASSIGNED MARK	ASSIGNED TRADEMARK REGISTRATION (Registration Date)	Corresponding Application (Filing Date)
1. STAKPAK	1,877,493 02/07/95	74/482,635 01/21/94
2. Stylized "S"	1,790,187 08/31/93	74/276,327 05/15/92
3. STAKTEK	1,987,882 07/23/96	74/515,812 04/19/94

ASSIGNED KNOW HOW

1. DRAM Testing
2. Factory Automation
3. Module (DIMM) Design
4. Electronic Packaging
5. Surface Mount Assembly
6. Thermal Modeling