RECEIVED
OCT - 2001

FORM PTO-1618A
Expires 06/30/99
OMB 0651-0027

10-17-2001

101876353

RECORDATION FORM COVER SHEET
TRADEMARKS ONLY

TO: The Commissioner of Patents and Trademarks: Please record the attached original document(s) or copy(ies).

Submission Type

- [X] New (10/09/01)
- [ ] Resubmission (Non-Recordation) Document ID #
- [ ] Correction of PTO Error Reel # Frame #
- [ ] Corrective Document Reel # Frame #

Conveyance Type

- [ ] Assignment
- [ ] License
- [X] Security Agreement
- [ ] Nunc Pro Tunc Assignment
- [ ] Merger — Effective Date Month Day Year
- [ ] Change of Name
- [ ] Other

Conveying Party [ ] Mark if additional names of conveying parties attached

Name: Xemod, Inc — Execution Date Month Day Year: 2/22/00

Formerly:

- [ ] Individual
- [ ] General Partnership
- [ ] Limited Partnership
- [ ] Corporation
- [ ] Association
- [ ] Other
- [X] Citizenship/State of Incorporation/Organization: Arizona

Receiving Party [ ] Mark if additional names of receiving parties attached

Name: Silicon Valley Bank

DBA/AKA/TA:

Composed of:

Address (line 1): 3003 Tasman Dr. HA155

Address (line 2):

Address (line 3): Santa Clara (City) CA (State/Country) 95054 (Zip Code)

- [ ] Individual
- [ ] General Partnership
- [ ] Limited Partnership
- [ ] If document to be recorded is an assignment and the receiving party is not domiciled in the United States, an appointment of a domestic representative should be attached. *(Designation must be a separate document from Assignment.)*
- [X] Corporation
- [ ] Association
- [ ] Other
- [X] Citizenship/State of Incorporation/Organization: California

FOR OFFICE USE ONLY

Mail documents to be recorded with required cover sheet(s) information to:
Commissioner of Patents and Trademarks, Box Assignments, Washington, D.C. 20231

Domestic Representative Name and Address

Enter for the first Receiving Party only.

Name

Address (line 1)

Address (line 2)

Address (line 3)

Address (line 4)

Correspondent Name and Address

Area Code and Telephone Number

Name: Silicon Valley Bank

Address (line 1): 3003 Tasman Dr. HA155

Address (line 2):

Address (line 3):

Address (line 4): Santa Clara CA 95054

Pages

Enter the total number of pages of the attached conveyance document including any attachments. #

Trademark Application Number(s) or Registration Number(s)

☐ Mark if additional numbers attached

Enter either the Trademark Application Number or the Registration Number (DO NOT ENTER BOTH numbers for the same property).

Trademark Application Number(s)			Registration Number(s)		
			2,358,266		
			2,304,754		
			2,202,745		

Number of Properties

Enter the total number of properties involved. # 3

Fee Amount

Fee Amount for Properties Listed (37 CFR 3.41): $ 90.00

Method of Payment: Enclosed ☒ Deposit Account ☐

Deposit Account
(Enter for payment by deposit account or if additional fees can be charged to the account.)
Deposit Account Number: #

Authorization to charge additional fees: Yes ☐ No ☑

Statement and Signature

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document. Charges to deposit account are authorized, as indicated herein.

Richelle Medina — Name of Person Signing

Richelle Medina — Signature

9/28/01 — Date Signed

ADDENDUM TO INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Addendum to Intellectual Property Security Agreement is executed pursuant to, and is an addendum to, an Intellectual Property Security Agreement, dated February 22, 2000. This Addendum to Intellectual Property Security Agreement is presented for recordation as constructive notice that XEMOD INCORPORATED ("Grantor"), with its principal office at 9365 S. McKenny Street, Suite 105, Tempe, AZ 85284, the owner of the intellectual property identified in the Exhibit(s) attached hereto, has granted to Silicon Valley Bank ("Bank"), with its principal office at 3003 Tasman Drive, Santa Clara, California, 95054, a security interest in the intellectual property described on the Exhibit(s) attached hereto, and the exclusive rights comprised in the intellectual property, to secure payment of a debt.

IN WITNESS WHEREOF, Grantor has executed this Addendum to Intellectual Property Security Agreement as of August 9, 2001.

GRANTOR:

XEMOD INCORPORATED

By: _____

Name: J H Johnson

Title: President / CEO

[illegible]XemodAddendum.doc

Exhibit "A" attached to that certain Intellectual Property Security Agreement dated August 9, 2001.

EXHIBIT "A"

COPYRIGHTS

SCHEDULE A - ISSUED COPYRIGHTS

COPYRIGHT DESCRIPTION	REGISTRATION NUMBER	DATE OF ISSUANCE

SCHEDULE B - PENDING COPYRIGHT APPLICATIONS

COPYRIGHT DESCRIPTION	APPLICATION NUMBER	DATE OF FILING	DATE OF CREATION	FIRST DATE OF PUBLIC DISTRIBUTION

SCHEDULE C - UNREGISTERED COPYRIGHTS (Where No Copyright Application is Pending)

COPYRIGHT DESCRIPTION	DATE OF CREATION	FIRST DATE OF DISTRIBUTION	ORIGINAL AUTHOR OR OWNER OF COPYRIGHT (IF DIFFERENT FROM GRANTOR)	DATE AND RECORDATION NUMBER OF IP AGREEMENT TO OWNER OF GRANTOR (IF ORIGINAL AUTHOR OR OWNER OF COPYRIGHT IS DIFFERENT FROM GRANTOR)

Exhibit "B" attached to that certain Intellectual Property Security Agreement dated August 9, 2001.

EXHIBIT "B"

PATENTS

PATENT DESCRIPTION	DOCKET NO.	COUNTRY	FILING DATE	STATUS
Pre-Post Distortion Amplifier	**5,781,069**	USA	May 16, 1996	Granted
Quasi-Mesh Gate Structure for Lateral RF MOS Devices	**5,900,663**	USA	Feb. 7, 1998	Granted
Source Connection Structure for Lateral RF MOS Devices	**5,949,104**	USA	Feb. 7, 1998	Granted
Lateral RF MOS Device Having a Combined Source Structure	**6,034,415**	USA	April 8, 1999	Granted
Glue Deposit Device for Power Printed Circuit Board	**6,045,653**	USA	July 24, 1998	Granted
Method for Fabricating a Lateral RF MOS Device with a Non-Diffusion Source-Backside Connection.	**6,048,772**	USA	May 4, 1998	Granted
Fabrication of Lateral RF MOS Devices With Enhanced RF Properties	**6,063,678**	USA	July 31, 1999	Granted
RF Power MOSFET Device with Extended Linear Region of Transconductance Characteristic at Low Drain Current.	**6,064,088**	USA	June 15, 1998	Granted
Method for Fabricating Lateral RF MOS Devices with enhanced RF Properties.	**6,190,978**	USA	April 16, 1999	Granted
Pre-Post Distortion Amplifier	**0281622**	KOREA	Nov. 12, 1998	Granted
Lateral RF MOS Device with Improved Drain Structure	**6,222,233**	USA	Oct. 4, 1999	Granted
E/Lateral RF MOS Device with Improved Breakdown Voltage	**6,271,552**	USA	Oct. 4, 1999	Granted

J:\legal\docs\IPAgr\XemodAddendum.doc
08/09/01by jgu

Exhibit "C" attached to that certain Intellectual Property Security Agreement dated August 9, 2001.

EXHIBIT "C"

TRADEMARKS

TRADEMARK DESCRIPTION	COUNTRY	SERIAL NO.	REG. NO	STATUS
Xemod	USA		**2,202,745**	GRANTED
Xemod Logo	USA		**2,304,754**	GRANTED
XeMOS	USA		**2,358,266**	GRANTED

J:\legalDocs\IPAgr\XemodAddendum.doc
08/09/01by jgu

Exhibit "D" attached to that certain Intellectual Property Security Agreement dated August 9, 2001.

EXHIBIT "D"

MASK WORKS

MASK WORK DESCRIPTION	COUNTRY	SERIAL NO.	REG. NO	STATUS

Patents and Trademarks.

1. **List of Patents**
   a. Baskin et al., "Pre-Post Distortion Amplifier," U.S. Patent No. 5,781,069, issued July 14, 1998 filed May 16, 1996, corresponds to U.S. Patent Application No. 08/649,841; **Granted.**
   The Invention discloses an apparatus and a method for linearization of a cascade of non-linear RF amplifiers by matching the distortion characteristics of each pair of amplifiers, and by taking into account the variation of the distortion characteristics of each amplifier over frequency, temperature and other sources of non-linearity.
   b. Johnson et al., "Quasi-Mesh Gate Structure for Lateral RF MOS Devices" U.S. Patent No. 5,900,663, issued May 4, 1999, filed on February 7, 1998, corresponds to the U.S. patent application No. 09/020,256; **Granted.**
   A lateral RF MOS transistor fabricated with a quasi-mesh structure is described.
   c. D'Anna et al., "Source Connection Structure for Lateral RF MOS Devices" U.S. Patent No. 5,949,104, issued September 7, 1999, filed on February 7, 1998, corresponds to the U.S. patent application number 09/020,257; **Granted.**
   A source connection structure for a lateral RF MOS device that utilizes a conductive plug to connect a source area and a body area of the device to the backside is disclosed.
   d. Johnson et al., "Lateral RF MOS Device Having a Combined Source Structure" U.S. Patent No. 6,034,415, issued March 7, 2000, filed April 8, 1999, corresponds to the U.S. patent application No. 09/289,370; **Granted.**
   A lateral RF MOS device having a combined source connection structure that utilizes a diffusion area and a conductive plug region is disclosed.
   e. Johnson et al., "Glue Deposit Device for Power Printed Circuit Board" U.S. Patent No. 6,045,653, issued April 4, 2000, filed July 24, 1998, corresponds to the U.S. patent application No. 09/122,456; **Granted.**
   A glue deposit device and method for automatically mounting a plurality of power devices to a heatsink using a plurality of spring clamps is disclosed.
   f. D'Anna et al., "Method for Fabricating a Lateral RF MOS Device with a Non-Diffusion Source- Backside Connection" U.S. Patent No. 6,048,772, issued April 11, 2000, filed May 4, 1998, corresponds to the U.S. patent application No. 09/072,393; **Granted.**
   Methods of fabrication of a lateral RF MOS device having a non-diffusion connection between source and substrate using both interdigitated and mesh structures and silicide gates are disclosed.

List of Patents (cont.)

g. D'Anna et al., "Fabrication of Lateral RF MOS Devices with Enhanced RF Properties" U.S. Patent No 6,063,678, issued on May 16, 2000 filed on July 31, 1999, corresponds to the U. S. Patent application No. 09/366,612, **Granted.**
Method of fabrication of lateral RF MOS devices having a non-diffusion connection between source and backside with interdigitated and mesh structures and topside silicided gates.

h. D'Anna et al., "RF Power MOSFET Device with Extended Linear region of Transconductance Characteristic at Low Drain Current" U.S. Patent No 6.064,088, issued May 16, 2000 corresponds to U.S. Patent application No 09/097,532, filed on 06/15/98 **Granted.**
A semiconductor MOSFET device having a decreased length of the body diffusion is disclosed.

i. D'Anna et al., "Method for fabricating lateral RF MOS devices with enhanced RF properties" U.S. Patent No. 6,190,978, issued February 20, 2001, filed April 16, 1999, corresponds to the U.S. patent application No. 09/293,431; **Granted.**
Methods of fabrication of a lateral RF MOS device having a non-diffusion connection between source and substrate are disclosed. In one embodiment, the lateral RF MOS device has an interdigitated silicided gate structure. In another embodiment, the lateral RF MOS device has a quasi-mesh silicided gate structure. Both sides of each gate are oxidized thus preventing possible shorts between source and gate regions and between drain and gate regions. The top of each gate is silicided once the protective layer of silicon nitride is removed.

j. Baskin et al., corresponding to the US Patent "Pre-Post Distortion Amplifier," Korean Letters Patent No. 0281622, issued November 20, 2000, filed on November 12, 1998, corresponds to the patent application No. 1998-0709116; **Granted.**

k. D'Anna et al., "Lateral RF MOS Device with Improved Drain Structure" U.S. Patent No. 6,222,233 B1, issued April 24, 2001, filed on October 4, 1999, corresponds to the U.S. patent application No. 09/410,934; **Granted.**
The lateral RF MOS device having a conducive plug in the source region and an oxide plug in the drain region is disclosed. The oxide plug in the drain region reduces the drain-source capacitance, improves the matching ability to the outside circuitry, and results in a lateral RF MOS device having a wider BW, and an improved power efficiency than a prior art lateral RF MOS device. The oxide plug can comprise a shallow plug or a deep plug. The shallow oxide plug results in a lesser reduction in the drain-source capacitance but is relatively easy to fabricate. The deep oxide plug results in a higher reduction in the drain-source capacitance but is relatively difficult to fabricate.

l. U.S. Patent Application; serial number 09/413,912, filed on 10/04/99; **Allowed**.
m. U.S. Patent Application; serial number 09/567,422, filed on 05/09/00; **Pending**.
n. U.S. Patent Application; serial number 09/494,408, filed on 01/29/00; **Pending**.

2. List of Trademarks
   a. QuikPAC
   b. Xemod
   c. Xemod logo
   d. XeMOS