

02-06-2002

FORM PTO-1595

1-31-92

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HEET

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U.S. DEPARTMENT OF COMMERCE  
Patent and Trademark Office

To the Honorable Commissioner of Patents and Trademarks: **Please record the attached** original documents or copy thereof.

1. Name of conveying party(ies):  
**Sequence Design, Inc.**  
*1.22.02*  
Additional name(s) of conveying party(ies) attached?  Yes  No

2. Name and address of receiving party(ies):  
Name: Silicon Valley Bank  
Internal Address: ~~HC150~~ HA155

3. Nature of conveyance:  
 Assignment  Merger  
 Security Agreement  Change of Name  
 Other \_\_\_\_\_  
Execution Date: April 17, 2001

Street Address: 3003 Tasman Drive  
City: Santa Clara State: CA ZIP: 95054  
Additional name(s) & address(es) attached?  Yes  No

4. Application number(s) or trademark number(s):  
If this document is being filed together with a new application, the execution date of the application is: \_\_\_\_\_  
A. Trademark Application No.(s)      B. Trademark No.(s)  
~~75,813,579~~      1,132,614  
2,306,075      1,138,622  
2,262,053      2,252,594  
Additional numbers attached?  Yes  No

5. Name and address of party to whom correspondence concerning document should be mailed:  
Name: **Silicon Valley Bank**  
Internal Address: Loan Documentation ~~HC150~~ HA155  
Street Address: 3003 Tasman Dr.  
City: Santa Clara State: Ca ZIP: 95054

6. Total number of applications and trademark involved: 6  
7. Total fee (37 CFR 3.41): \$165.00  
 Enclosed  
 Authorized to be charged to deposit account  
8. Deposit account number:  
(Attach duplicate copy of this page if paying by deposit account)

02/05/2002 GT0M11 00000243 75813579  
01 FC:481 40.00 OP  
02 FC:482 125.00 OP

DO NOT USE THIS SPACE

9. Statement and signature.  
*To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.*  
Jacquelyn Le  
Name of Person Signing  
  
Signature  
10/19/01  
Date

Total number of pages comprising cover sheet:

OMB No 0651 -0011 (exp 4/94)

TRADEMARK  
REEL: 002437 FRAME: 0499

## INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement is entered into as of April 17, 2001 by and between SILICON VALLEY BANK ("Bank") and Sequence Design, Inc. ("Grantor").

### RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodation to Grantor (the "Loans") in the amounts and manner set forth in that certain Loan and Security Agreement by and between Bank and Grantor dated April 17, 2001 (as the same may be amended, modified or supplemented from time to time, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in certain Copyrights, Trademarks, Patents, and Mask Works to secure the obligations of Grantor under the Loan Agreement.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement, Grantor hereby represents, warrants, covenants and agrees as follows:

### AGREEMENT

To secure its obligations under the Loan Agreement, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its Intellectual Property Collateral (including without limitation those Copyrights, Patents, Trademarks and Mask Works listed on Schedules A, B, C, and D hereto), and including without limitation all proceeds thereof (such as, by way of example but not by way of limitation, license royalties and proceeds of infringement suits), the right to sue for past, present and future infringements, all rights corresponding thereto throughout the world and all re-issues, divisions continuations, renewals, extensions and continuations-in-part thereof.

This security interest is granted in conjunction with the security interest granted to Bank under the Loan Agreement. The rights and remedies of Bank with respect to the security interest granted hereby are in addition to those set forth in the Loan Agreement and the other Loan Documents, and those which are now or hereafter available to Bank as a matter of law or equity. Each right, power and remedy of Bank provided for herein or in the Loan Agreement or any of the Loan Documents, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right, power or remedy provided for herein and the exercise by Bank of any one or more of the rights, powers or remedies provided for in this Intellectual Property Security Agreement, the Loan Agreement or any of the other Loan Documents, or now or hereafter existing at law or in equity, shall not preclude the simultaneous or later exercise by any person, including Bank, of any or all other rights, powers or remedies.

IN WITNESS WHEREOF, the parties have cause this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

Address of Grantor:

Sequence Design, Inc.

469 El Camino Real, Ste. 202  
Santa Clara, CA 95050

By: 

Attn: \_\_\_\_\_

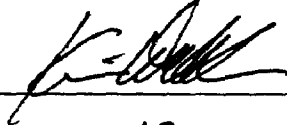
Title: Director of Finance

BANK:

Address of Bank:

SILICON VALLEY BANK

3003 Tasman Drive  
Santa Clara, CA 95054-1191

By: 

Attn: \_\_\_\_\_

Title: VP

EXHIBIT A

Copyrights

Description

Registration/  
Application  
Number

Registration/  
Application  
Date

EXHIBIT A

Copyrights

Description

Registration/  
Application  
Number

Registration/  
Application  
Date

Isoreg computer power modules

TX1106040

1/19/83

EXHIBIT B

Patents

<u>Description</u>	<u>Registration/ Application Number</u>	<u>Registration/ Application Date</u>
C/Methods for determining on-chip interconnect process parameters	6,057,171	5/2/00
E/Power estimation software system	6,151,568	911/21/00
Interconnection modeling system for IC designing – has network extract tool which analyses signal path of IC and offers electric network model of signal path based on mapping information and stored parameterised data	5,901,063	5/4/99
Inductor-capacitor impedance device and mfr. for lamp ballast- has integral terminal formed as folded end portion of both foil and dielectric material	4,368,407	1/11/83
Discharge lamp ballast circuit – has two inductors capacitor windings and cores between lamp and power source	4,327,311	4/27/83

EXHIBIT C

Trademarks

<u>Description</u>	<u>Registration/ Application Number</u>	<u>Registration/ Application Date</u>
Cartier	75,813,579	10/4/99
Isoshield	1,132,614	4/8/80
Isoreg	1,138,622	8/12/80
Sente	2,306,075	1/4/00
Sente	2,262,053	7/20/99
Wattwatcher	2,252,594	6/15/99

EXHIBIT D

Mask Works

Description

Registration/  
Application  
Number

Registration/  
Application  
Date

none