10-09-2002

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FORM PT((Rev. 03/0 OMB No. (

ON FORM COVER SHEET
DEMARKS ONLY

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof.

1. Name of conveying party(ies):
SYCHIP, INC.

☐ Individual(s) ☐ Association
☐ General Partnership ☐ Limited Partnership
☒ Corporation-State **DE**
☐ Other

10/4/02

Additional name(s) of conveying party(ies) attached? ☐Yes ☒ No

2. Name and address of receiving party(ies):
Name: **Silicon Valley Bank**
Internal Address: HA155

Street Address: 3003 Tasman Drive

City: Santa Clara State: CA ZIP: 95054

☐ Individual(s) citizenship
☐ Association
☐ General Partnership
☐ Limited Partnership
☒ Corporation-State-**DE**
☐ Other
If assignee is not domiciled in the United States, a domestic representative designation is attached: ☐ Yes ☐ No
Additional name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance:

☐ Assignment ☐Merger

☒Security Agreement ☐ Change of Name

☐ Other ________________

Execution Date: **9/20/02**

4. Application number(s) or registration number(s):

A. Trademark Application No.(s)	B. Trademark No.(s)
76/058,023	

Additional numbers attached? ☐ Yes ☒ No

OFFICE OF PUBLIC RECORDS
2002 OCT -4 AM 9:15
FINANCE SECTION

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: **Silicon Valley Bank**

Internal Address: Loan Documentation HA155

Street Address: 3003 Tasman Dr.

City: Santa Clara State: Ca ZIP: 95054

6. Total number of applications and registrations involved: **1**

7. Total fee (37 CFR 3.41): **$40.00**
☒ Enclosed

☐ Authorized to be charged to deposit account

8. Deposit account number:
(Attach duplicate copy of this page if paying by deposit account)

DO NOT USE THIS SPACE

10/08/2002 LMUELLER 00000070 76058023

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9. Statement and signature.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Shannon Hubbard — [signature] — 9/25/02

Name of Person Signing — Signature — Date

Total number of pages including cover sheet, attachments, and document: 16

Mail documents to be recorded with required cover sheet information to:
Commissioner of Patent & Trademarks, Box Assignments
Washington, D.C. 20231

INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement is entered into as of September 20, 2002 by and between SILICON VALLEY BANK ("Bank") and Sychip, Inc. ("Grantor").

RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodation to Grantor (the "Loans") in the amounts and manner set forth in that certain Loan and Security Agreement by and between Bank and Grantor dated September 20, 2002 (as the same may be amended, modified or supplemented from time to time, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in certain Copyrights, Trademarks, Patents, and Mask Works to secure the obligations of Grantor under the Loan Agreement.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

To secure its obligations under the Loan Agreement, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its Intellectual Property Collateral (including without limitation those Copyrights, Patents, Trademarks and Mask Works listed on Schedules A, B, C, and D hereto), and including without limitation all proceeds thereof (such as, by way of example but not by way of limitation, license royalties and proceeds of infringement suits), the right to sue for past, present and future infringements, all rights corresponding thereto throughout the world and all re-issues, divisions continuations, renewals, extensions and continuations-in-part thereof. To the extent that Intellectual Property Collateral is any license or contract right of Grantor, the security interest herein granted extends only to Grantor's interest therein, and does not extend to such licenses or contract rights to the extent that the granting of a security interest therein would be prohibited by applicable law, or (ii) that such rights are nonassignable by their terms (but only to the extent the prohibition is enforceable under applicable law, including, without limitation, Section 9.318(d) of the Code) without the consent of the licensor or other party (but only to the extent such consent has not been obtained). Except as disclosed on the Schedule to the Loan and Security Agreement, Grantor is not a party to, nor is bound by, any material license or other material agreement that prohibits or otherwise restricts Grantor from granting a security interest in Grantor's interest in such license or agreement or any other property. Without prior notice to Bank, Grantor shall not enter into, or become bound by, any such license or agreement which is reasonably likely to have a material impact on Grantor's business or financial condition. Grantor shall take such commercially reasonable steps as Bank requests to obtain the consent of, or waiver by, any person whose consent or waiver is necessary for such licenses or contract rights to be deemed "Collateral" and for Bank to have a security interest in it that might otherwise be restricted or prohibited by law or by the terms of any such license or agreement, whether now existing or entered into in the future.

This security interest is granted in conjunction with the security interest granted to Bank under the Loan Agreement. The rights and remedies of Bank with respect to the security interest granted hereby are in addition to those set forth in the Loan Agreement and the other Loan Documents, and those which are now or hereafter available to Bank as a matter of law or equity. Each right, power and remedy of Bank provided for herein or in the Loan Agreement or any of the Loan Documents, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right,

power or remedy provided for herein and the exercise by Bank of any one or more of the rights, powers or remedies provided for in this Intellectual Property Security Agreement, the Loan Agreement or any of the other Loan Documents, or now or hereafter existing at law or in equity, shall not preclude the simultaneous or later exercise by any person, including Bank, of any or all other rights, powers or remedies.

IN WITNESS WHEREOF, the parties have cause this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

Address of Grantor:

2805 North Dallas Parkway, Suite 400
Plano, TX 75093

Attn: ____________________

Sychip, Inc.

By: [signature]

Title: CONTROLLER & SECRETARY

BANK:

Address of Bank:

16633 N. Dallas Parkway, Sixth Floor
Dallas, TX 75001

Attn: ____________________

SILICON VALLEY BANK

By: [signature]

Title: Relationship Manager

EXHIBIT A

Copyrights

Description	Registration/ Application Number	Registration/ Application Date

EXHIBIT B

Patents

Description	Registration/ Application Number	Registration/ Application Date

EXHIBIT C

Trademarks

Description	Registration/ Application Number	Registration/ Application Date

EXHIBIT D

Mask Works

Description	Registration/ Application Number	Registration/ Application Date

	Title of Issued Patents	Category	Patent Number	File Date	Owner
1	Integrated Circuit Chip-and-Substrate Assembly	**Process**	4,670,770	02/17/1984	Tai 8
2	Interconnection Lines for Wafer-Scale-Integrated Assemblies	**Electrical Design**	4,703,288	04/03/1985	Frye 3-12
3	Decentralized Bus Arbitration Using Distributed Arbiters	**Electrical Design**	4,745,548	01/23/1987	Blahut 26
78	Optical Fiber Switch	**Fiber Optics**	4,896,937	01/30/1990	
80	Optical Assembly Comprising optical fiber coupling means	**Fiber Optics**	4,995,695	02/26/1991	
79	Optical Fiber Switch	**Fiber Optics**	5,000,532	03/19/1991	
4	Integrated Circuit Package and Compact Assemblies Thereof	**Structure**	5,043,794	08/27/1991	Tai
5	Method of Soldering Including Removal of Flux Residue (immersion)	**Material and Process**	5,125,560	11/04/1991	Degani 11-1
6	Solder Paste (water cleanable, no-clean)	**Material**	5,150,832	06/28/1991	Degani 10-3
7	Bonding Method using ... Alternating Gold and Tin Layers	**Material and Process**	5,197,654	11/15/1991	Katz 5-1-21-4
8	Solder Paste and Method of Using the Same ("no-clean")	**Material**	5,211,764	11/10/1992	Degani 13
9	Debondable Metallic Bonding Method (for burn-in, dissim metal layer)	**Bumped Die Burn-in Testing**	5,234,149	08/28/1992	Katz 11-3-23
10	Permanent Metallic Bonding Method (codeposited metallic "micro-Velcro")	**Material**	5,234,153	08/28/1992	Bacon 4-6-2-22-5
11	Pseudo-Electroless, Followed by Electroless, Metallization of Ni	**Material and Process**	5,264,107	12/17/1991	Bentson 1-3-1
12	Method of Making an Article Comprising Solder Bump Bonding	**Process**	5,307,983	04/27/1993	Dudderar 7-1
13	Surface Mount Assembly of Leadless IC Packages (BGA bumping)	**Process**	5,346,118	09/28/1993	Degani 14-8-4
14	An Improved Solder Paste Mixture (mixed alloy powder)	**Material**	5,382,300	03/22/1994	Blonder 61-17-10
15	Soldering Material and Procedure (mixed size powder)	**Material and Process**	5,385,290	11/24/1993	Degani 15
16	MCMs Having Chip-to-Chip Intercon (w Reduced Signal Volt Lev & Swing)	**Electrical Design**	5,461,333	02/24/1994	Condon 17-13-16-32-32
17	Electronic Device Package (Shell and Gel)	**Structure**	5,473,512	06/16/1994	Degani 20-11-3-3
18	Temporary Connections for Fast Electrical Access to Electronic Devices	**Electrical Die Testing**	5,481,205	11/23/1994	Frye 15-6-35
19	Method for Bumping Silicon Devices (single die bumping for repair)	**Process**	5,505,367	11/02/1994	Degani 24-14-1
20	Process for Fabricating an IC (MCM tile dicing protection)	**Process**	5,516,728	03/31/1994	Degani 18-6
21	Method for Making Multichip Ckts Using Active Semicon Substrates	**Active Substrate Design**	5,534,465	01/10/1995	Frye 16-36
22	Method and Apparatus for Assembling MCMs	**Structure**	5,564,617	06/07/1995	Degani 25-15-39
23	Packaging MCMs without Wire-bond Interconnections (flip-tile in BGA)	**Structure**	5,608,262	02/24/1995	Degani 21-12-4-6-41
24	Bonding Scheme using Group IV Metallic Layer	**Mahterial**	5,622,305	05/10/1995	Bacon 7-3-14-21-37
25	Thin Packaging of MCMs w Enhanced Thermal/Power Management	**Structure**	5,646,282	02/24/1995	Degani 23-13-5-7-42
26	Thin Packaging of MCMs w Enhanced Thermal/Power Management	**Structure**	5,646,828	08/20/1996	Degani 28-19-10-10-45
50	Curbside Circuitry for Interactive Communications Services	**Design**	5,699,105	12/16/1997	Chen 1-1-31

27	MCMs with Isolated Coupling between Modules	**Design**	5,747,982	12/05/1996	Dromgoole 3-16-18-7-46
28	Electronic Device Pkg'g Enclosed by a Pliant Medium Laterally...	**Structure**	5,767,447	12/05/1995	Dudderar 16-6-6-21
29	Cleaning Solder-Bonded Flip-Chip Assemblies	**Process**	5,778,913	02/20/1997	Degani 30-20-9
30	Method and Apparatus for Forming Fine Patterns on PCB	**Equipment**	5,834,160	11/10/1998	Ferry 1-8-7-1-43
31	RF IC Package	**Structure**	5,869,894	07/18/1997	Degani 34-3-49
32	Chip-on-Chip IC Packages	**Structure**	5,898,223	10/08/1997	Frye 19-2-11
33	Etchant for Under Bump Metallization ("Flip-Chip Metallization")	**Process**	5,904,859	04/01/1997	Degani 31
34	Method and Apparatus for Flip-Chip Dispensing (Hi-Speed BDDS)	**Equiment**	5,966,903	05/28/1998	Dudderar 27-1
35	Flip Chip Packaging of Memory Chips	**Structure**	5,990,564	05/28/1997	Degani 35-23-50
36	Solder Bonding Printed Solder Boards (via in Pad)	**Material and Process**	6,013,877	03/12/1998	Degani 40-55
37	Manufacture of flip-chip device.	**Process**	6,015,652	02/24/1998	Ahlquist 2-39
38	Method of Packaging Fragile Devices with a Gel Medium ...	**Structure**	6,020,219	09/26/1997	Dudderar 31-12-10-36
49	Self Managing Extended Secondary Cache Memory	**Design**	6,029,224	02/22/2000	Asthana 5-1-38
39	Method for Testing Integrated Circuits	**Testing**	6,043,670	12/16/1997	Degani 38-12
40	Integrated Circuit Bonding Method and Apparatus	**Process**	6,074,897	01/28/1999	Degani 47-9
41	MCM with High Q Overlapping Resonator	**Design**	6,075,427	??? (issued 06/13/2000)	Tai 54-2
42	Method and Apparatus for Assembling MCMs (original microSMT)	**Process**	6,077,725	09/03/1992	Degani 12-6-25
43	Solder Bonding Printed Solder Boards (Practical Refinement of Degani 40-55)	**Process**	6,100,475	04/27/1998	Degani 41-56
44	Recessed Flip-Chip Package	**Structure**	6,154,370	07/21/1998	Degani 43-20-3
45	Translator for Recessed Flip-Chip Packages	**Structure**	6,160,715	09/08/1998	Degani 44-28-21-59
46	High Speed Flip-Chip Dispensing	**Equipment**	6,205,745	08/14/1998	Dudderar 29-2

Pending Patents	Category
3	**Design**
1	**Electrical Testing**
4	**Material**
4	**Material and Process**
3	**Process**
11	**Structure**
3	**Testing**

56	Circuit and Method for Providing Interconnections among Individual ...	**Design**	filed	04/09/1997	Gabara 38-48
64	Fabricating High-Q RF Component	**Design**	filed	03/02/1999	Frye 23-4-61
67	Thin-film monolithic coupled spiral balun transfomer	**Design**	filed	08/04/1999	Frye 25-1
66	Testing Integrated Circuits	**Electrical Testing**	filed	08/03/1999	Ahlquist 4-51-18-65
55	High Frequency Apparatus Including a Low-Loss Silicon Substrate	**Material**	filed	04/03/1997	Lau 8-3-44

57	Low Flux Process for Making Flip-Chip Assemblies	**Material**	filed	05/13/1997	Degani 33-22-11
58	Thin Film Capacitors and Process for Making Them	**Material**	filed	08/25/1997	Duenas 1-9-14-9-1-52
68	Article with Improved EMI Characteristics	**Material**	filed	09/22/1999	Dudderar 33-17-6
54	Method for Making Thin Film Tantalum Oxide Capacitors ... Product	**Material and Process**	filed	03/06/1997	Kola 8-47
60	Method of Making a High Frequency Apparatus Including a low Loss Substrate	**Material and Process**	filed	05/07/1998	Lau 10-8-57
62	Flip Chip Metallization (w J.A. Gregus)	**Material and Process**	filed	10/14/1998	Degani 46-4
74	Flip Chip Metallization	**Material and Process**	filed	09/14/2000	Degani 58-5
52	Integrated Circuit Bonding Method and Apparatus	**Process**	filed	05/01/1996	Degani 27-5
59	Improved Air Isolated Crossovers	**Process**	filed	10/08/1997	Kossives 12-21-53
63	Flip-Chip Bump Bonding	**Process**	filed	02/23/1999	Degani 48-15
47	Low Profile integrated Circuit Packages	**Structure**	allowed	10/22/1999	Degani 52-34-67
48	Interposer for Recessed Flip-Chip Packages	**Structure**	allowed 09/29/00	09/08/1998	Degani 45-30-22-60
51	Multi-level Stacked IC Chip Assembly	**Structure**	filed	12/28/1995	Degani 26-18-9
61	Packaging Silicon-on-Silicon MCMs (ZAP CARD)	**Structure**	filed	05/19/1998	Degani 42-26-58
65	Low-Cost Ball Grid Array Package (Silicon "Build-Up" BGA)	**Structure**	filed	07/01/1999	Degani 49-32-24
69	Cluster Packaging of IC Chips and Multi-Chip Packages	**Structure**	filed	11/22/1999	Gabara 76-3-14-66
70	High Performance Multi-Chip IC Package	**Structure**	filed	02/01/2000	Degani 54-35-69
71	Multi-Chip Ball Grid Array Package	**Structure**	filed	03/21/2000	Degani 55-36-70
72	Packaging Micromechanical Devices	**Structure**	filed	05/22/2000	Degani 56-37-71
73	Interconnecting Micromechanical Devices	**Structure**	filed	06/06/2000	Degani 57-38-72
76	Stacked Module Package	**Structure**	filed	12/27/2000	Degani 60-40-1-1
53	Manufacture of Printed Circuit Cards (Testing)	**Testing**	filed	02/28/1997	Degani 32-21-10-1
75	Method Of Testing And Constructing Monolithic Multi-Chip Modules	**Testing**	filed	12/22/2000	Degani 59-39-73
77	Method Of Making Semiconductor Apparatus Including Testing	**Testing**	filed	08/03/1999	Ahlquist 3-50-17-64

SyChip, Inc.
Copyrights

none per attorneys (Brobeck and Wilde)

Trademark actions: none

Trademark counsel:

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Dallas, TX 75201
Ph: 214.468.3708
Fax: 214.468.3704
email: jkrieser@brobeck.com

STATUS CHART OF
SYCHIP'S MARKS

Friday, August 09, 2002

Trademark List

Trademark Name	Country	Attorney(s			Classes	Agent	Status	Application Number	Registration	Renewal	First Use
COC	United States of America	RD	SA	AM	9	0000 USPTO	Allowed	76058023 19-May-2000			
MSIT	Canada	RD	SA	AM	9	FAS Fasken Martineau DuMoulin	Allowed	1062414 21-Aug-2000			
MSIT	China	RD	SA	AM	9	CCP CCPIT Patent & Trademark Ofc.	Registered	2000087247 19-Jun-2000	1618588 14-Aug-2001	13-Aug-201	
MSIT	Taiwan	RD	SA	AM	9	TAI Taiwan Int. Patent & Law Ofc.	Registered	89035292 20-Jun-2000	960146 16-Sep-2001	15-Sep-201	
SYCHIP	United States of America	RD	SA	AM	9	0000 USPTO	Registered	75651931 02-Mar-1999	2462417 19-Jun-2001	19-Jun-201	30-Sep-2000
SYCHIP	France	RD	SA	AM	9	CAB Cabinet Flechner	Registered	99771060 26-Jan-1999	99771060 02-Jul-1999	26-Jan-2009	
SYCHIP	Germany	RD	SA	AM	9, 38, 42	KU Kuhnen & Wacher	Registered	39967623 28-Oct-1999	39967623 09-Dec-1999	31-Oct-200	
SYCHIP	Japan	RD	SA	AM	9	OK Okabe International Patent Ofc	Registered	1113511 19-Feb-1999	4378854 21-Apr-2000	21-Apr-201	

TRADEMARK
REEL: 002595 FRAME: 0128

Trademark List

Trademark Name				Status	Application Number	Registration	Renewal	First Use
SYCHIP				Registered	99365	460537	10-Dec-200	
Country Korea, Republic of					11-Jan-1999	10-Dec-1999		
Attorney(s RD SA	AM	Classes 9	Agent: OK	Okabe International Patent Ofc				
SYCHIP				Registered	28799	T9900287J	13-Jan-2009	
Country Singapore					13-Jan-1999	13-Jan-1999		
Attorney(s RD SA	AM	Classes 9	Agent: DRE	Drew & Napier LLC				
SYCHIP				Registered	89020902	950044	15-Jul-2011	
Country Taiwan					17-Apr-2000	16-Jul-2001		
Attorney(s RD SA	AM	Classes 9	Agent: TAI	Taiwan Int. Patent & Law Ofc.				
SYCHIP				Registered	2192494	2192494	23-Mar-200	
Country United Kingdom					23-Mar-1999	24-Sep-1999		
Attorney(s RD SA	AM	Classes 9	Agent: GSC	The GSCP Partnership				

SyChip, Inc.
Copyrights

-none-