6-23-03

06-27-2003

RECC U.S. Department of Commerce
Patent and Trademark Office

102484587

To the Honorable Commissioner of Pat... original documents or copy thereof:

1. Name of conveying party(ies):

Schlumberger Technologies, Inc.

____ Individual ____ Association
____ General Partnership ____ Limited partnership
x Corporation, State of Delaware
____ Other: ____________________

Additional name(s) of conveying party(ies) attached?
____ Yes X No

2. Name and address of receiving party(ies):

Name: NPTest, LLC
Address: 150 Baytech Drive
San Jose, California 95134

Additional name(s) of receiving party(ies) attached?
____ Yes X No

3. Nature of Conveyance:
X Assignment ____ Merger
____ Security Agreement ____ Change of Name
____ Other: ________

Execution Date: 5/10/2002

4. Application Number(s) or Registration Number(s):

| A. Trademark Application Nos. | B. Trademark Registration Nos. |
|---|---|
| 75/195,095 | 1,759,075 |
| 76/081,008 | 1,774,080 |
| 76/284,263 | 1,813,447 |
| 76/333,767 | 1,837,767 |
| 76/340932 | 1,887,766 |
| 76/340933 | 2,099,862 |
| | 2,198,732 |
| | 2,252,458 |
| | 2,307,702 |
| | 2,345,915 |

Additional numbers attached: __ Yes _x_ No

5. Name and address of party to whom correspondence concerning this document should be mailed:

Name: Frederick D. Kim
Skadden, Arps, Slate, Meagher & Flom, LLP
Address: 525 University Avenue, Suite 1100
Palo Alto, CA 94301

6. Total no. of applications and registrations involved: 16

7. Total fee (37 C.F.R. § 3.41) ($40.00 per assignment): $40.00

X Enclosed a check for $640.00
____ The Commissioner is authorized to charge under-payment of any fees or credit any overpayment to Deposit Account Number:

8. Deposit Account Number: ____________

DO NOT USE THIS SPACE

9. Statement and signature.
To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Frederick D. Kim (signature) 6/23/03
Frederick D. Kim Date

Total number of pages including cover sheet, attachments and document: 26

Mail documents to be recorded with required cover sheet information to:

Commissioner of Patents and Trademarks
Box Assignments
Washington, D.C. 20231

06/26/2003 ECOOPER 00000124 75195095

01 FC:8521 40.00 OP
02 FC:8522 375.00 OP

Refund Ref: 06/26/2003 ECOOPER 00000128462
CHECK Refund Total: $225.00

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REEL: 002766 FRAME: 0166

**ACKNOWLEDGEMENT**
**OF**
**SCHLUMBERGER TECHNOLOGIES, INC.**

This Acknowledgement ("Acknowledgement") of Schlumberger Technologies, Inc., a Delaware corporation (the "Assignor") made, executed and delivered as of June 23, 2003 makes reference to that certain General Assignment and Assumption Agreement, dated as of May 10, 2002 and attached hereto as Annex 1 (the "Assignment"), by and between the Assignor and NPTest, LLC, a Delaware limited liability company, formerly Schlumberger Technology Solutions LLC ("NPT" or the "Assignee").

WITNESSETH:

WHEREAS, pursuant to the Assignment, Assignor granted, sold, conveyed, assigned and delivered to Assignee all of the assets described on Schedule 1 thereto, including but not limited to all of the intellectual property of the Semiconductor Solutions Group of Assignor relating to Assignor's Test, Probe and SABER business segments, the goodwill associated therewith, licenses and sublicenses granted and obtained with respect thereto, and rights thereunder, remedies against infringement thereof, and rights to protection of interests therein under the laws of all jurisdictions (the "Assigned IP");

WHEREAS, the Assignor desires to acknowledge that certain patents and patent applications owned by Assignor as of May 10, 2002 and listed on Schedule A hereto, including all inventions disclosed and/or claimed therein, all patents that may issue therefrom and the right to sue for past and future infringement thereof, are included in the Assigned IP that was assigned by the Assignor to the Assignee pursuant to the Assignment; and

WHEREAS, the Assignor desires to acknowledge that certain trademarks and service marks owned by Assignor as of May 10, 2002 and listed on Schedule B hereto, including the goodwill symbolized thereby and associated therewith, the registrations and applications for registration thereof, and the right to sue for past and future infringement thereof, are included in the Assigned IP that was assigned by the Assignor to the Assignee.

NOW THEREFORE, Assignor hereby acknowledges the following:

1. The patents and patent applications listed on Schedule A hereto, including all inventions disclosed and/or claimed therein, all patents that may issue therefrom and the right to sue for past and future infringement thereof, are included in the Assigned IP that was assigned by Assignor to NPT pursuant to the Assignment.

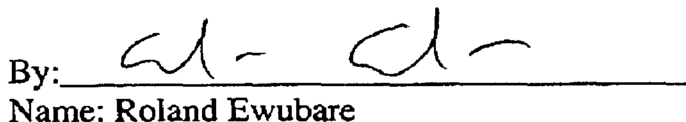
2. The trademarks and service marks listed on Schedule B hereto, including the goodwill symbolized thereby and associated therewith, the

registrations and applications for registration thereof, and the right to sue for past and future infringement thereof, are included in the Assigned IP that was assigned by the Assignor to NPT pursuant to the Assignment.

This instrument shall be construed and enforced in accordance with the laws of the State of Delaware (regardless of the laws that might be applicable under principles of conflicts of law) as to all matters, including but not limited to matters of validly, construction, effect and performance.

IN WITNESS WHEREOF, the undersigned, being a duly authorized officer of Assignor, has executed this Acknowledgement for and on behalf of Assignor as of this 23rd day of June 2003.

SCHLUMBERGER TECHNOLOGIES, INC.



By:____________________________
Name: Roland Ewubare



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REEL: 002766 FRAME: 0168

# Schedule A

Patents:

| Country | Patent No. | Grant Date | Appl. Date | Title | [illegible] |
|---|---|---|---|---|---|
| U.S. | 4,594,544 | 10-Jun-86 | 07-Mar-83 | PARTICIPATE REGISTER FOR PARALLEL LOADING PIN-ORIENTED REGISTERS IN TEST EQUIPMENT | 65.0081 |
| U.S. | 4,623,802 | 18-Nov-86 | 17-May-84 | MULTIPLE-STAGE GATE NETWORK HAVING INDEPENDENT REFERENCE VOLTAGE SOURCES | 65.0118 |
| U.S. | 4,651,038 | 17-Mar-87 | 17-May-84 | GATE HAVING TEMPERATURES-STABILIZED DELAY | 65.0117 |
| U.S. | 4,673,917 | 16-Jun-87 | 18-Jul-84 | METHOD AND APPARATUS FOR MINIMIZING DIGITAL-TO-ANALOG CONVERTER CORRECTION TRIMS | 65.0120 |
| U.S. | 4,706,019 | 10-Nov-87 | 15-Nov-85 | ELECTRON BEAM TEST PROBE SYSTEM FOR ANALYZING INTEGRATED CIRCUITS | 65.0132 |
| U.S. | 4,721,909 | 26-Jan-88 | 10-Feb-86 | APPARATUS FOR PULSING ELECTRON BEAMS | 65.0133 |
| U.S. | 4,795,984 | 03-Jan-89 | 19-Nov-86 | MULTI-MARKER, MULTI-DESTINATION TIMING SIGNAL GENERATOR | 65.0125 |
| U.S. | 4,864,228 | 05-Sep-89 | 16-Aug-85 | ELECTRON BEAM TEST PROBE FOR INTEGRATED CIRCUIT TESTING | 65.0135 |
| U.S. | 4,864,228 | 05-Sep-89 | 16-Aug-85 | ELECTRON BEAM TEST PROBE FOR INTEGRATED CIRCUIT TESTING | 65.0150 |
| U.S. | 4,910,698 | 20-Mar-90 | 12-Dec-88 | SINE WAVE GENERATOR USING A CORDIC ALGORITHM | 65.0128 |
| U.S. | 4,912,405 | 27-Mar-90 | 17-May-88 | MAGNETIC LENS AND ELECTRON BEAM DEFLECTION SYSTEM | 65.0135 |
| U.S. | 5,054,097 | 01-Oct-91 | 13-Nov-88 | METHODS AND APPARATUS FOR ALIGNMENT OF IMAGES | 65.0165 |
| U.S. | 5,091,693 | 25-Feb-92 | 13-Jul-90 | DUAL-SIDED TEST HEAD HAVING FLOATING CONTACT SURFACES | 65.0180 |
| U.S. | 5,122,988 | 16-Jun-92 | 17-Jul-91 | DATA STREAM SMOOTHING USING A FIFO MEMORY | 65.0172 |
| U.S. | 5,127,064 | 30-Jun-92 | 13-Feb-91 | HIGH RESOLUTION IMAGE COMPRESSION METHODS AND APPARATUS | 65.0164 |
| U.S. | 5,140,164 | 18-Aug-92 | 14-Jan-91 | IC MODIFICATION WITH FOCUSED ION BEAM | 65.0189 |
| U.S. | 5,144,225 | 01-Sep-92 | 25-Jul-91 | METHODS AND APPARATUS FOR ACQUIRING DATA FROM INTERMITTENTLY FAILING CIRCUITS | 65.0173 |
| U.S. | 5,210,487 | 11-May-93 | 04-Jun-91 | DOUBLE-GATED INTEGRATING SCHEME FOR ELECTRON BEAM TESTER | 65.0191 |
| U.S. | 5,212,443 | 18-May-93 | 05-Sep-90 | Event Sequencer for Automatic Test Equipment | 65.0148 |
| U.S. | 5,225,772 | 06-Jul-93 | 05-Sep-90 | AUTOMATIC TEST EQUIPMENT SYSTEM USING PIN SLICE ARCHITECTURE | 65.0168 |
| U.S. | 5,235,273 | 10-Aug-93 | 12-Jul-91 | APPARATUS FOR SETTING PIN DRIVER/SENSOR REFERENCE VOLTAGE LEVEL | 65.0194 |
| U.S. | 5,270,643 | 14-Dec-93 | 12-Aug-92 | PULSED LASER PHOTOEMISSION ELECTRON-BEAM PROBE | 65.0188 |

| [illegible] | [illegible] | [illegible] | [illegible] | [illegible] | [illegible] |
|---|---|---|---|---|---|
| U.S. | 5,287,022 | 15-Feb-94 | 24-Mar-93 | METHOD AND CIRCUIT FOR CONTROLLING VOLTAGE REFLECTIONS ON TRANSMISSION LINES | 65.0193 |
| U.S. | 5,357,116 | 18-Oct-94 | 23-Nov-92 | FOCUSED ION BEAM PROCESSING WITH CHARGE CONTROL | 65.0204 |
| U.S. | 5,392,222 | 21-Feb-95 | 30-Dec-91 | LOCATING A FIELD OF VIEW IN WHICH SELECTED IC CONDUCTORS ARE UNOBSCURED | 65.0184 |
| U.S. | 5,401,972 | 28-Mar-95 | 02-Sep-93 | LAYOUT OVERLAY FOR FIB OPERATIONS | 65.0210 |
| U.S. | 5,430,400 | 04-Jul-95 | 03-Aug-93 | DRIVER CIRCUITS FOR IC TESTER | 65.0209 |
| U.S. | 5,461,310 | 24-Oct-95 | 28-Jun-94 | AUTOMATIC TEST EQUIPMENT SYSTEM USING PIN SLICE ARCHITECTURE | 65.0168 |
| U.S. | 5,475,624 | 12-Dec-95 | 30-Apr-92 | TEST GENERATION BY ENVIRONMENT EMULATION | 65.0192 |
| U.S. | 5,477,139 | 19-Dec-95 | 13-May-93 | Event Sequencer for Automatic Test Equipment | 65.0148 |
| U.S. | 5,481,550 | 02-Jan-96 | 12-Oct-93 | APPARATUS FOR MAINTAINING STIMULATION TO A DEVICE UNDER TEST AFTER A TEST STOPS | 65.0203 |
| U.S. | 5,530,372 | 25-Jun-96 | 15-Apr-94 | METHOD OF PROBING A NET OF AN IC AT AN OPTIMAL PROBE-POINT | 65.0211 |
| U.S. | 5,604,819 | 18-Feb-97 | 15-Mar-93 | DETERMINING OFFSET BETWEEN IMAGES OF AN IC | 65.0202 |
| U.S. | 5,616,921 | 01-Apr-97 | 30-Jun-94 | SELF-MASKING FIB MILLING | 65.0207 |
| U.S. | 5,638,005 | 10-Jun-97 | 08-Jun-95 | Predictive Waveform Acquistion | 65.0216 |
| U.S. | 5,646,521 | 08-Jul-97 | 01-Aug-95 | ANALOG CHANNEL FOR MIXED-SIGNAL-VLSI TESTER | 65.0222 |
| U.S. | 5,654,657 | 05-Aug-97 | 01-Aug-95 | ACCURATE ALIGNMENT OF CLOCKS IN MIXED-SIGNAL TESTER | 65.0228 |
| U.S. | 5,673,275 | 30-Sep-97 | 13-Aug-96 | ACCELERATED MODE TESTER TIMING | 65.0220 |
| U.S. | 5,675,499 | 07-Oct-97 | 02-Apr-96 | METHOD OF PROBING A NET OF AN IC AT AN OPTIMAL PROBE-POINT | 65.0211 |
| U.S. | 5,700,526 | 23-Dec-97 | 04-May-95 | INSULATOR DEPOSITION USING FOCUSED ION BEAM | 65.0234 |
| U.S. | 5,731,984 | 28-Mar-98 | 17-Jul-95 | VECTOR-BASED WAFEFORM ACQUISITION AND DISPLAY | 65.0239 |
| U.S. | 5,745,003 | 28-Apr-98 | 11-Sep-96 | DRIVER CIRCUITS FOR IC TESTER | 65.0243 |
| U.S. | 5,747,818 | 05-May-98 | 21-Oct-96 | THERMOELECTRIC COOLING GAS-ASSISTED FIB SYSTEM | 65.0245 |
| U.S. | 5,748,124 | 05-May-98 | 09-Dec-96 | ANALOG CHANNEL FOR MIXED-SIGNAL-VLSI TESTER | 65.0222 |
| U.S. | 5,821,549 | 13-Oct-98 | 03-Mar-97 | Through the Substrate Investigation of Flip-Chip ICs | 65.0246 |
| U.S. | 5,840,630 | 24-Nov-98 | 20-Dec-96 | FIB ETCHING ENHANCED WITH 1,2 DI-IODO-ETHANE | 65.0244 |
| U.S. | 5,883,905 | 16-Mar-99 | 18-Feb-97 | PATTERN GENERATOR WITH EXTENDED REGISTER PROGRAMMING | 65.0266 |
| U.S. | 5,892,949 | 06-Apr-99 | 30-Aug-96 | ATE TEST PROGRAMMING ARCHITECTURE | 65.0233 |
| U.S. | 5,905,266 | 18-May-99 | 19-Dec-96 | CHARGED PARTICLE BEAM SYSTEM WITH OPTICAL MICROSCOPE | 65.0248 |
| U.S. | 5,905,577 | 18-May-99 | 15-Mar-97 | DUAL-LASER VOLTAGE PROBING OF IC'S | 65.0261 |
| U.S. | 5,913,022 | 15-Jun-99 | 15-Dec-95 | LOADING HARDWARE PATTERN MEMORY IN AUTOMATIC TEST EQUIPMENT FOR | 65.0231 |

| Country | Patent # | Grant Date | Appl. Date | Title | [illegible] |
|---|---|---|---|---|---|
| | | | | TESTING CIRCUITS | |
| U.S. | 5,918,198 | 29-Jun-99 | 22-Oct-96 | GENERATING PULSES IN ANALOG CHANNEL OF ATE TESTER | 65.0252 |
| U.S. | 5,920,073 | 06-Jul-99 | 22-Apr-97 | OPTICAL SYSTEM WITH AN AXIALLY MOVEABLE APERTURED PLATE | 65.0262 |
| U.S. | 5,944,846 | 31-Aug-99 | 30-Sep-97 | Method and Apparatus for Selectively Testing Identical Pins of a Plurality of Electronic Components | 65.0238 |
| U.S. | 5,959,458 | 28-Sep-99 | 08-Nov-96 | METHOD AND APPARATUS FOR MEASURING ELECTRICAL WAVEFORMS USING ATOMIC FORCE MICROSCOPY | 65.0253 |
| U.S. | 5,996,099 | 30-Nov-99 | 30-Sep-97 | METHOD AND APPARATUS FOR AUTOMATICALLY TESTING ELECTRONIC COMPONENTS IN PARALLEL UTILIZING DIFFERENT TIMING SIGNALS FOR EACH ELECTRONIC COMPONENT | 65.0236 |
| U.S. | 6,006,346 | 21-Dec-99 | 14-May-97 | Method and Equipment for Automatically Testing Electronic Components | 65.0221 |
| U.S. | 6,014,764 | 11-Jan-00 | 20-May-97 | PROVIDING TEST VECTORS WITH PATTERN CHAINING DEFINITION | 65.0254 |
| U.S. | 6,031,229 | 29-Feb-00 | 20-May-98 | AUTOMATIC SEQUENCING OF FIB OPERATIONS | 65.0269 |
| U.S. | 6,049,900 | 11-Apr-00 | 30-Sep-97 | AUTOMATIC PARALLEL ELECTRONIC COMPONENT TESTING METHOD AND EQUIPMENT | 65.0237 |
| U.S. | 6,061,815 | 09-May-00 | 09-Dec-96 | PROGRAMMING UTILITY REGISTER TO GENERATE ADDRESSES IN ALGORITHMIC PATTERN GENERATOR | 65.0247 |
| U.S. | 6,078,845 | 20-Jun-00 | 25-Nov-96 | APPARATUS FOR CARRYING SEMICONDUCTOR DEVICES | 65.0257 |
| U.S. | 6,081,484 | 27-Jun-00 | 14-Oct-97 | Measuring Signals in a Tester System | 65.0274 |
| U.S. | 6,128,754 | 03-Oct-00 | 24-Nov-97 | AUTOMATIC CIRCUIT TESTER HAVING A WAVEFORM ACQUISITION MODE OF OPERATION | 65.0271 |
| U.S. | 6,181,117 | 30-Jan-01 | 25-Oct-99 | POWER SUPPLY CIRCUIT OF AN ELECTRONIC COMPONENT IN A TEST MACHINE | 65.0264 |
| U.S. | 6,225,626 | 01-May-01 | 30-Sep-98 | Through the Substrate Investigation of Flip-Chip ICs | 65.0246 |
| U.S. | 6,252,222 | 26-Jun-01 | 13-Jan-00 | Differential Pulsed Laser Beam Probing of Integrated Circuits | 65.0312 |
| U.S. | 6,263,464 | 17-Jul-01 | 22-Apr-99 | DEVICE FOR CONTROLLING CONFORMITY OF CONSUMPTION OF AN ELECTRONIC COMPONENT IN A TESTING MACHINE | 65.0263 |
| U.S. | 6,285,963 | 04-Sep-01 | 30-Nov-99 | Measuring Signals in a Tester System | 65.0274 |
| U.S. | 6,410,924 | 25-Jun-02 | 16-Nov-99 | Energy Filtered Focused Ion Beam Column | 65.0281 |
| U.S. | 6,420,888 | 16-Jul-02 | 29-Sep-00 | Test Interface Module | 65.0339 |
| U.S. | 6,462,814 | 08-Oct-02 | 15-Mar-00 | BEAM DELIVERY AND IMAGING FOR OPTICAL PROBING OF A DEVICE OPERATING UNDER ELECTRICAL TEST | 65.0267 |
| U.S. | 6,492,797 | 10-Dec-02 | 28-Feb-00 | Socket Calibration Method and Apparatus | 65.0302 |

| [illegible] | [illegible] | [illegible] | [illegible] | [illegible] | [illegible] |
|---|---|---|---|---|---|
| U.S. | 6,496,261 | 17-Dec-02 | 08-Feb-00 | Double-Pulsed Optical Interferometer for Waveform Probing of Integrated Circuits | 65.0316 |
| U.S. | 6,496,953 | 17-Dec-02 | 15-Mar-00 | Calibration Method and Apparatus for Correcting Pulse Width Timing Erros in Integrated Circuit Testing | 65.0307 |
| U.S. | 6,501,706 | 31-Dec-02 | 22-Aug-00 | TIME-TO-DIGITAL CONVERTER | 65.0296 |
| U.S. | 6,501,288 | 31-Dec-02 | 28-Sep-00 | On-Chip Optically Triggered Latch for IC Time Measurements | 65.0324 |
| U.S. | 6,514,866 | 04-Feb-03 | 31-May-01 | Chemical Enhanced Forcused Ion Beam Micro-Machining of Copper | 65.0345 |
| U.S. | 6,518,571 | 11-Feb-03 | 10-Feb-01 | Through the Substrate Investigation of Flip-Chip ICs | 65.0246 |
| U.S. | 6,522,162 | 18-Feb-03 | 24-Apr-02 | Test System Having Interface Module | 65.0339 |
| U.S. | 6,553,522 | 22-Apr-03 | 22-Feb-00 | Valuation of Tester Accuracy | 65.0303 |
| Canada | 1256587 | 27-Jun-89 | 10-Nov-86 | ELECTRON BEAM TEST PROBE SYSTEM FOR ANALYZING INTEGRATED CIRCUITS | 65.0132 |
| Canada | 1256597 | 27-Jun-89 | 06-Feb-87 | APPARATUS FOR PULSING ELECTRON BEAMS | 65.0133 |
| Canada | 1271997 | 24-Jul-90 | 14-Mar-86 | ELECTRON BEAM TEST PROBE FOR INTEGRATED CIRCUIT TESTING | 65.0150 |
| France | 8308129 | 28-Jul-86 | 17-May-83 | Test System Memory Architecture for Passing | 65.0077 |
| France | 0390675 | 12-Apr-95 | 28-Mar-90 | METHODS AND APPARATUS FOR ACQUIRING DATA FROM INTERMITTENTLY FAILING CIRCUITS | 65.0173 |
| France | 0599367 | 15-May-96 | 02-Nov-93 | FOCUSED ION BEAM PROCESSING WITH CHARGE CONTROL | 65.0204 |
| France | 0492677 | 12-Jun-96 | 24-Oct-91 | PULSED LASER PHOTOEMISSION ELECTRON-BEAM PROBE | 65.0188 |
| France | FR91 08845 | 12-Jul-96 | 12-Jul-91 | DUAL-SIDED TEST HEAD HAVING FLOATING CONTACT SURFACES | 65.0180 |
| France | 0474275 | 15-Jan-97 | 12-Aug-91 | AUTOMATIC TEST EQUIPMENT SYSTEM USING PIN SLICE ARCHITECTURE | 65.0168 |
| France | 0474274 | 02-Apr-97 | 12-Aug-91 | Event Sequencer for Automatic Test Equipment | 65.0148 |
| France | 0517294 | 02-Jul-97 | 20-May-92 | DOUBLE-GATED INTEGRATING SCHEME FOR ELECTRON BEAM TESTER | 65.0191 |
| France | 0370323 | 09-Jul-97 | 09-Nov-89 | HIGH RESOLUTION IMAGE COMPRESSION METHODS AND APPARATUS | 65.0164 |
| France | 2738640 | 31-Oct-97 | 12-Sep-96 | ACCELERATED MODE TESTER TIMING | 65.0220 |
| France | 2756380 | 29-May-98 | 25-Nov-96 | DEVICE FOR CONTROLLING CONFIRMITY OF CONSUMPTION OF AN ELECTRONIC COMPONENT IN A TESTING MACHINE | 65.0263 |
| France | 0370322 | 08-Jul-98 | 09-Nov-89 | METHODS AND APPARATUS FOR ALIGNMENT OF IMAGES | 65.0165 |
| France | 2737620 | 07-Aug-98 | 01-Aug-96 | ACCURATE ALIGNMENT OF CLOCKS IN MIXED-SIGNAL TESTER | 65.0228 |
| France | 0 800676 | 19-Aug-98 | 20-Dec-95 | Method and Equipment for Automatically Testing Electronic Components | 65.0221 |
| France | 2709351 | 30-Oct-98 | 02-Aug-94 | DRIVER CIRCUITS FOR IC TESTER | 65.0209 |
| France | 2753273 | 22-Jan-99 | 08-Sep-97 | DRIVER CIRCUITS FOR IC TESTER | 65.0243 |
| France | 2759460 | 16-Apr-99 | 13-Feb-97 | POWER SUPPLY CIRCUIT OF AN ELECTRONIC COMPONENT IN A TEST MACHINE | 65.0264 |



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| [illegible] | [illegible] | [illegible] | [illegible] | [illegible] | [illegible] |
|---|---|---|---|---|---|
| France | 0619551 | 12-Jan-00 | 07-Mar-94 | DETERMINING OFFSET BETWEEN IMAGES OF AN IC | 65.0202 |
| France | 0855734 | 29-Nov-00 | 10-Dec-97 | FIB ETCHING ENHANCED WITH 1,2 DI-IODO-ETHANE | 65.0244 |
| France | 2781066 | 02-May-02 | 09-Jul-98 | SECURING DATA IN A MACHINE FOR TESTING ELECTRONIC COMPONENTS | 65.0291 |
| France | 2806527 | 25-Oct-02 | 20-Mar-00 | Column Simultaneously Focusing a Particle Beam and an Optical Beam | 65.0290 |
| France | 2779009 | 03-Jan-03 | 10-May-02 | AUTOMATIC SEQUENCING OF FIB OPERATIONS | 65.0269 |
| Germany | 0599367 | 15-May-96 | 02-Nov-93 | FOCUSED ION BEAM PROCESSING WITH CHARGE CONTROL | 65.0204 |
| Germany | 69120233.8 | 12-Jun-96 | 24-Oct-91 | PULSED LASER PHOTOEMISSION ELECTRON-BEAM PROBE | 65.0188 |
| Germany | 0517294 | 02-Jul-97 | 20-May-92 | DOUBLE-GATED INTEGRATING SCHEME FOR ELECTRON BEAM TESTER | 65.0191 |
| Germany | P3688612.2 | 09-Jul-97 | 09-Nov-89 | HIGH RESOLUTION IMAGE COMPRESSION METHODS AND APPARATUS | 65.0164 |
| Germany | 3317593 | 20-May-98 | 14-May-83 | Test System Memory Architecture for Passing | 65.0077 |
| Germany | 68928726 | 08-Jul-98 | 09-Nov-89 | METHODS AND APPARATUS FOR ALIGNMENT OF IMAGES | 65.0165 |
| Germany | 69422539.8-08 | 12-Jan-00 | 07-Mar-94 | DETERMINING OFFSET BETWEEN IMAGES OF AN IC | 65.0202 |
| Germany | 69703611.1 | 29-Nov-00 | 10-Dec-97 | FIB ETCHING ENHANCED WITH 1,2 DI-IODO-ETHANE | 65.0244 |
| Germany | 19629869 | 13-Feb-03 | 24-Jul-96 | ACCURATE ALIGNMENT OF CLOCKS IN MIXED-SIGNAL TESTER | 65.0228 |
| Italy | 0599367 | 15-May-96 | 02-Nov-93 | FOCUSED ION BEAM PROCESSING WITH CHARGE CONTROL | 65.0204 |
| Italy | 0474275 | 15-Jan-97 | 12-Aug-91 | AUTOMATIC TEST EQUIPMENT SYSTEM USING PIN SLICE ARCHITECTURE | 65.0168 |
| Italy | 0517294 | 02-Jul-97 | 20-May-92 | DOUBLE-GATED INTEGRATING SCHEME FOR ELECTRON BEAM TESTER | 65.0191 |
| Italy | 0619551 | 12-Jan-00 | 07-Mar-94 | DETERMINING OFFSET BETWEEN IMAGES OF AN IC | 65.0202 |
| Japan | 1988075 | 08-Nov-95 | 13-Feb-91 | HIGH RESOLUTION IMAGE COMPRESSION METHODS AND APPARATUS | 65.0164 |
| Japan | 2581815 | 21-Nov-96 | 24-Nov-89 | METHODS AND APPARATUS FOR ALIGNMENT OF IMAGES | 65.0165 |
| Japan | 2864647 | 18-Dec-98 | 28-Jun-94 | SELF-MASKING FIB MILLING | 65.0207 |
| Japan | 3115108 | 29-Sep-00 | 13-Jul-92 | APPARATUS FOR SETTING PIN DRIVER/SENSOR REFERENCE VOLTAGE LEVEL | 65.0194 |
| Japan | 3169232 | 16-Mar-01 | 02-Jul-91 | DUAL-SIDED TEST HEAD HAVING FLOATING CONTACT SURFACES | 65.0180 |
| Japan | 3220480 | 10-Aug-01 | 04-Sep-91 | Event Sequencer for Automatic Test Equipment | 65.0148 |
| Japan | 3263503 | 21-Dec-01 | 22-Nov-93 | FOCUSED ION BEAM PROCESSING WITH CHARGE CONTROL | 65.0204 |
| Japan | 3298653 | 19-Apr-02 | 04-Sep-91 | AUTOMATIC TEST EQUIPMENT SYSTEM USING PIN SLICE ARCHITECTURE | 65.0168 |
| Netherlands | 0599367 | 15-May-96 | 02-Nov-93 | FOCUSED ION BEAM PROCESSING WITH CHARGE CONTROL | 65.0204 |



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REEL: 002766 FRAME: 0173

| [illegible] | [illegible] | Grant Date | Appl. Date | Title | [illegible] |
|---|---|---|---|---|---|
| Netherlands | 0474275 | 15-Jan-97 | 12-Aug-91 | AUTOMATIC TEST EQUIPMENT SYSTEM USING PIN SLICE ARCHITECTURE | 65.0168 |
| Netherlands | 0517294 | 02-Jul-97 | 20-May-92 | DOUBLE-GATED INTEGRATING SCHEME FOR ELECTRON BEAM TESTER | 65.0191 |
| Netherlands | 0370322 | 08-Jul-98 | 09-Nov-89 | METHODS AND APPARATUS FOR ALIGNMENT OF IMAGES | 65.0165 |
| Netherlands | 0619551 | 12-Jan-00 | 07-Mar-94 | DETERMINING OFFSET BETWEEN IMAGES OF AN IC | 65.0202 |
| Taiwan | NI-092318 | 13-May-98 | 08-Jun-96 | Predictive Waveform Acquistion | 65.0216 |
| Taiwan | NI-093673 | 24-Jul-98 | 10-Jul-97 | METHOD AND APPARATUS FOR MEASURING ELECTRICAL WAVEFORMS USING ATOMIC FORCE MICROSCOPY | 65.0253 |
| Taiwan | NI-096415 | 08-Dec-98 | 16-Jul-97 | GENERATING PULSES IN ANALOG CHANNEL OF ATE TESTER | 65.0252 |
| Taiwan | NI-098099 | 15-Mar-99 | 28-Jul-97 | DRIVER CIRCUITS FOR IC TESTER | 65.0243 |
| Taiwan | 105657 | 11-Jun-99 | 03-Mar-98 | POWER SUPPLY CIRCUIT OF AN ELECTRONIC COMPONENT IN A TEST MACHINE | 65.0264 |
| Taiwan | NI-104487 | 01-Jul-99 | 20-Jan-98 | METHOD AND APPARATUS FOR GENERATING SPLIT TIMING TEST SIGNALS FOR INTEGRATED CIRCUIT TESTING | 65.0268 |
| Taiwan | NI-107526 | 01-Oct-99 | 05-Feb-98 | PATTERN GENERATOR WITH EXTENDED REGISTER PROGRAMMING | 65.0266 |
| Taiwan | NI-103668 | 05-Oct-99 | 03-Dec-97 | PROGRAMMING UTILITY REGISTER TO GENERATE ADDRESSES IN ALGORITHMIC PATTERN GENERATOR | 65.0247 |
| Taiwan | NI-109360 | 10-Apr-00 | 11-Nov-97 | FIB ETCHING ENHANCED WITH 1,2 DI-IODO-ETHANE | 65.0244 |
| Taiwan | NI-109540 | 13-Apr-00 | 21-Oct-97 | APPARATUS FOR CARRYING SEMICONDUCTOR DEVICES | 65.0257 |
| Taiwan | NI-109745 | 18-Apr-00 | 23-Mar-98 | PROVIDING TEST VECTORS WITH PATTERN CHAINING DEFINITION | 65.0254 |
| Taiwan | NI-120890 | 01-Oct-00 | 13-Oct-98 | AUTOMATIC CIRCUIT TESTER HAVING A WAVEFORM ACQUISITION MODE OF OPERATION | 65.0271 |
| Taiwan | NI-121589 | 21-Oct-00 | 30-Jul-97 | CHARGED PARTICLE BEAM SYSTEM WITH OPTICAL MICROSCOPE | 65.0248 |
| Taiwan | NI-142848 | 21-Oct-01 | 13-Oct-98 | MEASURING SIGNALS IN A TESTER SYSTEM | 65.0274 |
| Taiwan | 159509 | 11-Jul-02 | 14-Sep-01 | Compact, High Collection Efficiency Scinitillator for Secondary Electron Detection | 65.0322 |
| Taiwan | 161277 | 11-Aug-02 | 15-Mar-01 | BEAM DELIVERY AND IMAGING FOR OPTICAL PROBING OF A DEVICE OPERATING UNDER ELECTRICAL TEST | 65.0267 |
| Taiwan | 090123901 | 11-Aug-02 | 27-Sep-01 | Method and Apparatus for Remotely Testing Semiconductor | 65.0340 |
| U.K. | 2121550B | 18-Dec-85 | 17-May-83 | Test System Memory Architecture for Passing | 65.0077 |
| U.K. | 0390675 | 12-Apr-95 | 28-Mar-90 | METHODS AND APPARATUS FOR ACQUIRING DATA FROM INTERMITTENTLY FAILING CIRCUITS | 65.0173 |
| U.K. | 0599367 | 15-May-96 | 02-Nov-93 | FOCUSED ION BEAM PROCESSING WITH CHARGE CONTROL | 65.0204 |

| [illegible] | [illegible] | [illegible] | [illegible] | [illegible] | [illegible] |
|---|---|---|---|---|---|
| U.K. | 0474275 | 15-Jan-97 | 12-Aug-91 | AUTOMATIC TEST EQUIPMENT SYSTEM USING PIN SLICE ARCHITECTURE | 65.0168 |
| U.K. | 0474274 | 02-Apr-97 | 12-Aug-91 | Event Sequencer for Automatic Test Equipment | 65.0148 |
| U.K. | 0517294 | 02-Jul-97 | 20-May-92 | DOUBLE-GATED INTEGRATING SCHEME FOR ELECTRON BEAM TESTER | 65.0191 |
| U.K. | 2300515 | 09-Jul-97 | 17-Apr-96 | INSULATOR DEPOSITION USING FOCUSED ION BEAM | 65.0234 |
| U.K. | 0370322 | 08-Jul-98 | 09-Nov-89 | METHODS AND APPARATUS FOR ALIGNMENT OF IMAGES | 65.0165 |
| U.K. | 0 800676 | 19-Aug-98 | 20-Dec-95 | Method and Equipment for Automatically Testing Electronic Components | 65.0221 |
| U.K. | 0855734 | 29-Nov-00 | 10-Dec-97 | FIB ETCHING ENHANCED WITH 1,2 DI-IODO-ETHANE | 65.0244 |

Patent Applications:

| [illegible] | [illegible] | [illegible] | [illegible] | [illegible] |
|---|---|---|---|---|
| U.S. | 09/350,611 | 7/9/99 | SECURING DATA IN A MACHINE FOR TESTING ELECTRONIC COMPONENTS | 65.0291 |
| U.S. | 09/410,569 | 10/1/99 | Test Method and Apparatus for Source Synchronous Signals | 65.0309 |
| U.S. | 09/419,317 | 10/17/99 | Measuring Jitter of High-Speed Data Channels | 65.0299 |
| U.S. | 09/421,784 | 10/19/99 | Packet-Based Device Test System | 65.0306 |
| U.S. | 09/628,116 | 7/28/00 | Superconducting Single Photon Detector | 65.0332 |
| U.S. | 09/648,716 | 8/25/00 | Edge Placement and Jitter Measurement for Electronic Elements | 65.0297 |
| U.S. | 09/676,292 | 9/28/00 | Method and Apparatus for Remotely Testing Semiconductor | 65.0340 |
| U.S. | 09/675,981 | 9/29/00 | Compact, High Collection Efficiency Scinitillator for Secondary Electron Detection | 65.0322 |
| U.S. | 09/679,042 | 10/2/00 | Method and Apparatus for High Speed IC Test Interface | 65.0337 |
| U.S. | 09/696,102 | 10/24/00 | Scan Stream Sequencing for Testing Integrated Circuits | 65.0321 |
| U.S. | 09/746,618 | 12/21/00 | Optical Coupling for Testing Integrated Circuits | 65.0329 |
| U.S. | 09/924,736 | 8/7/01 | Method for Global Die Thinning and Polishing of Flip-Chip Packaged Integrated Circuits | 65.0338 |
| U.S. | 10/004,018 | 10/18/01 | Photoconductive-Sampling Voltage Measurement | 65.0272 |
| U.S. | 10/056,287 | 1/23/02 | Circuit and Method for Distributing Events in an Event Stream | 65.0363 |
| U.S. | 10/057,134 | 1/24/02 | Comparator Circuit for Differential Swing Comparison and Common-Mode Voltage Comparison | 65.0364 |
| U.S. | 10/066,123 | 1/30/02 | PICA System Timing Measurement & Calibration | 65.0372 |
| U.S. | 10/079,780 | 2/19/02 | PICA System Detector Calibration | 65.0373 |
| U.S. | 10/101,564 | 3/18/02 | Test System Formatters | 65.0348 |
| U.S. | 10/102,526 | 3/19/02 | Test System Algorithmic Program Generators | 65.0350 |
| U.S. | 10/106,280 | 3/25/02 | Method and Apparatus for Socket Calibration of Integrated Circuit Testers | 65.0352 |
| U.S. | 10/123,842 | 4/15/02 | Measuring Back-Side Voltage of an Integrated Circuit | 65.0354 |
| U.S. | 10/421,059 | 4/23/02 | Method for Backside Die Thinning and Polishing of Packaged Integrated Circuits | 65.0338 |
| U.S. | 10/136,710 | 4/30/02 | Open-Loop for Waveform Acquisition | 65.0355 |
| China | 01141510.X | 9/28/01 | Method and Apparatus for Remotely Testing Semiconductor | 65.0340 |
| EC | 96201465.0 | 5/28/96 | Predictive Waveform Acquistion | 65.0216 |
| EC | 97/402304.6 | 10/1/97 | THERMOELECTRIC COOLING GAS-ASSISTED FIB SYSTEM | 65.0245 |
| EC | 97402305.3 | 10/1/97 | METHOD AND APPARATUS FOR MEASURING ELECTRICAL WAVEFORMS USING ATOMIC FORCE MICROSCOPY | 65.0253 |
| EC | 97/402535.5 | 10/24/97 | CHARGED PARTICLE BEAM SYSTEM WITH OPTICAL MICROSCOPE | 65.0248 |
| EC | 97402533.0 | 10/24/97 | APPARATUS FOR CARRYING SEMICONDUCTOR DEVICES | 65.0257 |
| EC | 98/400378.0 | 2/17/98 | PATTERN GENERATOR WITH EXTENDED REGISTER PROGRAMMING | 65.0266 |
| EC | 98/400441.6 | 2/23/98 | Through the Substrate Investigation of Flip-Chip ICs | 65.0246 |
| EC | 98/400562.9 | 3/10/98 | DUAL-LASER VOLTAGE PROBING OF IC'S | 65.0261 |
| EC | 98400789.8 | 4/2/98 | Optical System with an Axially Moveable Apertured Plate | 65.0262 |
| EC | 98401017.3 | 4/24/98 | PROVIDING TEST VECTORS WITH PATTERN CHAINING DEFINITION | 65.0254 |

| [illegible] | [illegible] | [illegible] | [illegible] | [illegible] |
|---|---|---|---|---|
| EC | 98402555.1 | 10/14/98 | MEASURING SIGNALS IN A TESTER SYSTEM | 65.0274 |
| EC | 98402769.8 | 11/6/98 | AUTOMATIC CIRCUIT TESTER HAVING A WAVEFORM ACQUISITION MODE OF OPERATION | 65.0271 |
| EC | 01925126.3 | 3/15/01 | BEAM DELIVERY AND IMAGING FOR OPTICAL PROBING OF A DEVICE OPERATING UNDER ELECTRICAL TEST | 65.0267 |
| EC | 01204103.4 | 10/30/01 | Method and Apparatus for Remotely Testing Semiconductor | 65.0340 |
| France | 94/07913 | 6/28/94 | SELF-MASKING FIB MILLING | 65.0207 |
| France | 94/10272 | 8/23/94 | LAYOUT OVERLAY FOR FIB OPERATIONS | 65.0210 |
| France | 96/05206 | 4/23/96 | INSULATOR DEPOSITION USING FOCUSED ION BEAM | 65.0234 |
| France | 96/09712 | 8/1/96 | ANALOG CHANNEL FOR MIXED-SIGNAL-VLSI TESTER | 65.0222 |
| France | 97/12223 | 10/1/97 | GENERATING PULSES IN ANALOG CHANNEL OF ATE TESTER | 65.0252 |
| France | 0012079 | 9/22/00 | Double-Pulsed Optical Interferometer for Waveform Probing of Integrated Circuits | 65.0316 |
| France | 0012525 | 10/2/00 | Test Method and Apparatus for Source Synchronous Signals | 65.0309 |
| France | 0100299 | 1/11/01 | Differential Pulsed Laser Beam Probing of Integrated Circuits | 65.0312 |
| France | 0101366 | 1/31/01 | Electric Feeding Device for a Test Installation of Components | 65.0353 |
| France | 0103388 | 3/13/01 | Calibration Method and Apparatus for Correcting Pulse Width Timing Erros in Integrated Circuit Testing | 65.0307 |
| France | 0110076 | 7/27/01 | Superconducting Single Photon Detector | 65.0332 |
| France | 0110993 | 8/22/01 | TIME-TO-DIGITAL CONVERTER | 65.0296 |
| France | 0111093 | 8/24/01 | EDGE PLACEMENT AND JITTER MEASUREMENT FOR ELECTRONIC ELEMENTS | 65.0297 |
| France | 0112423 | 9/27/01 | On-Chip Optically Triggered Latch for IC Time Measurements | 65.0324 |
| France | 0112506 | 9/28/01 | Compact, High Collection Efficiency Scinitillator for Secondary Electron Detection | 65.0322 |
| France | 0113588 | 10/22/01 | Scan Stream Sequencing for Testing Integrated Circuits | 65.0321 |
| France | 0112656 | 10/26/01 | Method and Apparatus for High Speed IC Test Interface | 65.0337 |
| France | 0116591 | 12/20/01 | Optical Coupling for Testing Integrated Circuits | 65.0329 |
| France | 02 03575 | 3/22/02 | Method and Apparatus for Socket Calibration of Integrated Circuit Testers | 65.0352 |
| Germany | P4414295.1 | 4/23/94 | APPARATUS FOR MAINTAINING STIMULATION TO A DEVICE UNDER TEST AFTER A TEST STOPS | 65.0203 |
| Germany | P4421517.7 | 6/20/94 | SELF-MASKING FIB MILLING | 65.0207 |
| Germany | P 4426538.7 | 7/27/94 | Driver Circuits for IC Tester | 65.0209 |
| Germany | P4430456.0 | 8/27/94 | LAYOUT OVERLAY FOR FIB OPERATIONS | 65.0210 |
| Germany | 19513819.8 | 4/12/95 | METHOD OF PROBING A NET OF AN IC AT AN OPTIMAL PROBE-POINT | 65.0211 |
| Germany | 19617027.3 | 4/27/96 | INSULATOR DEPOSITION USING FOCUSED ION BEAM | 65.0234 |
| Germany | 19631005.9 | 8/1/96 | ANALOG CHANNEL FOR MIXED-SIGNAL-VLSI TESTER | 65.0222 |
| Germany | 19636881.2 | 9/11/96 | ACCELERATED MODE TESTER TIMING | 65.0220 |
| Germany | 19627056.1 | 7/5/97 | VECTOR-BASED WAFEFORM ACQUISITION AND DISPLAY | 65.0239 |
| Germany | 19922653.9 | 5/18/99 | AUTOMATIC SEQUENCING OF FIB OPERATIONS | 65.0269 |
| Germany | 19931047.5 | 7/6/99 | SECURING DATA IN A MACHINE FOR TESTING ELECTRONIC COMPONENTS | 65.0291 |
| Germany | 19950506.3 | 10/20/99 | MEASURING JITTER OF HIGH-SPEED DATA CHANNELS | 65.0299 |
| Germany | 10047136.6 | 9/22/00 | Double-Pulsed Optical Interferometer for Waveform Probing of Integrated Circuits | 65.0316 |
| Germany | 10048895.1 | 10/2/00 | Test Method and Apparatus for Source Synchronous Signals | 65.0309 |



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| Germany | 10100816.3 | 1/10/01 | Differential Pulsed Laser Beam Probing of Integrated Circuits | 65.0312 |
| Germany | 10109385.3 | 2/27/01 | Socket Calibration Method and Apparatus | 65.0302 |
| Germany | 10112311.6 | 3/14/01 | Calibration Method and Apparatus for Correcting Pulse Width Timing Erros in Integrated Circuit Testing | 65.0307 |
| Germany | 01919529.6 | 3/19/01 | Column Simultaneously Focusing a Particle Beam and an Optical Beam | 65.0290 |
| Germany | 10141070.0 | 8/22/01 | TIME-TO-DIGITAL CONVERTER | 65.0296 |
| Germany | 10141523.0 | 8/24/01 | EDGE PLACEMENT AND JITTER MEASUREMENT FOR ELECTRONIC ELEMENTS | 65.0297 |
| Germany | 10147298.6 | 9/26/01 | Method and Apparatus for High Speed IC Test Interface | 65.0337 |
| Germany | 10147652.3 | 9/27/01 | On-Chip Optically Triggered Latch for IC Time Measurements | 65.0324 |
| Germany | 10147995.6 | 9/28/01 | Compact, High Collection Efficiency Scinitillator for Secondary Electron Detection | 65.0322 |
| Germany | 10150321.0 | 10/11/01 | Scan Stream Sequencing for Testing Integrated Circuits | 65.0321 |
| Germany | 10162222.8 | 12/18/01 | Optical Coupling for Testing Integrated Circuits | 65.0329 |
| Germany | 10136679.5 | 2/7/02 | Superconducting Single Photon Detector | 65.0332 |
| Germany | 10212617.8 | 3/21/02 | Method and Apparatus for Socket Calibration of Integrated Circuit Testers | 65.0352 |
| Italy | 01919529.6 | 3/19/01 | Column Simultaneously Focusing a Particle Beam and an Optical Beam | 65.0290 |
| Japan | 6-90015 | 4/27/94 | APPARATUS FOR MAINTAINING STIMULATION TO A DEVICE UNDER TEST AFTER A TEST STOPS | 65.0203 |
| Japan | 6-182089 | 8/3/94 | DRIVER CIRCUITS FOR IC TESTER | 65.0209 |
| Japan | 6-210030 | 9/2/94 | LAYOUT OVERLAY FOR FIB OPERATIONS | 65.0210 |
| Japan | 7-91090 | 4/17/95 | METHOD OF PROBING A NET OF AN IC AT AN OPTIMAL PROBE-POINT | 65.0211 |
| Japan | 8-531508 | 4/10/96 | AUTOMATIC PARALLEL ELECTRONIC COMPONENT TESTING METHOD AND EQUIPMENT | 65.0237 |
| Japan | 8-112683 | 5/7/96 | INSULATOR DEPOSITION USING FOCUSED ION BEAM | 65.0234 |
| Japan | 8-147393 | 6/10/96 | Predictive Waveform Acquistion | 65.0216 |
| Japan | 8-187670 | 7/17/96 | VECTOR-BASED WAFEFORM ACQUISITION AND DISPLAY | 65.0239 |
| Japan | 8-203773 | 8/1/96 | Analog Channel for Mixed-Signal VLSI Tester | 65.0222 |
| Japan | 8-203824 | 8/1/96 | Accurate Alignment of Clocks in Mixed-Signal Tester | 65.0228 |
| Japan | 8-240710 | 9/11/96 | ACCELERATED MODE TESTER TIMING | 65.0220 |
| Japan | 9-246703 | 9/11/97 | DRIVER CIRCUITS FOR IC TESTER | 65.0243 |
| Japan | 9-288580 | 10/21/97 | THERMOELECTRIC COOLING GAS-ASSISTED FIB SYSTEM | 65.0245 |
| Japan | 9-289374 | 10/22/97 | GENERATING PULSES IN ANALOG CHANNEL OF ATE TESTER | 65.0252 |
| Japan | 9-307449 | 11/10/97 | METHOD AND APPARATUS FOR MEASURING ELECTRICAL WAVEFORMS USING ATOMIC FORCE MICROSCOPY | 65.0253 |
| Japan | 9-323311 | 11/25/97 | APPARATUS FOR CARRYING SEMICONDUCTOR DEVICES | 65.0257 |
| Japan | 9-338419 | 12/9/97 | PROGRAMMING UTILITY REGISTER TO GENERATE ADDRESSES IN ALGORITHMIC PATTERN GENERATOR | 65.0247 |
| Japan | 9-345286 | 12/15/97 | FIB ETCHING ENHANCED WITH 1,2 DI-IODO-ETHANE | 65.0244 |
| Japan | 9-344985 | 12/15/97 | CHARGED PARTICLE BEAM SYSTEM WITH OPTICAL MICROSCOPE | 65.0248 |
| Japan | 10-36225 | 2/18/98 | PATTERN GENERATOR WITH EXTENDED REGISTER | 65.0266 |

| Country | App. No. | Appl. Date | Title | Case |
|---|---|---|---|---|
| | | | PROGRAMMING | |
| Japan | 10-51060 | 3/3/98 | Through the Substrate Investigation of Flip-Chip ICs | 65.0246 |
| Japan | 10-65834 | 3/16/98 | DUAL-LASER VOLTAGE PROBING OF IC'S | 65.0261 |
| Japan | 10-111250 | 4/22/98 | OPTICAL SYSTEM WITH AN AXIALLY MOVEABLE APERTURED PLATE | 65.0262 |
| Japan | 10-138281 | 5/20/98 | PROVIDING TEST VECTORS WITH PATTERN CHAINING DEFINITION | 65.0254 |
| Japan | 10-292303 | 10/14/98 | MEASURING SIGNALS IN A TESTER SYSTEM | 65.0274 |
| Japan | 10-332748 | 11/24/98 | AUTOMATIC CIRCUIT TESTER HAVING A WAVEFORM ACQUISITION MODE OF OPERATION | 65.0271 |
| Japan | 11-140173 | 5/20/99 | AUTOMATIC SEQUENCING OF FIB OPERATIONS | 65.0269 |
| Japan | 11-189015 | 7/2/99 | SECURING DATA IN A MACHINE FOR TESTING ELECTRONIC COMPONENTS | 65.0291 |
| Japan | 11-298939 | 10/20/99 | MEASURING JITTER OF HIGH-SPEED DATA CHANNELS | 65.0299 |
| Japan | 2000-288647 | 9/22/00 | Double-Pulsed Optical Interferometer for Waveform Probing of Integrated Circuits | 65.0316 |
| Japan | 2000-302945 | 10/2/00 | Test Method and Apparatus for Source Synchronous Signals | 65.0309 |
| Japan | 2000-316082 | 10/17/00 | Packet-Based Device Test System | 65.0306 |
| Japan | 2000-384490 | 11/13/00 | Energy Filtered Focused Ion Beam Column | 65.0281 |
| Japan | 2001-668 | 1/5/01 | Differential Pulsed Laser Beam Probing of Integrated Circuits | 65.0312 |
| Japan | 2001-31019 | 2/7/01 | Socket Calibration Method and Apparatus | 65.0302 |
| Japan | 2001-67243 | 3/9/01 | Calibration Method and Apparatus for Correcting Pulse Width Timing Erros in Integrated Circuit Testing | 65.0307 |
| Japan | 2001-568039 | 3/15/01 | BEAM DELIVERY AND IMAGING FOR OPTICAL PROBING OF A DEVICE OPERATING UNDER ELECTRICAL TEST | 65.0267 |
| Japan | 2001-221971 | 7/23/01 | Superconducting Single Photon Detector | 65.0332 |
| Japan | 2001-252061 | 8/22/01 | TIME-TO-DIGITAL CONVERTER | 65.0296 |
| Japan | 2001-252110 | 8/22/01 | EDGE PLACEMENT AND JITTER MEASUREMENT FOR ELECTRONIC ELEMENTS | 65.0297 |
| Japan | 2001-287506 | 9/20/01 | Method and Apparatus for Remotely Testing Semiconductor | 65.0340 |
| Japan | 2001-303480 | 9/28/01 | Compact, High Collection Efficiency Scinitillator for Secondary Electron Detection | 65.0322 |
| Japan | 2001-303461 | 9/28/01 | On-Chip Optically Triggered Latch for IC Time Measurements | 65.0324 |
| Japan | 2001-305733 | 10/1/01 | Method and Apparatus for High Speed IC Test Interface | 65.0337 |
| Japan | 2001-323752 | 10/22/01 | Scan Stream Sequencing for Testing Integrated Circuits | 65.0321 |
| Japan | 2001-390123 | 12/21/01 | Optical Coupling for Testing Integrated Circuits | 65.0329 |
| Japan | 2001-81349 | 3/22/02 | Method and Apparatus for Socket Calibration of Integrated Circuit Testers | 65.0352 |
| Malaysia | PI9801199 | 3/19/98 | PROVIDING TEST VECTORS WITH PATTERN CHAINING DEFINITION | 65.0254 |
| PCT | PCT/FR97/01987 | 11/6/97 | DEVICE FOR CONTROLLING CONFIRMITY OF CONSUMPTION OF AN ELECTRONIC COMPONENT IN A TESTING MACHINE | 65.0263 |
| PCT | PCT/FR98/00245 | 2/9/98 | POWER SUPPLY CIRCUIT OF AN ELECTRONIC COMPONENT IN A TEST MACHINE | 65.0264 |
| PCT | PCT/IB02/00263 | 1/29/02 | Electric Feeding Device for a Test Installation of Components | 65.0353 |

| Country | App. No. | App. Date | Title | [illegible] |
|---|---|---|---|---|
| PCT | PCT/US02/07305 | 3/11/02 | Method for Global Die Thinning and Polishing of Flip-Chip Packaged Integrated Circuits | 65.0338 |
| PCT | PCT/US02/08427 | 3/18/02 | Test System Formatters | 65.0348 |
| PCT | PCT/US02/08627 | 3/19/02 | Low-Jitter Clock for Test System | 65.0349 |
| PCT | PCT/US02/08539 | 3/19/02 | Test System Algorithmic Program Generators | 65.0350 |
| PCT | PCT/US02/12109 | 4/16/02 | Measuring Back-Side Voltage of an Integrated Circuit | 65.0354 |
| PCT | PCT/US02/13649 | 4/30/02 | Open-Loop for Waveform Acquisition | 65.0355 |
| S. Korea | 32178/96 | 7/18/96 | ANALOG CHANNEL FOR MIXED-SIGNAL-VLSI TESTER | 65.0222 |
| S. Korea | 32177/96 | 8/1/96 | ACCURATE ALIGNMENT OF CLOCKS IN MIXED-SIGNAL TESTER | 65.0228 |
| S. Korea | 38878/96 | 9/9/96 | ACCELERATED MODE TESTER TIMING | 65.0220 |
| S. Korea | 40545/97 | 8/25/97 | GENERATING PULSES IN ANALOG CHANNEL OF ATE TESTER | 65.0252 |
| S. Korea | 41268/97 | 8/26/97 | CHARGED PARTICLE BEAM SYSTEM WITH OPTICAL MICROSCOPE | 65.0248 |
| S. Korea | 42058/97 | 8/28/97 | | 65.0243 |
| S. Korea | 44675/97 | 8/30/97 | METHOD AND APPARATUS FOR MEASURING ELECTRICAL WAVEFORMS USING ATOMIC FORCE MICROSCOPY | 65.0253 |
| S. Korea | 60724/97 | 11/18/97 | APPARATUS FOR CARRYING SEMICONDUCTOR DEVICES | 65.0257 |
| S. Korea | 66467/97 | 12/6/97 | PROGRAMMING UTILITY REGISTER TO GENERATE ADDRESSES IN ALGORITHMIC PATTERN GENERATOR | 65.0247 |
| S. Korea | 70005/97 | 12/17/97 | FIB ETCHING ENHANCED WITH 1,2 DI-IODO-ETHANE | 65.0244 |
| S. Korea | 7006327/99 | 2/9/98 | POWER SUPPLY CIRCUIT OF AN ELECTRONIC COMPONENT IN A TEST MACHINE | 65.0264 |
| S. Korea | 4724/98 | 2/17/98 | PATTERN GENERATOR WITH EXTENDED REGISTER PROGRAMMING | 65.0266 |
| S. Korea | 14126/98 | 4/21/98 | OPTICAL SYSTEM WITH AN AXIALLY MOVEABLE APERTURED PLATE | 65.0262 |
| S. Korea | 17910/98 | 5/19/98 | PROVIDING TEST VECTORS WITH PATTERN CHAINING DEFINITION | 65.0254 |
| S. Korea | 50368/98 | 11/24/98 | AUTOMATIC CIRCUIT TESTER HAVING A WAVEFORM ACQUISITION MODE OF OPERATION | 65.0271 |
| S. Korea | 55963/2000 | 9/23/00 | Double-Pulsed Optical Interferometer for Waveform Probing of Integrated Circuits | 65.0316 |
| S. Korea | 0057947/2000 | 10/2/00 | Test Method and Apparatus for Source Synchronous Signals | 65.0309 |
| S. Korea | 0001728/2001 | 1/12/01 | Differential Pulsed Laser Beam Probing of Integrated Circuits | 65.0312 |
| S. Korea | 00086118/2001 | 2/21/01 | Socket Calibration Method and Apparatus | 65.0302 |
| S. Korea | 0013100/2001 | 3/14/01 | Calibration Method and Apparatus for Correcting Pulse Width Timing Erros in Integrated Circuit Testing | 65.0307 |
| S. Korea | 0045456/2001 | 7/27/01 | Superconducting Single Photon Detector | 65.0332 |
| S. Korea | 0050697/2001 | 8/22/01 | TIME-TO-DIGITAL CONVERTER | 65.0296 |
| S. Korea | 51333/2001 | 8/24/01 | EDGE PLACEMENT AND JITTER MEASUREMENT FOR ELECTRONIC ELEMENTS | 65.0297 |
| S. Korea | 59897/2001 | 9/27/01 | On-Chip Optically Triggered Latch for IC Time Measurements | 65.0324 |
| S. Korea | 10-2001-0059997 | 9/27/01 | Method and Apparatus for Remotely Testing Semiconductor | 65.0340 |
| S. Korea | 60418/2001 | 9/28/01 | Compact, High Collection Efficiency Scinitillator for Secondary Electron Detection | 65.0322 |
| S. Korea | 00600419/2001 | 9/28/01 | Method and Apparatus for High Speed IC Test Interface | 65.0337 |
| S. Korea | 0065625/2001 | 10/24/01 | Scan Stream Sequencing for Testing Integrated Circuits | 65.0321 |



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| Country | App. No. | App. Date | Title | [illegible] |
|---|---|---|---|---|
| S. Korea | 0082422/2001 | 12/21/01 | Optical Coupling for Testing Integrated Circuits | 65.0329 |
| S. Korea | 0016318/2002 | 3/26/02 | Method and Apparatus for Socket Calibration of Integrated Circuit Testers | 65.0352 |
| Singapore | 200105909-6 | 9/26/01 | Method and Apparatus for Remotely Testing Semiconductor | 65.0340 |
| Taiwan | 87101512 | 2/5/98 | DUAL-LASER VOLTAGE PROBING OF IC'S | 65.0261 |
| Taiwan | 89119176 | 9/18/00 | Double-Pulsed Optical Interferometer for Waveform Probing of Integrated Circuits | 65.0316 |
| Taiwan | 89120494 | 12/1/00 | Test Method and Apparatus for Source Synchronous Signals | 65.0309 |
| Taiwan | 90101828 | 1/31/01 | Socket Calibration Method and Apparatus | 65.0302 |
| Taiwan | 89127898 | 1/31/01 | Differential Pulsed Laser Beam Probing of Integrated Circuits | 65.0312 |
| Taiwan | 9012312 | 8/20/01 | TIME-TO-DIGITAL CONVERTER | 65.0296 |
| Taiwan | 90120431 | 8/20/01 | EDGE PLACEMENT AND JITTER MEASUREMENT FOR ELECTRONIC ELEMENTS | 65.0297 |
| Taiwan | 90117378 | 9/3/01 | Superconducting Single Photon Detector | 65.0332 |
| Taiwan | 90122395 | 9/6/01 | On-Chip Optically Triggered Latch for IC Time Measurements | 65.0324 |
| Taiwan | 90124440 | 10/3/01 | Scan Stream Sequencing for Testing Integrated Circuits | 65.0321 |
| Taiwan | 90123501 | 10/12/01 | Method and Apparatus for High Speed IC Test Interface | 65.0337 |
| Taiwan | 90130971 | 12/13/01 | Optical Coupling for Testing Integrated Circuits | 65.0329 |
| Taiwan | 91105007 | 3/15/02 | Method and Apparatus for Socket Calibration of Integrated Circuit Testers | 65.0352 |
| Taiwan | 091105226 | 3/19/02 | Test System Formatters | 65.0348 |
| Taiwan | 0911052254 | 3/19/02 | Low-Jitter Clock for Test System | 65.0349 |
| Taiwan | 091105225 | 3/19/02 | Test System Algorithmic Program Generators | 65.0350 |
| Taiwan | 091107758 | 4/16/02 | Measuring Back-Side Voltage of an Integrated Circuit | 65.0354 |
| Taiwan | 091108979 | 4/30/02 | Open-Loop for Waveform Acquisition | 65.0355 |
| U.K. | 0100780.6 | 1/11/01 | Test Method and Apparatus for Source Synchronous Signals | 65.0309 |
| U.K. | 01919529.6 | 3/19/01 | Column Simultaneously Focusing a Particle Beam and an Optical Beam | 65.0290 |



TRADEMARK
REEL: 002766 FRAME: 0181

**Schedule B**

Trademarks:

| Country | Trademark | Serial Number | Reg. No. |
|---|---|---|---|
| U.S. | Accelerated Vector Mode | 74/655,764 | 2,198,732 |
| U.S. | Arrow | | |
| U.S. | ASAP | 74/295198 | 1,813,447 |
| U.S. | ASAP | 74/083792 | 1,887,766 |
| U.S. | AutoEdge | | |
| U.S. | AVM | 74/655,766 | 2,099,862 |
| U.S. | BatchProbe | 75/195,094 | 2,307,702 |
| U.S. | BATCHREPAIR | 75/195,026 (abandoned) | |
| U.S. | BATCHREPAIR | 76/191,969 (abandoned) | |
| U.S. | DART | | |
| U.S. | DeFT | 76/228570 (abandoned) | |
| U.S. | DeFT | 76/257564 (abandoned) | |
| U.S. | ETC1000 | | |
| U.S. | EXA 3000 | | |
| U.S. | EXA2000 | | |
| U.S. | GBS | | |
| U.S. | Gigabit Sampler | | |
| U.S. | IDS | 74/177,780 | 1,774,080 |
| U.S. | IDS OptiFIB | 76/284,263 | |
| U.S. | IDS5000 | | |
| U.S. | Integrated Test Facility (ITF) | | |
| U.S. | InterActiv Services | | |
| U.S. | ISOCHRONOUS FABRIC INTERFACE | 78/175,606 | |
| U.S. | ITS | 75/298,146 | 2,252,458 |
| U.S. | JAVELIN | | |
| U.S. | Keep Alive | 74/387,205 | 1,837,767 |
| U.S. | NanoBlade | 76/081,008 (abandoned) | |
| U.S. | NetTracer | 75/195,095 (abandoned) | |
| U.S. | NP Platform | 78/244,106 | |
| U.S. | NPTest IDS OptiFIB | 78/201,707 | |
| U.S. | NPTest | 76/446026 | |
| U.S. | NxGenConnect | 76/340933 | |
| U.S. | NxGenSupport | 76/340932 | |
| U.S. | ONIDIA | | |
| U.S. | OptiCA | 78/201,756 | |
| U.S. | Performer/Performa | | |
| U.S. | PICA | | |
| U.S. | RDRAM | | |
| U.S. | RDX2200 | | |
| U.S. | SABER | 75/301,652 | 2,345,915 |
| U.S. | Sapphire | | |
| U.S. | Sapphire NP | 78/244,117 | |
| U.S. | SEMIQUEST | | |
| U.S. | Sequencer-Per-Pin | 74/083,754 | 1,759,075 |
| U.S. | Sprint | | |

| Country | Trademark | Serial Number | Reg. # |
|---|---|---|---|
| U.S. | TESTER PER BOARD | | |
| U.S. | The Eye of the FIB | | |
| U.S. | Through Silicon | | |
| U.S. | TimeStamper | 76/333,767 | |
| U.S. | TruEdge | | |
| U.S. | TruSite | | |
| U.S. | XTOS | | |
| Benelux | NanoBlade | 0968038 | |
| Benelux | Sequencer-Per-Pin | 730605 | 465805 |
| Canada | ASAP | 644,115 | |
| China | NanoBlade | 2000118605 | |
| China | NxGenSupport | 3242989 | |
| CTM | IDS OptiFIB | 002518397 | |
| France | NanoBlade | 003037591 | 003037591 |
| France | Sequencer Per Pin | 1542822 | 1542822 |
| Germany | NanoBlade | 300 49 118.2/09 | 30049118 |
| Germany | Sequencer-Per-Pin | | |
| Italy | Sequencer-Per-Pin | 22149C/89 | 557736 |
| Japan | ASAP | 01-073912 | 2663770 |
| Japan | IDS | 134,794/1996 | |
| Japan | IDS OptiFIB | 2002-001113 | |
| Japan | RDX 2200 | | |
| Japan | SABER | 2000-129870 | |
| Japan | SABER | 2000-129870 | |
| Japan | Sequencer-Per-Pin | 01-073911 | 2670975 |
| Japan | TruEdge | | |
| S. Korea | ASAP | | |
| S. Korea | IDS OptiFIB | 40-2001-57497 | |
| S. Korea | RDX 2200 | | |
| S. Korea | Sequencer-Per-Pin | 89-16290 | 210717 |
| Singapore | ASAP | 4706/1989 | 4706/89 |
| Singapore | NanoBlade | T00/12054Z | |
| Singapore | Sequencer-Per-Pin | 4645/89 | 4646/1989 |
| Taiwan | ASAP | 78/30190 | 502574 |
| Taiwan | RDX 2200 | | |
| Taiwan | Sequencer-Per-Pin | 78/030189 | 502573 |
| U.K. | Sequencer-Per-Pin | 1388155 | 1388155 |

**Annex 1**

# GENERAL ASSIGNMENT AND ASSUMPTION AGREEMENT

This General Assignment and Assumption Agreement (this "Agreement"), dated as of May 10, 2002, by and between Schlumberger Technologies, Inc., a Delaware Corporation ("STI" or the "Assignor"), and Schlumberger Technology Solutions LLC, a Delaware limited liability company ("STS LLC" or the "Assignee").

## WITNESSETH

**WHEREAS,** Assignor desires to transfer certain of its assets to Assignee in consideration of, among other things, Assignee's assumption of certain liabilities of Assignor, and the issuance of interests in Assignee; and

**WHEREAS,** Assignee desires to accept that transfer of certain assets and liabilities from Assignor;

**NOW, THEREFORE,** for and in consideration of the agreements contained herein and other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the parties hereby agree as follows:

1. Assignor does hereby grant, sell, convey, assign and deliver all of the assets described on Schedule 1 hereto (collectively, the "Conveyed Assets"), unto Assignee, and Assignee's successors and assigns on an "as is," "where is" basis, and Assignee hereby accepts and assumes from Assignor, the assets, properties and rights hereby granted, sold, conveyed, assigned and delivered.

2. Assignee does hereby assume all Liabilities of Assignor arising out of or related to the Conveyed Assets or arising out of or related to the business and operations transacted with the Conveyed Assets whether incurred or occurring before, on or after the date of this Agreement, including, without limitation, those Liabilities listed on Schedule 2 hereto (collectively, the "Assumed Liabilities") and agrees to pay, discharge or perform those Liabilities when due.

3. Assignor hereby covenants and agrees to and with Assignee, and Assignee's successors and assigns, to execute, acknowledge, and deliver all and every such further conveyance and other instrument and to do such further acts as may be deemed by Assignee to be reasonably necessary or appropriate more fully to assure Assignee and Assignee's successors and assigns that all the Conveyed Assets have been validly conveyed hereby, or to aid and assist in collecting and reducing to possession, any of or all of the Conveyed Assets, or in connection with the settlement of any obligations or liabilities to Assignor.

4. Assignee hereby covenants and agrees to and with Assignor and Assignor's successors and assigns, to execute, acknowledge, and deliver all and every such further conveyance and other instrument and to do such further acts as may be deemed by Assignor to be reasonably necessary or appropriate more fully to assure Assignor and Assignor's successors and assigns that all the Assumed Liabilities have been validly conveyed hereby.

5. (a) If there are prohibitions against, or conditions to, the conveyance of any of the Conveyed Assets or the assumption of any of the Assumed Liabilities without the prior written consent of third parties, including governmental authorities, whose consent is needed for the transfer of any of the Conveyed Assets or the assumption of any of the Assumed Liabilities or

the issuance of any necessary licenses, permits or other authorizations, which if not satisfied would result in a breach of such prohibitions or conditions or would give an outside party the right to terminate or limit any right of the Assignee with respect to any Conveyed Asset or-Assumed Liability or allow the outside party to receive a payment or other consideration then any provisions contained in this Agreement to the contrary notwithstanding, the transfer of title to, or interest in, such Conveyed Asset, or the assumption-of such Assumed Liability pursuant to this Agreement shall not become effective unless and until such restrictions on transfer are satisfied, waived or no longer applies.

(b) The parties shall cooperate to effect such transfers as promptly as shall be, practicable. Nothing herein shall be deemed to require the transfer of any Conveyed Assets or the assumption of any Assumed Liabilities that by their terms or operation of law cannot be transferred or assumed; provided, however, that the parties shall cooperate to obtain any necessary consents or approvals for the transfer of all Conveyed Assets and the assumption of all Assumed Liabilities contemplated to be transferred or assumed pursuant to this Agreement and shall, even in the absence of any necessary consents or approvals, transfer the equitable ownership of Assets when such a transfer is permitted. In the event that any such transfer of Conveyed Assets or assumption of Assumed Liabilities is not consummated as of the date of this Agreement the party retaining such Conveyed Asset or Assumed Liability shall thereafter hold such Conveyed Asset in trust for the use and benefit of the party entitled thereto (at the expense of the party entitled thereto) and retain such Assumed Liability for the account of the party by whom such Assumed Liability is to be assumed, pursuant hereto, and take such other action as may be reasonably requested by the party to which such Conveyed Asset is to be transferred, or by whom such Assumed Liability is to be assumed, as the case may be, in order to place such party, insofar as reasonably possible, in the same position as would have existed had such Conveyed Asset or Assumed Liability been transferred or assumed as contemplated hereby. As and when any such Conveyed Asset becomes transferable or such Assumed Liability can be assumed, such transfer or assumption shall be effected forthwith. Subject to the foregoing, the parties agree that, as of the date of this Agreement, each party hereto shall be deemed to have acquired complete and sole beneficial ownership over all of the Conveyed Assets, together -with all rights, powers and privileges incident thereto, and shall be deemed to have assumed in accordance with the terms of this Agreement all of the Assumed Liabilities, and all duties, obligations and responsibilities incident thereto, which such party is entitled to acquire or required to assume pursuant to the terms of this Agreement.

(c) If after two years from the date of this Agreement any Conveyed Asset remains subject to an arrangement described in Section 5(b) unless the parties elect to continue such arrangement on such terms as they may mutually agree, such arrangement shall terminate. In the event of a termination, the beneficial owner may (i) direct the party acting as trustee to transfer the Conveyed Asset to the beneficial owner, at the sole risk of such owner (which will thereafter indemnify the trustee/transferor from all losses, claims, damages, Liabilities, lawsuits, actions, costs and expenses, including reasonable attorneys' fees, arising as a result of such transfer), (ii) direct the party acting as trustee to sell or liquidate the subject Conveyed Asset for the account of, and at the sole risk and expense of, such owner, which shall be entitled to receive all of the net proceeds of such sale or liquidation or (iii) direct the party acting as trustee to purchase the affected Conveyed Asset at a price mutually agreed or, if no such agreement is reached, at the fair market value thereof as determined by a neutral third-party appraisal process.

This Agreement shall be governed by and construed in accordance with the laws of the State of Delaware, without regard to the conflicts of laws provisions thereof.

**IN WITNESS WHEREOF,** the parties have caused this Agreement to be duly executed as of the date first set forth above.

**ASSIGNOR:**

**SCHLUMBERGER TECHNOLOGIES, INC.**

By:
Name: Jurren Schoonbeek
Title: Vice President

**ASSIGNEE:**

**SCHLUMBERGER TECHNOLOGY SOLUTIONS LLC**

By:____________________________________
Name:
Title:

**IN WITNESS WHEREOF,** the parties have caused this Agreement to be duly executed as of the date first set forth above.

**ASSIGNOR:**

**SCHLUMBERGER TECHNOLOGIES, INC.**

By:________________________________

Name:

Title:

**ASSIGNEE:**

**SCHLUMBERGER TECHNOLOGY SOLUTIONS LLC**

By: Ashok Belani

Name:

Title:

**SCHEDULE 1**

**to the**

**General Assignment and Assumption Agreement**

The following Conveyed Assets shall be transferred by Assignor to Assignee:

All of the assets of the Semiconductor Solutions Group related to the Test, Probe and SABER business segments ("Test, Probe and SABER") of Assignor (i) represented on the Balance Sheet, dated as of March 31, 2002, attached herewith as Exhibit A (the "Balance Sheet"), (ii) written off, expensed or fully depreciated that, had they not been written off, expensed or fully depreciated, would have been reflected in the Balance sheet in accordance with the principles and accounting policies under which the Balance Sheet was prepared; and (iii) acquired after the date of the Balance Sheet that would be reflected in the Balance Sheet if such Balance Sheet were prepared, including any business transaction processing that may occur on the systems of Assignor or its affiliates during the period from the date of the Balance Sheet through the date of separation, including in the case of (i) through (iii) above, without limitation, all of the:

(a) real property, leaseholds and subleaseholds therein, improvements, fixtures, and fittings thereon, and easements, rights-of-way, and other appurtenants thereto;
(b) tangible personal property (such as machinery, equipment, inventories of raw materials and supplies, manufactured and purchased parts, goods in process and finished goods, furniture, automobiles, trucks, tractors, trailers, tools, jigs, and dies);
(c) intellectual property, goodwill associated therewith, licenses and sublicenses granted and obtained with respect thereto, and rights thereunder, remedies against infringements thereof, and rights to protection of interests therein under the laws of all jurisdictions;
(d) agreements, contracts, indentures, mortgages, instruments, security interests, guaranties, other similar arrangements, and rights thereunder, including but not limited to the following contracts:
   - Intel Corporation Purchase Agreement, between Intel Corporation, as Buyer, and Schlumberger Technologies ATE Division, as Seller; and
   - PICA Tooling Technology License and Joint Development Agreement, between International Business Machines Corporation and Schlumberger Technologies, Inc.;
(e) accounts, notes, and other receivables;
(f) claims, deposits, prepayments, refunds, causes of action, chooses in action, rights of
(g) recovery, rights of set off, and rights of recoupment, but excluding any such item relating to the payment of taxes;
(h) franchises, approvals, permits, licenses, orders, registrations, certificates, variances, and similar rights obtained from governments and governmental agencies;
(i) books, records, ledgers, files, documents, correspondence, lists, plats, architectural plans;
(j) drawings, and specifications, creative materials, and advertising and promotional materials;
(k) studies, reports, and other printed or written materials, and rights in and with respect to the assets associated with its employee benefit plans;

provided, however, that the Conveyed Assets shall not include (i) any assets required or used by the Assignor in relation to any business of the Assignor other than Test, Probe and

SABER, unless such assets are expressly allocated to Test, Probe and SABER pursuant to the books and records of Assignor, and (ii) any of the rights of the Assignor under this Agreement.

End of Schedule

**SCHEDULE 2**

**to the**

**General Assignment and Assumption Agreement**

The following Assumed Liabilities shall be assumed by Assignee from Assignor:

All of the liabilities, obligations, claims and commitments (whether known or unknown, whether asserted or unasserted, whether absolute or contingent, whether accrued or unaccrued, whether liquidated or unliquidated, and whether due or to become due) of the Semiconductor Solutions Group related to the Test, Probe and SABER business segments ("Test, Probe and SABER") of Assignor, whether or not the same would be required by generally accepted principles and accounting policies to be reflected in financial statements or disclosed in the notes thereto, including, without limitation:

(a) all liabilities and obligations of Test, Probe & SABER of Assignor represented on the Balance Sheet, subject to any discharge subsequent to the date of the Balance Sheet;
(b) all liabilities and obligations of Test, Probe & SABER of Assignor arising after the date of the Balance Sheet that would be reflected in the Balance Sheet if the Balance Sheet were prepared using the same principals and accounting policies under which the Balance Sheet was prepared;
(c) all liabilities and obligations of Test, Probe & SABER of Assignor under the agreements, contracts, leases, licenses, and other arrangements referred to in relation to the Conveyed Assets;
(d) all liabilities and obligations of Test, Probe & SABER under existing Assignor employee benefit plans;
(e) all obligations of Test, Probe & SABER of Assignor to indemnify any person by reason of the fact that he or it was an employee or agent of Test, Probe & SABER or was serving at the request of Test, Probe & SABER as an employee, or agent of another entity (whether such indemnification is for judgments, damages, penalties, fines, costs, amounts paid in settlement, losses, expenses, or otherwise and whether such indemnification is pursuant to any statute, agreement, or otherwise); and
(f) all other liabilities and obligations of Test, Probe & SABER of Assignor;

provided, however, that the Assumed Liabilities shall not include (i) any liability or obligation under the existing Assignor employee benefit plans relating to pensions and retiree medical benefits, including, without limitations the Schlumberger Technology Corporation Pension Plan, Schlumberger Group Health Care Plan and Schlumberger Technologies Inc. Savings and Profit Sharing Plan, (ii) any liability or obligation arising from any proceeding or suit which is pending against Assignor or the Test, Probe and SABER business segments of Assignor as of the date hereof, and (iii) any cost or expense incurred by Test, Probe & SABER required for the consummation of the transactions contemplated in this Agreement.

End of Schedule

RECORDED: 06/23/2003

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REEL: 002766 FRAME: 0191