12-27-2004

FORM PTO-1594
(Rev. 03/01)
OMB No. 0651-0027 (exp. 05/31/2002)

102910908

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof.

1. Name of conveying party(ies): Sequence Design, Inc.

☐ Individual(s) ☐ Association
☐ General Partnership ☐ Limited Partnership
☒ Corporation-State
☐ Other

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies):
Name: **Silicon Valley Bank**
Internal Address: HA155

Street Address: 3003 Tasman Drive

City: Santa Clara State: CA ZIP: 95054

3. Nature of conveyance:

☐ Assignment ☐ Merger
☒ Security Agreement ☐ Change of Name
☐ Other _____

Execution Date: 11/24/04

☐ Individual(s) citizenship
☐ Association
☐ General Partnership
☐ Limited Partnership
☒ Corporation-State-Delaware
☐ Other

If assignee is not domiciled in the United States, a domestic representative designation is attached: ☐ Yes ☐ No
Additional name(s) & address(es) attached? ☐ Yes ☒ No

4. Application number(s) or registration number(s):

A. Trademark Application No.(s)	B. Trademark No.(s)
76/523,490 76/523,255	
78/382,490	**2,162,591**
76/564,875	
76/557,290	
76/557,279	
76/425,586	

Additional numbers attached? ☐ Yes ☒ No

2004 DEC 23 AM 11:24
OPR/FINANCE

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: **Silicon Valley Bank**

Internal Address: Loan Documentation HA155

Street Address: 3003 Tasman Dr.

City: Santa Clara State: Ca ZIP: 95054

6. Total number of applications and registrations involved: 8

7. Total fee (37 CFR 3.41): $ 215.-
☑ Enclosed
☐ Authorized to be charged to deposit account

8. Deposit account number:
(Attach duplicate copy of this page if paying by deposit account)

DO NOT USE THIS SPACE

12/27/2004 ECOOPER 00000084 76523490
01 FC:8521 40.00 OP
02 FC:8522 175.00 OP

9. Statement and signature.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Trisha Sedillo
Name of Person Signing
Jacqueline Le

Trisha Sedillo
Signature

12/15/04

Total number of pages including cover sheet, attachments, and document:

Mail documents to be recorded with required cover sheet information to:
Commissioner of Patent & Trademarks, Box Assignments
Washington, D.C. 20231

INTELLECTUAL PROPERTY SECURITY AGREEMENT

THIS INTELLECTUAL PROPERTY SECURITY AGREEMENT is entered into as of November 24, 2004 by and between SILICON VALLEY BANK ("Bank") and SEQUENCE DESIGN, INC. ("Grantor").

RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodation to Grantor (the "Loans") in the amounts and manner set forth in that certain Second Amended and Restated Loan and Security Agreement by and between Bank and Grantor and the other Borrowers party thereto of even date herewith (as the same may be amended, modified or supplemented from time to time, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in certain Copyrights, Trademarks, Patents, and Mask Works to secure the obligations of Grantor under the Loan Agreement.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

To secure its obligations under the Loan Agreement, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its Intellectual Property Collateral (including without limitation those Copyrights, Patents and Trademarks and Mask Works listed on Exhibits A, B and C and D hereto), and including without limitation all proceeds thereof (such as, by way of example but not by way of limitation, license royalties and proceeds of infringement suits), the right to sue for past, present and future infringements, all rights corresponding thereto throughout the world and all re-issues, divisions continuations, renewals, extensions and continuations-in-part thereof.

This security interest is granted in conjunction with the security interest granted to Bank under the Loan Agreement. The rights and remedies of Bank with respect to the security interest granted hereby are in addition to those set forth in the Loan Agreement and the other Loan Documents, and those which are now or hereafter available to Bank as a matter of law or equity. Each right, power and remedy of Bank provided for herein or in the Loan Agreement or any of the Loan Documents, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right, power or remedy provided for herein and the exercise by Bank of any one or more of the rights, powers or remedies provided for in this

Intellectual Property Security Agreement, the Loan Agreement or any of the other Loan Documents, or now or hereafter existing at law or in equity, shall not preclude the simultaneous or later exercise by any person, including Bank, of any or all other rights, powers or remedies.

[SIGNATURES APPEAR ON THE FOLLOWING PAGE]

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

Address of Grantor:

SEQUENCE DESIGN, INC.

469 El Camino Real, Suite 202
Santa Clara, California 95050

By: _____
Name: VIC KULKARNI
Title: President & CEO

BANK:

Address of Bank:

SILICON VALLEY BANK

3003 Tasman Drive
Santa Clara, California 95054

By: _____
Name: Rick Tu
Title: VP

EXHIBIT A

Copyrights

Description	Registration/ Application Number	Registration/ Application Date
~~No registered copyrights~~		
1soreg computer power modules	TX1-106-040	10/31/01

SVB/Sequence (IP Sec Ag)
SVB_Sequence (IP Security Agreement - Sequence Design) (2)

EXHIBIT B

Patents

Description	Registration/ Application Number	Registration/ Application Date
See attached spreadsheet		

Sequence Design, Inc. as of November 17, 2004

Our File No.	Country	Title	Application No.	Filing Date	Patent No.	Issue Date	Status
M-11051 US	USA	RTL Power Analysis Using Gate-Level Cell Power Models	09/798,016	February 28, 2001	6,598,209	July 22, 2003	Granted
M-11051-1C US	USA	RTL Power Analysis Using Gate-Level Cell Power Models	10/447,076	May 27, 2003			Allowed
M-11976 US	USA	Method and Apparatus for Logic Synthesis (Word-Oriented Netlist)	09/375,836	August 16, 1999	6,574,787	June 3, 2003	Granted
M-11977 US	USA	Method and Apparatus for Logic Synthesis (Inferring Complex Components)	09/375,254	August 16, 1999	6,493,648	December 10, 2002	Granted
M-11984 US	USA	Method for Balanced- Delay Clock Tree Insertion	10/023,329	December 14, 2001	6,698,006	February 24, 2004	Granted
M-11985 US	USA	Circuit Optimization for Minimum Path Timing Violations	10/008,458	November 30, 2001	6,701,505	March 2, 2004	Granted
M-11985-1D US	USA	Circuit Optimization for Minimum Path Timing Violations	10/627,933	July 25, 2003			Pending
M-11990 US	USA	Method and Apparatus Logic Synthesis With Elaboration	09/375,843	August 16, 1999	6,519,755	February 11, 2003	Granted
M-12482 US	USA	Method for Determining a Zero-Skew Buffer Insertion Point	10/022,751	December 14, 2001	6,701,507	March 2, 2004	Granted
M-12483 US	USA	Method for Match Delay Buffer Insertion	10/022,743	December 14, 2001	6,701,506	March 2, 2004	Granted
M-12484 US	USA	Method for Optimal Driver Selection	10/022,747	December 14, 2001			Granted
M-12484-1D US	USA	Method for Optimal Driver Selection	N/A	May 3, 2004			Pending
M-12608 US	USA	Vectorless Instantaneous Current Estimation	10/262,914	October 1, 2002			Granted
M-12608-1D US	USA	Vectorless Instantaneous Current Estimation	10/926,660	August 25, 2004			Pending
M-15118 US	USA	Current Scheduling System And Method For Optimizing Multi-Threshold CMOS Designs	10/739,659	December 17, 2003			Pending
M-4310 JP	Japan	System and Method for Interconnect Modeling	10-40376	February 23, 1998			Pending

Sequence Design, Inc. as of November 17, 2004

Our File No.	Country	Title	Application No.	Filing Date	Patent No.	Issue Date	Status
M-4310 US	USA	System and Method for Interconnect Modeling	08/804,524	February 21, 1997	5,901,063	May 4, 1999	Granted
M-4833 TW	Taiwan	Methods for Determining On-Chip Interconnect Process Parameters	87115892	September 24, 1998	136000	November 1, 2001	Granted
M-4833 US	USA	Methods for Determining On-Chip Interconnect Process Parameters	08/937,393	September 25, 1997	6,057,171	May 2, 2000	Granted
M-4833-1D US	USA	Methods for Determining On-Chip Interconnect Process Parameters	09/245,812	February 4, 1999	6,312,963	November 6, 2001	Granted
M-4833-2D US	USA	Methods for Determining On-Chip Interconnect Process Parameters	09/244,616	February 4, 1999	6,291,254	September 18, 2001	Granted
M-4833-3P US	USA	Methods for Determining On-Chip Interconnect Process Parameters	09/373,923	August 12, 1999	6,403,389	June 11, 2002	Granted
M-7493 US	USA	Method and System for Extraction of Parasitic Interconnect Impedance Including Inductance	09/350,966	July 9, 1999	6,381,730	April 30, 2002	Granted
M-7493-1C US	USA	Method and System for Extraction of Parasitic Interconnect Impedance Including Inductance	10/057,165	January 24, 2002	6,643,831	November 4, 2003	Granted
M-7781 US	USA	Method for Modeling A Conductive Semiconductor Substrate	09/405,510	September 23, 1999	6,311,312	October 20, 2001	Granted
M-8179 US	USA	Method and Apparatus for Interconnect-Driven Optimization of Integrated Circuit Design	09/516,489	March 1, 2000	6,591,407	July 8, 2003	Granted
M-8179-1D US	USA	Method and Apparatus for Interconnect-Driven Optimization of Integrated Circuit Design	10/387,644	March 12, 2003			Pending

EXHIBIT C

Trademarks

Description	Registration/ Application Number	Registration/ Application Date
See attached spreadsheet		

Sequence Design, Inc. as of November 17, 2004

Our File No.	Country	Mark Name	Application No.	Filing Date	Registration No.	Registered Date	Status
TM-2030 US	USA	ELMO	76/523,490	June 18, 2003			Filed
TM-2031 US	USA	COOLTIME	76/523,255	June 18, 2003	2,881,00	9/7/2004	Registered
TM-2022i US	USA	ELECTRONICALLYCORRECT	78/382,490	March 11, 2004			Filed
TM-2024 US	USA	Extractionstage	76/564,875	December 12, 2003			Filed
TM-2021 US	USA	PHYSICALSTUDIO	76/557,290	November 5, 2003			Filed
TM-2000 JP	JAPAN	NANOCOOL	2002-097653	November 19, 2002	4665189	4/18/2003	Registered
TM-2026 US	USA	Columbus	75/109,383	May 24, 1996	2,162,591	6/2/1998	Registered
TM-2009 US	USA	Showtime	76/557,279	November 5, 2003			Filed
TM-2000 US	USA	NANOCOOL	76/425,586	June 27, 2002			Filed
	USA	WATTWATCHER	75/338,869	August 11,1997	2,252,594	6/15/1999	Registered
	USA	SENTE	75/586,180	November 10, 1998	2,306,075	1/4/2000	Registered
	USA	SENTE	75/338,872	August 11,1997	2,262,053	7/20/1999	Registered

EXHIBIT D

Mask Works

Description	Registration/ Application Number	Registration/ Application Date
No mask works		