Form PTO-1594 (Rev. 07/05)
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U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

RECORDATION FORM COVER SHEET
TRADEMARKS ONLY

To the Director of the U. S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies):
irvine Sensors Corporation

☐ Individual(s) ☐ Association
☐ General Partnership ☐ Limited Partnership
☑ Corporation- State: Delaware
☐ Other

Citizenship (see guidelines)

Additional names of conveying parties attached? ☐ Yes ☑ No

2. Name and address of receiving party(ies)
Additional names, addresses, or citizenship attached? ☐ Yes ☑ No

Name: Sqaure 1 Bank
Internal Address:
Street Address: 406 Blackwell Street, Suite 240
City: Durham
State: NC
Country: USA Zip: 27701

☐ Association Citizenship
☐ General Partnership Citizenship
☐ Limited Partnership Citizenship
☑ Corporation Citizenship
☐ Other Citizenship

If assignee is not domiciled in the United States, a domestic representative designation is attached: ☐ Yes ☐ No
(Designations must be a separate document from assignment)

3. Nature of conveyance)/Execution Date(s) :
Execution Date(s) December 30, 2005

☐ Assignment ☐ Merger
☑ Security Agreement ☐ Change of Name
☐ Other

4. Application number(s) or registration number(s) and identification or description of the Trademark.

A. Trademark Application No.(s)
78/620,483
78/544,618
76/552,662

B. Trademark Registration No.(s)
2,728,041
2.490.859

Additional sheet(s) attached? ☐ Yes ☑ No

C. Identification or Description of Trademark(s) (and Filing Date if Application or Registration Number is unknown):
POD-IR
PMTV
Irvine Sensors Corporation
CAM-NOIR
Redhawk Vision

5. Name & address of party to whom correspondence concerning document should be mailed:
Name: Terri Finnegan
Internal Address: Square 1 Bank
Street Address: 406 Blackwell Street
Suite 240
City: Durham
State: NC Zip: 27701
Phone Number: 914-314-3086
Fax Number: 914-314-3080
Email Address: tfinnegan@square1bank.com

6. Total number of applications and registrations involved: 5

7. Total fee (37 CFR 2.6(b)(6) & 3.41) $ 140
☐ Authorized to be charged by credit card
☑ Authorized to be charged to deposit account
☐ Enclosed

8. Payment Information:
a. Credit Card Last 4 Numbers
Expiration Date
b. Deposit Account Number 50-3822
Authorized User Name Terri Finnegan

9. Signature: Terri Finnegan 4-4-06
Signature Date

Terri Finnegan
Name of Person Signing

Total number of pages including cover sheet, attachments, and document: 9

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O. Box 1450, Alexandria, VA 22313-1450

CH $140.00 503822 78620483

INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement is entered into as of December 30, 2005 by and between SQUARE 1 BANK ("Bank") and IRVINE SENSORS CORPORATION, a Delaware corporation ("Grantor").

RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodations to Grantor (the "Loans") in the amounts and manner set forth in that certain Loan and Security Agreement by and between Bank and Grantor dated of even date herewith (as the same may be amended, modified or supplemented from time to time, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in certain Copyrights, Trademarks and Patents to secure the obligations of Grantor under the Loan Agreement.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement and all other agreements now existing or hereafter arising between Grantor and Bank, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

To secure its obligations under the Loan Agreement and under any other agreement now existing or hereafter arising between Grantor and Bank, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its Intellectual Property Collateral (including without limitation those Copyrights, Patents and Trademarks listed on Schedules A, B and C hereto), and including without limitation all proceeds thereof (such as, by way of example but not by way of limitation, license royalties and proceeds of infringement suits), the right to sue for past, present and future infringements, all rights corresponding thereto throughout the world and all re-issues, divisions continuations, renewals, extensions and continuations-in-part thereof.

This security interest is granted in conjunction with the security interest granted to Bank under the Loan Agreement. The rights and remedies of Bank with respect to the security interest granted hereby are in addition to those set forth in the Loan Agreement and the other Loan Documents, and those which are now or hereafter available to Bank as a matter of law or equity. Each right, power and remedy of Bank provided for herein or in the Loan Agreement or any of the Loan Documents, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right, power or remedy provided for herein and the exercise by Bank of any one or more of the rights, powers or remedies provided for in this Intellectual Property Security Agreement, the Loan Agreement or any of the other Loan Documents, or now or hereafter existing at law or in equity, shall not preclude the simultaneous or later exercise by any person, including Bank, of any or all other rights, powers or remedies.

Grantor represents and warrants that Exhibits A, B, and C attached hereto set forth any and all intellectual property rights in connection to which Grantor has registered or filed an application with either the United States Patent and Trademark Office or the United States Copyright Office, as applicable.

This Agreement may be executed in two or more counterparts, each of which shall be deemed an original but all of which together shall constitute the same instrument.

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

IRVINE SENSORS CORPORATION

By: _____

Title: CFO

Address of Grantor:

3001 Red Hill Ave., Bldg. 4-108
Costa Mesa, CA 92626

Attn: Chief Executive Officer

BANK:

SQUARE 1 BANK

By: _____

Title: SVP / Regional Manager

Address of Bank:

406 Blackwell Street, Suite 240
Crowe Building
Durham, NC 27701

Attn: Manager

EXHIBIT A

Copyrights

	Description	Registration Number	Registration Date

EXHIBIT B

Patents

Description	Patent Application No./Issued Patent No.	Date
Stackable Layers Containing Ball Grid Array Packages	6967411	11/22/2005
Cryopump Piston Position Tracking	6912862	7/5/2005
Method and Apparatus for Temperature Compensation of an Uncooled Focal Plane Array	6891160	5/10/2005
Wearable Biomonitor With Flexible Thinned Integrated Circuit	11/003429	12/6/2004
Field Programmable Gate Array With a Variably Wide Word Width Memory	6856167	2/15/2005
High Speed Multi-Stage Switching Network Formed From Stacked Switching Layers	6829237	12/7/2004
Method and Apparatus for Connecting Vertically Stacked Integrated Circuit Chips	6806559	10/19/2004
Method of Making Stackable Layers Containing Encapsulated Integrated Circuit Chips With One or More Overlaying Interconnect Layers	6797537	9/28/2004
Stackable Layers Containing Encapsulated Integrated Circuit Chips With One or More Overlying Interconnect Layers	6784547	8/31/2004
Multilayer Modules With Flexible Substrates	6734370	5/11/2004
Stacking of Multilayer Modules	6717061	4/6/2004
Stackable Microcircuit Layer Formed From a Plastic Encapsulated Microcircuit	6706971	3/16/2004
Method of Producing a High Quality, High Resolution Image From a Sequence of Low quality, Low Resolution Images That Are Undersampled and Subject to Jitter	6650704	11/18/2003
Retro-Reflector Warm Stop for Uncooled Thermal Imaging Cameras and Method of Using the Same	6596997	7/22/2003
Stack of Multilayer Modules With Heat-Focusing Metal Layer	6560109	5/6/2003
Method and Apparatus for Temperature Compensation of an Uncooled Focal Plane Array	6476392	11/5/2002
Multi-Axis Micro Gyro Structure	6578420	6/17/2003
Neural Processing Module With Input Architectures That Make Maximal Use of a Weighted Synapse Array	6389404	5/14/2002
Stackable Layers Containing Encapsulated Chips	6117704	9/12/2000
Stack of Equal Layer Neo-Chips Containing Encapsulated IC Chips of Different Sizes	6072234	6/6/2000

Description	Patent Application No./Issued Patent No.	Date
Multi-Element Micro Gyro	6089089	7/18/2000
IC Stack Utilizing Secondary Leadframes	6028352	2/22/2000
IC Stack Utilizing BGA Contacts	6014316	1/11/2000
Multi-Element Micro Gyro	5955668	9/21/1999
Stackable Layers Containing Encapsulated IC Chips	5953588	9/14/1999
Self-Aligning Optical Beam System	5745631	4/28/1998
Stackable Layers Containing Encapsulated IC Chips	6195268	2/27/2001
Stackable Modules and Multimodular Assemblies	5701233	12/23/1997
3D Stack of IC Chips Having Leads Reached by Vias Through Passivation Covering Access Plane	5688721	11/18/1997
Sensing and Selecting Observed Events for Signal Processing	5635705	6/3/1997
Stack of IC Chips in Lieu of Single IC Chip	5581498	12/3/1996
Infrared Wireless Communication Between Electronic System Components	5508836	4/16/1996
Electronic Module Comprising a Stack of IC Chips Each Interacting with an IC Chip Secured to the Stack	5432729	7/11/1995
Apparatus for Segmenting Stacked IC Chips	5432318	7/11/1995
Non-Conductive End Layer for Integrated Stack of IC Chips	5424920	6/13/1995
Fabrication of Dense Parallel Solder Bump Connections	5406701	4/18/1995
Module Comprising IC Memory Stack Dedicated to and Structurally Combined With an IC Microprocessor Chip	5347428	9/13/1994
Apparatus and System for Controllably Varying Image Resolution to Reduce Data Output	5304790	4/19/1994
Method for Fabricating Stacks of IC Chips by Segmenting a Larger Stack	5279991	1/18/1994
Hardware for Electronic Neural Network	5235672	8/10/1993
Method of Fabricating Electronic Circuitry Unit Containing Stacked IC Layers Having Lead Rerouting	5104820	4/14/1992
Analog to Digital Conversion on Multiple Channel IC Chips	5045685	9/3/1991
High-Density Electronic Modules – Process and Product	4983533	1/8/1991
Bonding of Aligned Conductive Bumps on Adjacent Surfaces	4912545	3/27/1990
Pixel Displacement by Series-Parallel Analog Switching	4814629	3/21/1989
Thermal Imager Incorporating Electronics Module Having Focal Plan Sensor Mosaic	4806761	2/21/1989
Pre-Amplifier in Focal Plane Detector Array	4791286	12/13/1988

Description	Patent Application No./Issued Patent No.	Date
Multiple Detector Viewing of Pixels Using Parallel Time Delay and Integration Circuitry	4779005	10/18/1988
High Density Electronic Package Comprising Stacked Sub-Modules	4764846	8/16/1988
High-Density Electronic Modules & MDash; Process and Product	4706166	11/10/1987
Apparatus and Method for Fabricating Modules Comprising Stacked Circuit – Carrying Layers	4704319	11/3/1987
Combined Staring and Scanning Photodetector Sensing System Having Both Temporal and Spatial Filtering	4675532	6/23/1987
Detector Array Module Fabrication Process	4672737	6/16/1987
High-Density Electronic Processing Package & MDash; Structure and Fabrication	4646128	2/24/1987
Method for Fabricating Modules Comprising Uniformly Stacked, Aligned Circuit-Carrying Layers	4617160	10/14/1086
Constant Current Source for Integrated Circuits	4596948	6/24/1986
Pre-Amplifier in Focal Plane Detector Array	4555623	11/26/1985
Detector Array ModuleStructure and Fabrication	4551629	11/5/1985
High-Density Electronic Processing Package-Structure and Fabrication	4525921	7/2/1985
Multiplexer Circuitry for High Density Analog Signals	4490626	12/25/1984
Detector Array Focal Plane Configuration	4403238	9/6/1983
Detector Array Module-Structure and Fabrication	4354107	10/12/1982
Detector Array Module Fabrication	4352715	10/5/1982
Method of Fabricating a Multi-Layer Structure for Detector Array Module	4304624	12/8/1981
Three-Dimensional Imaging Device Incorporating Stacked Layers Containing Microelectronic Circuits	10/805849	3/22/2004
Neo-Wafer Device and Method	10/703177	11/6/2003
Wearable Biomonitor with Flexible Thinned Integrated Circuit	10/197006	7/16/2002
Stocked Microelectronic Module with Vertical Interconnect Vias	10/663371	9/16/2003
Method for Effectively Embedding Various Integrated Circuits within Field Programmable Gate Arrays	10/346363	1/17/2003

EXHIBIT C

Trademarks

Description	Registration/ Application Number	Registration/ Application Date
CAM-NOIR	2,728,041	6/17/2003
POD-IR	78-620,483	5/1/2005
PMTV (block letters)	78-544,618	1/10/2005
Irvine Sensors Corporation (and design)	76-552,662	10/20/2003
Redhawk Vision	2490859	9/18/2001