

06-01-2006

FORM PTO-1594

(Rev. 07/05)

OMB No. 0651-0027 (exp. 06/30/2008)

REC

U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

103248162

To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies):

Tanisys Technology Inc

- ☐ Individual(s) ☐ Association
☐ General Partnership ☐ Limited Partnership
☒ Corporation-State
☐ Other

Additional name(s) of conveying parties attached? ☐ Yes ☒ No

3. Nature of conveyance/ Execution Date(s):

Execution Date(s): 7/29/2005

- ☐ Assignment ☐ Merger
☒ Security Agreement ☐ Change of Name
☐ Other

2. Name and address of receiving party(ies):

Additional name(s) of conveying parties attached? ☐ Yes ☒ No

Name: SILICON VALLEY BANK

Internal Address HF 154

Street Address: 3003 TASMAN DRIVE

City SANTA CLARA

State CA

Country USA

Zip 95054

- ☐ Association Citizenship
☐ General Partnership Citizenship
☐ Limited Partnership Citizenship
☒ Corporation Citizenship
☐ Other Citizenship

If assignee is not domiciled in the United States, a domestic representative designation is attached: ☐ Yes ☐ No
 (Designations must be a separate document from assignment)

4. Application number(s) or registration number(s) and identification or description of the Trademark:

A. Trademark Application No.(s)

B. Trademark Registration No.(s)

2,036,464

2,026,399

1,959,395

C. Identification or Description of Trademark(s) (and Filing Date if Application or Registration Number is unknown):

Additional sheets attached? ☐ Yes ☒ No

"See attached"

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Silicon Valley Bank

Internal Address: Loan Collateral HF154

Street Address: 3003 Tasman Dr.

City: Santa Clara State: CA ZIP: 95054

Phone Number: (408) 654-4042

Fax Number: (408) 654-6313

Email Address: ldc@svbank.com

6. Total number of applications and registrations involved: 3

7. Total fee (37 CFR 2.6 (b)(6) & 3.41): \$ 90.00

- ☐ Authorized to be charged by credit card
☐ Authorized to be charged to deposit account
☒ Enclosed

8. Payment Information:

a. Credit Card Last 4 Numbers
 Expiration Date

b. Deposit Account Number
 Authorized User Name

9. Signature.

Manuel Hgareda

Signature

5/22/06

Date

Manuel Hgareda c/o Shannon Hubbard

Name of Person Signing

Total number of pages including cover sheet, attachments, and document: 3

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
 Mail Stop Assignment Recordation Services, Director of the USPTO, P.O. Box 1450, Alexandria, VA 22313-1450

TRADEMARK
 REEL: 003349 FRAME: 0733

00000000 2036464

05/31/2006 09:09:00

01 FC:6520
02 FC:652040.00 DP
50.00 DP

OFFICE OF PUBLIC RECORDS
 2006 MAY 30 PM 5:33
 FINANCE SECTION

5302

INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement dated as of the Effective Date (as defined in the Loan Agreement) is between SILICON VALLEY BANK ("Bank") and Tanisys Technology, Inc. ("Grantor").

RECITALS

A. Bank will make advances to Grantor ("Loans") as described in the Loan and Security Agreement (as amended from time to time, the "Loan Agreement"), but only if Grantor grants Bank a security interest in its Copyrights, Trademarks, Patents, and Mask Works and other intellectual property (the "Intellectual Property Collateral"). Capitalized terms not otherwise defined herein shall have the meaning set forth in the Loan Agreement.

B. Grantor has granted Bank a security interest in all of its right, title and interest, presently existing or later acquired to all the Collateral.


AGREEMENT

Grantor grants Bank a security interest in all of its right, title and interest in its Intellectual Property Collateral (such as the Copyrights, Patents, Trademarks and Mask Works listed on Schedules A, B, C and D), and all proceeds (such as license royalties and proceeds of infringement suits), the right to sue for past, present and future infringements rights throughout the world and all reissues, divisions, continuations, renewals, extensions and continuations-in-part.

This security interest is granted in conjunction with the security interest granted under the Loan Agreement. Bank's rights and remedies in the security interest are in addition to those in the Loan Agreement and the other Loan Documents, and those available in law or equity. Bank's rights powers and interests are cumulative with every right, power or remedy provided here. Bank's exercise of its rights, powers or remedies in this Agreement, the Loan Agreement or any other Loan Document, does not preclude the simultaneous or later exercise of any or all other right, power or remedy.

BANK:

SILICON VALLEY BANK


(Signature)
Vice President
(Title)

GRANTOR:

TANISYS TECHNOLOGY, INC.,
a Wyoming corporation

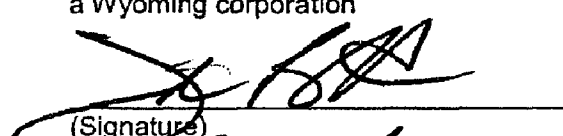

(Signature)
President & CEO
(Title)

EXHIBIT A

Copyrights

| <u>Description</u> | Registration/Application <u>Number</u> | Registration/Application <u>Date</u> |
|--------------------|---|---|
|--------------------|---|---|

NONE

EXHIBIT B

Patents

Description

Registration/Application
Number

Registration/Application
Date

SEE ATTACHED LIST

Tanisys Patent Status Report

US PENDING

BB Case No: 021579.0204.1
Client Ref No: 021579.0204.1
Country: United States of America
Owner: Tanisys Technology, Inc.
Status: Allowed
Case Type: CVP
Application No: 09/966541
Filing Date: 9/27/2001
Patent No.:
Issue Date:
Title: Method and System for Distributed Testing of Electronic Devices
Inventors: Hunter, Paul R.; Klein, Joseph C.; Lawrence, Archer R.; Little, Jack C.

Related Cases:

021579.0204 US Closed

Outstanding Actions:

| | |
|---------------------------|-------------|
| Fee Due in 1 Month | 28-Feb-2005 |
| Notice/Publ. Fee Reminder | 28-Feb-2005 |
| Notice/Publ. Fee Due | 30-Mar-2005 |
| Issue Fee Due | 30-Mar-2005 |
| Comments/Allowance | 30-Mar-2005 |

Tanisys Patent Status Report

US GRANTED

BB Case No.: 021579.0104
 Client Ref No.:
 Country: United States of America
 Owner: Tanisys Technology, Inc.
 Status: Granted

Title: Method and System for Testing Rambus Memory Modules

Case Type: ORD
 Application No: 09/267731
 Filing Date: 3/15/1999
 Patent No.: 6285962
 Issue Date: 9/4/2001

Inventors: Hunter, Paul R.

Related Cases:

021579.0104 V1 US Closed; 021579.0166 US Abandoned; 021579.0182
 WO Abandoned; 021579.0208 US Granted

Outstanding Actions:

| | |
|----------|-------------|
| Tax 7.5 | 04-Mar-2001 |
| Tax 11.5 | 04-Mar-2011 |

BB Case No.: 021579.0105

Client Ref No:

Country: United States of America
 Owner: Tanisys Technology, Inc.
 Status: Granted

Case Type: ORD
 Application No: 09/193804
 Filing Date: 11/17/1998
 Patent No.: 5999468
 Issue Date: 12/7/1999

Title:

Method and System for Identifying a Memory Module Configuration

Inventors: Lawrence, Allen B.

Related Cases:

Outstanding Actions:

| | |
|----------|-------------|
| Tax 7.5 | 07-Jun-2001 |
| Tax 11.5 | 07-Jun-2011 |

BB Case No.: 021579.0113

Client Ref No:

Country: United States of America
 Owner: Tanisys Technology, Inc.
 Status: Granted

Case Type: ORD
 Application No: 08/895305
 Filing Date: 7/16/1997
 Patent No.: 5812472
 Issue Date: 9/22/1998

Title:

Nested Loop Method of Identifying Synchronous Memories

Inventors: Lawrence, Archer R.; Little, Jack C.

Related Cases:

021579.0114 WO Abandoned; 021579.0115 TW Granted

Outstanding Actions:

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| Tax 7.5 | 22-Mar-2001 |
| Tax 11.5 | 22-Mar-2011 |

Tanisys Patent Status Report

US GRANTED

BB Case No.: 021579.0116
 Client Ref No:
 Country: United States of America
 Owner: Tanisys Technology, Inc.
 Status: Granted
 Case Type: ORD
 Application No: 08/895307
 Filing Date: 7/16/1997
 Patent No.: 5995424
 Issue Date: 11/30/1999
 Title: Synchronous Memory Test System
 Inventors: Lawrence, Archer Russell; Little, Jack C.
 Related Cases:
 021579.0117 WO Abandoned; 021579.0118 TW Granted; 021579.0139 US Granted; 021579.0140 US Granted
 Outstanding Actions:
 Tax 7.5 30-May-200
 Tax 11.5 30-May-201

BB Case No.: 021579.0119
 Client Ref No:
 Country: United States of America
 Owner: Tanisys Technology, Inc.
 Status: Granted
 Case Type: CPA
 Application No: 08/895550
 Filing Date: 7/16/1997
 Patent No.: US6182253B1
 Issue Date: 1/30/2001
 Title: Synchronous Memory Identification System
 Inventors: LITTLE, JACK C; LAWRENCE, ARCHER
 Related Cases:
 021579.0119 US Closed
 Outstanding Actions:
 Tax 7.5 30-Jul-2008
 Tax 11.5 30-Jul-2012

BB Case No.: 021579.0122
 Client Ref No:
 Country: United States of America
 Owner: Tanisys Technology, Inc.
 Status: Granted
 Case Type: ORD
 Application No: 09/033285
 Filing Date: 3/2/1998
 Patent No.: 6008684
 Issue Date: 12/28/1999
 Title: Parametric Test System and Method
 Inventors: Jett, Allen (nm); Lawrence, Archer R.
 Related Cases:
 Outstanding Actions:
 Tax 7.5 28-Jun-2007
 Tax 11.5 28-Jun-2011

Tanisys Patent Status Report

US GRANTED

BB Case No.: 021579.0123
Client Ref No:
Country: United States of America
Owner: Tanisys Technology, Inc.
Status: Granted

Case Type: ORD
Application No: 09/032958
Filing Date: 3/2/1998
Patent No.: 5956280
Issue Date: 9/21/1999

Title: Contact Test Method and System for Memory Testers

Inventors: Lawrence, Allen B.

Related Cases:

Outstanding Actions:

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| Tax 7.5 | 21-Mar-200 |
| Tax 11.5 | 21-Mar-201 |

BB Case No.: 021579.0125
Client Ref No:
Country: United States of America
Owner: Tanisys Technology, Inc.
Status: Granted

Case Type: ORD
Application No: 09/032968
Filing Date: 3/2/1998
Patent No.: 6067648
Issue Date: 5/23/2000

Title: Programmable Pulse Generator

Inventors: Hunter, Paul R.; Lawrence, Archer R.; Little, Jack C.

Related Cases:

Outstanding Actions:

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| Tax 7.5 | 23-Nov-200 |
| Tax 11.5 | 23-Nov-201 |

BB Case No.: 021579.0126
Client Ref No:
Country: United States of America
Owner: Tanisys Technology, Inc.
Status: Granted

Case Type: ORD
Application No: 09/033364
Filing Date: 3/2/1998
Patent No.: 6064948
Issue Date: 5/16/2000

Title: Tester Systems

Inventors: Hunter, Paul R.; Lawrence, Archer R.; Little, Jack C.; West, Michael S.

Related Cases:

Outstanding Actions:

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| Tax 7.5 | 16-Nov-200 |
| Tax 11.5 | 16-Nov-201 |

Friday, February 18, 2005

Tanisys Patent Status Report

US GRANTED

BB Case No.: 021579.0139
Client Ref No:
Country: United States of America
Owner: Tanisys Technology, Inc.
Status: Granted

Case Type: DIV
Application No: 09/115386
Filing Date: 7/14/1998
Patent No.: 5914902
Issue Date: 6/22/1999

Title: Synchronous Memory Tester

Inventors: Lawrence, Archer R.; Little, Jack C.

Related Cases:
021579.0116 US Granted

Outstanding Actions:

| | |
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| Tax 7.5 | 22-Dec-2006 |
| Tax 11.5 | 22-Dec-2010 |

BB Case No.: 021579.0140
Client Ref No:
Country: United States of America
Owner: Tanisys Technology, Inc.
Status: Granted

Case Type: DIV
Application No: 09/115001
Filing Date: 7/14/1998
Patent No.: 5912852
Issue Date: 6/15/1999

Title: Synchronous Memory Test Method

Inventors: Lawrence, Archer R.; Little, Jack C.

Related Cases:
021579.0116 US Granted

Outstanding Actions:

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| Tax 7.5 | 15-Dec-2006 |
| Tax 11.5 | 15-Dec-2010 |

BB Case No.: 021579.0208
Client Ref No:
Country: United States of America
Owner: Tanisys Technology, Inc.
Status: Granted

Case Type: CON
Application No: 09/943721
Filing Date: 8/31/2001
Patent No.: US6480799B2
Issue Date: 11/12/2002

Title: Method and System for Testing Rambus Memory Modules

Inventors: Hunter, Paul R.

Related Cases:
021579.0104 US Granted

Outstanding Actions:

| | |
|----------|-------------|
| Tax 3.5 | 12-May-2006 |
| Tax 7.5 | 12-May-2011 |
| Tax 11.5 | 12-May-2011 |

Tanisys Patent Status Report

FOREIGN GRANTED

BB Case No.: 021579.0115
 Client Ref No:
 Country: Taiwan
 Owner: Tanisys Technology, Inc.
 Status: Granted
 Related Cases:
 021579.0113 US Granted

Case Type: ORD
 Application No: 87111551
 Filing Date: 7/16/1998
 Patent No.: 132190
 Issue Date: 9/7/2001

Title: Nested Loop Method of Identifying Synchronous Memories

Inventors: Lawrence, Archer R.; Little, Jack C.

Outstanding Actions:
 Annuity Fee Due 19-Apr-2005

BB Case No.: 021579.0118
 Client Ref No:
 Country: Taiwan
 Owner: Tanisys Technology, Inc.
 Status: Granted
 Related Cases:
 021579.0116 US Granted

Case Type: ORD
 Application No: 87111552
 Filing Date: 7/16/1998
 Patent No.: 118906
 Issue Date: 12/18/2000

Title: Synchronous Memory Test System

Inventors: Lawrence, Archer R.; Little, Jack C.

Outstanding Actions:
 Annuity Fee Due 20-Jul-2005

BB Case No.: 021579.0121
 Client Ref No:
 Country: Taiwan
 Owner: Tanisys Technology, Inc.
 Status: Granted
 Related Cases:
 021579.0119 US Closed

Case Type: ORD
 Application No: 87111553
 Filing Date: 7/16/1998
 Patent No.: 133631
 Issue Date: 10/4/2001

Title: Synchronous Memory Identification System

Inventors: Lawrence, Archer R.; Little, Jack C.

Outstanding Actions:
 Annuity Fee Due 14-May-2005

EXHIBIT C

Trademarks

| <u>Description</u> | <u>Registration/Application Number</u> | <u>Registration/Application Date</u> |
|--------------------|--|--|
| TANISYS | 1,959,395 | 2/26/97 |
| DARKHORSE | 2,036,464 | 2/11/97 |
| 1ST TECH | 2,026,399 | 12/31/96 |

EXHIBIT D

Mask Works

| <u>Description</u> | Registration/Application <u>Number</u> | Registration/Application <u>Date</u> |
|--------------------|---|---|
|--------------------|---|---|

NONE