FORM PTO-1594
COMMERCE
(Rev. 07/05)
OMB No. 0651-0027 (exp. 06/30/2008)

RECOR

01-15-2008

103475296

U.S. DEPARTMENT OF
States Patent and Trademark Office

To the Director of the U.S. Patent and Trade

nts or the new address (es) below.

1. Name of conveying party(ies):
SILICON VALLEY BANK

1-11-08

☐ Individual(s) ☐ Association
☐ General Partnership ☐ Limited Partnership

☒ Corporation-State
☐ Other

Additional name(s) of conveying parties attached? ☐Yes ☒ No

3. Nature of conveyance/ Execution Date(s):

Execution Date(s): **January 7, 2008**

☐ Assignment ☐Merger

☐Security Agreement ☐ Change of Name

☒ Other : **Release**

ng party(ies):
parties attached? ☐Yes ☒ No

Name: **Intrinsity, Inc.**

Internal Address

Street Address: **11612 Bee Caves Road Ste II 200**

JAN 11 2008

City: **Austin**
State: **TX**
Country: **USA**
Zip: **78738**

☐ Association Citizenship
☐ General Partnership Citizenship
☐ Limited Partnership Citizenship
☒ Corporation Citizenship
☐ Other Citizenship

If assignee is not domiciled in the United States, a domestic representative designation is attached: ☐ Yes ☒ No
(Designations must be a separate document from assignment)

4. Application number(s) or registration number(s) and identification or description of the Trademark:

A. Trademark Application No.(s)	B. Trademark Registration No.(s)
78465981 78466678	**2708216 2832962 2799110**
78933918 78466709	**2738968 2769500 2801275**
78934524	**2780706 2728084 2765942**
78466651	**2906315 2748597**

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: **Silicon Valley Bank**

Internal Address: **HF154**

Street Address: **3003 Tasman Drive**

City: **Santa Clara** State: **CA** ZIP: **95054**

Phone Number: **(408) 919-0310**

Fax Number: **(408) 654-6313**

Email Address: **svaldivia@svb.com**

6. Total number of applications and registrations involved: 17

7. Total fee (37 CFR 2.6 (b)(6) & 3.41): **$ 680.00**
☐ Authorized to be charged by credit card
☐ Authorized to be charged to deposit account
☒ Enclosed

8. Payment Information:

a. Credit Card Last 4 Numbers
Expiration Date

b. Deposit Account Number
Authorized User Name

9. Signature.

Signature

January 7, 2008
Date

Susana Valdivia
Name of Person Signing

Total number of pages including cover sheet, attachments, and document:

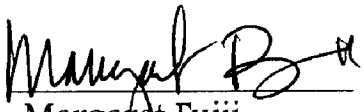
Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to: Mail Stop Assignment Recordation Services, Director of the USPTO, P.O. Box 1450, Alexandria, VA 22313-1450

RELEASE OF SECURITY AGREEMENT COVERING
INTERESTS IN TRADEMARKS

Silicon Valley Bank ("Secured Party"), hereby releases its security interest in the interests of **Intrinsity, Inc.** ("Assignor") in the trademarked works set forth in that certain **Intellectual Property And Security Agreement** dated, January 1, 2007, executed by Assignor in favor of Secured Party recorded with the United States Department of Commerce, Patent and Trademark Office on February 12, 2007, Reel 003485, Frame 0227.

Date: **Intrinsity, Inc.**

SILICON VALLEY BANK

By: 
Name: Margaret Fujii
Title: Operations Department Manager

h:\docs\ipagrmts\3release

INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement (this "Agreement")dated as of ~~November ___~~ January 1, 2007, 2006 (as defined in the Loan Agreement) is between **SILICON VALLEY BANK** ("Bank") and **INTRINSITY, INC.**, a Texas corporation ("Grantor").

RECITALS

A. Bank will make advances to Grantor ("Loans") as described in that certain Loan and Security Agreement dated as of even date herewith (as the same may from time to time be further amended, modified, supplemented or restated, the "Loan Agreement"). Capitalized terms not otherwise defined herein shall the meaning set forth in the Loan Agreement.

B. Bank's agreement to make such advances is subject to, among other things, Grantor's granting to Bank a security interest in Grantor's Copyrights, Trademarks, Patents, and Mask Works and other intellectual property (the "Intellectual Property Collateral").

C. Grantor has granted Bank a security interest in all of its right, title and interest, presently existing or later acquired to all the Collateral.

AGREEMENT

Grantor grants Bank a security interest in all of its right, title and interest in its Intellectual Property Collateral (such as the Copyrights, Patents, Trademarks and Mask Works listed on Schedules A, B, C and D), and all proceeds (such as license royalties and proceeds of infringement suits), the right to sue for past, present and future infringements rights throughout the world and all reissues, divisions, continuations, renewals, extensions and continuations-in-part.

This security interest is granted in conjunction with the security interest granted under the Loan Agreement. Bank's rights and remedies in the security interest are in addition to those in the Loan Agreement and the other Loan Documents, and those available in law or equity. Bank's rights powers and interests are cumulative with every right, power or remedy provided here. Bank's exercise of its rights, powers or remedies in this Agreement, the Loan Agreement or any other Loan Document, does not preclude the simultaneous or later exercise of any or all other right, power or remedy.

BANK:

SILICON VALLEY BANK

(Signature)

Vice President
(Title)

GRANTOR:

INTRINSITY, INC.,
a Texas corporation

(Signature)

CEO
(Title)

EXHIBIT A

Copyrights

Description	Registration/Application Number	Registration/Application Date
NONE		

EXHIBIT B

Patents

Description	Registration/Application Number	Registration/Application Date

Client-Matter/Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
31876-0101/0 United States of America	ORD	09/209,967 10-Dec-1998		6,124,735 26-Sep-2000	Granted 10-Dec-2018
		Title: Method and Apparatus for a N-Nary Logic Circuit Using Capacitance Isolation			
31876-0102/0 United States of America	ORD	09/209,207 10-Dec-1998		6,107,835 22-Aug-2000	Granted 10-Dec-2018
		Title: Operation-Independent Power Consumption			
31876-0103/0 United States of America	ORD	09/073,478 06-May-1998		6,202,194 13-Mar-2001	Granted 06-May-2018
		Title: Method and Apparatus for Routing 1 of N Signals			
31876-0104/0 United States of America	ORD	09/073,479 06-May-1998		6,211,456 03-Apr-2001	Granted 06-May-2018
		Title: Method and Apparatus for Routing 1 of 4 Signals			
31876-0106/0 United States of America	ORD	09/019,278 05-Feb-1998		6,911,846 28-Jun-2005	Granted 07-Aug-2021
		Title: Method and Apparatus for a 1 of N Signal			
31876-0107/0 United States of America	ORD	09/019,244 05-Feb-1998		6,069,497 30-May-2000	Granted 05-Feb-2018
		Title: Method and Apparatus for an N-Nary Logic Circuit Using 1 of N Signals			
31876-0108/0 United States of America	ORD	09/179,330 27-Oct-1998		6,118,304 12-Sep-2000	Granted 27-Oct-2018
		Title: Method and Apparatus for Logic Synchronization			
31876-0109/1 United States of America	ORD	09/206,905 07-Dec-1998		6,429,795 06-Aug-2002	Granted 07-Dec-2018
		Title: Method and Apparatus for Transforming Pseudorandom Binary Patterns into Test Stimulus Patterns Appropriate for Circuits Having 1 of N encoded Inputs			
31876-0111/1 United States of America	ORD	09/206,900 07-Dec-1998		6,295,622 25-Sep-2001	Granted 07-Dec-2018
		Title: Method and Apparatus for Transforming Pseudorandom Binary Patterns into Test Stimulus Patterns Appropriate for Circuits Having 1 of N encoded Inputs			
31876-0112/0 United States of America	ORD	09/124,207 28-Jul-1998		6,088,830 11-Jul-2000	Granted 28-Jul-2018
		Title: Method and Apparatus for Speed Detection Circuitry			

Client-Matter/Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
31876-0113/1 United States of America	ORD	09/181,406 28-Oct-1998		6,460,134 01-Oct-2002	Granted 28-Oct-2018
Title: A Method and Apparatus for a Late Pipeline Enhanced Floating Point Unit					
31876-0117/1 United States of America	ORD	09/195,752 18-Nov-1998		6,301,600 09-Oct-2001	Granted 18-Nov-2018
Title: Method and Apparatus for a Dynamic Partitionable Saturating Adder/Subtractor					
31876-0118/1 United States of America	ORD	09/195,779 18-Nov-1998		6,260,131 10-Jul-2001	Granted 18-Nov-2018
Title: Method and Apparatus for TLB Memory Ordering					
31876-0120/1 United States of America	ORD	09/195,757 18-Nov-1998		6,334,183 25-Dec-2001	Granted 18-Nov-2018
Title: Method and Apparatus for Partial Register Write Handling					
31876-0121/1 United States of America	ORD	09/122,504 24-Jul-1998		6,209,076 27-Mar-2001	Granted 24-Jul-2018
Title: Method and Apparatus for Two Stage Address Generation					
31876-0123/1 United States of America	ORD	09/191,813 13-Nov-1998		6,272,653 07-Aug-2001	Granted 13-Nov-2018
Title: Method and Apparatus for Built-In Self-Test of Logic Circuitry					
31876-0125/1 United States of America	ORD	09/120,775 22-Jul-1998		6,185,593 06-Feb-2001	Granted 22-Jul-2018
Title: Method and Apparatus for Parallel Normalization and Rounding Technique for Floating Point Arithmetic Operations					
31876-0126/0 United States of America	ORD	09/120,771 22-Jul-1998		6,173,299 09-Jan-2001	Granted 22-Jul-2018
Title: A Method and Apparatus for Selecting an Intermediate Result for Parallel Normalization and Rounding Technique for Floating Point Arithmetic Operations					
31876-0127/0 United States of America	ORD	09/019,355 05-Feb-1998		6,066,965 23-May-2000	Granted 05-Feb-2018
Title: Method and Apparatus for an N-Nary Logic Circuit Using 1 of 4 Signals					
31876-0129/1 United States of America	ORD	09/373,516 12-Aug-1999		6,360,315 19-Mar-2002	Granted 12-Aug-2019
Title: Method and Apparatus that Supports Multiple Assignment Code					

Client-Matter/Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
31876-0130/0 United States of America	ORD	09/120,814 22-Jul-1998		6,175,847 16-Jan-2001	Granted 22-Jul-2018
			Title: Shifting for Parallel Normalization and Rounding Technique for Floating Point Arithmetic Operations		
31876-0131/0 United States of America	ORD	09/209,935 11-Dec-1998		6,334,136 25-Dec-2001	Granted 11-Dec-2018
			Title: Dynamic 3-Level Partial Result Merge Adder		
31876-0132/0 United States of America	ORD	09/206,830 07-Dec-1998		6,347,327 12-Feb-2002	Granted 07-Dec-2018
			Title: Method and Apparatus for N-nary Incrementor		
31876-0133/0 United States of America	ORD	09/179,745 27-Oct-1998		6,288,589 11-Sep-2001	Granted 27-Oct-2018
			Title: Method and Apparatus for Generating Clock Signals		
31876-0134/0 United States of America	ORD	09/181,405 28-Oct-1998		6,275,838 14-Aug-2001	Granted 28-Oct-2018
			Title: A Method and Apparatus for an Enhanced Floating Point Unit with Graphics and Integer Capabilities		
31876-0135/0 United States of America	ORD	09/207,806 09-Dec-1998		6,104,642 15-Aug-2000	Granted 09-Dec-2018
			Title: Method and Apparatus for 1 of 4 Register File Design		
31876-0136/0 United States of America	ORD	09/210,408 11-Dec-1998		6,289,497 11-Sep-2001	Granted 11-Dec-2018
			Title: Method and Apparatus for N-nary Hardware Description Language		
31876-0137/0 United States of America	ORD	09/150,389 09-Sep-1998		6,118,716 12-Sep-2000	Granted 09-Sep-2018
			Title: Method and Apparatus for an Address Triggered RAM Circuit		
31876-0139/0 United States of America	ORD	09/179,626 27-Oct-1998		6,233,707 15-May-2001	Granted 27-Oct-2018
			Title: Method and Apparatus that Allows the Logic State of a Logic Gate to be Tested when Stopping or Starting the Logic Gate's clock		
31876-0140/0 United States of America	ORD	09/405,618 24-Sep-1999		7,031,897 18-Apr-2006	Granted 13-Mar-2021
			Title: Software Modeling of Logic Signals Capable of Holding More than Two Values		

Client-Matter/Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
31876-0144/0 United States of America	ORD	09/120,776 22-Jul-1998		6,151,615 21-Nov-2000	Granted 22-Jul-2018
			Title: A Method and Apparatus for Formatting an Intermediate Result for Parallel Normalization and Rounding Technique for Floating Point Arithmetic Operations		
31876-0145/0 United States of America	ORD	09/206,463 07-Dec-1998		6,269,387 31-Jul-2001	Granted 07-Dec-2018
			Title: Method and Apparatus for a 3-Stage 32-Bit Adder		
31876-0146/0 United States of America	ORD	09/150,720 10-Sep-1998		6,219,687 17-Apr-2001	Granted 10-Sep-2018
			Title: Method and Apparatus for an N-Nary Sum/HPG Gate		
31876-0147/0 United States of America	ORD	09/206,539 07-Dec-1998		6,324,239 27-Nov-2001	Granted 07-Dec-2018
			Title: Method and Apparatus for a 1 of 4 Shifter		
31876-0148/0 United States of America	ORD	09/186,843 05-Nov-1998		6,275,841 14-Aug-2001	Granted 05-Nov-2018
			Title: 1 of 4 Multiplier		
31876-0149/0 United States of America	ORD	09/123,742 28-Jul-1998		6,404,233 11-Jun-2002	Granted 28-Jul-2018
			Title: Method and Apparatus for Logic Circuit Transition Detection		
31876-0150/0 United States of America	ORD	09/150,717 10-Sep-1998		6,219,686 17-Apr-2001	Granted 10-Sep-2018
			Title: Method and Apparatus for an N-nary Sum/HPG Adder/Subtractor Gate		
31876-0151/0 United States of America	ORD	09/150,829 10-Sep-1998		6,216,146 10-Apr-2001	Granted 10-Sep-2018
			Title: Method and Apparatus for an N-Nary Adder Gate		
31876-0152/0 United States of America	ORD	09/150,575 10-Sep-1998		6,223,199 24-Apr-2001	Granted 10-Sep-2018
			Title: Method and Apparatus for an N-nary HPG Gate		
31876-0153/0 United States of America	ORD	09/150,162 09-Sep-1998		6,069,836 30-May-2000	Granted 09-Sep-2018
			Title: Method and Apparatus for a RAM Circuit having N-NARY Word Line Generation		

Client-Matter/Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
31876-0154/0 United States of America	ORD	09/150,258 09-Sep-1998		6,046,931 04-Apr-2000	Granted 09-Sep-2018
		Title: Method and Apparatus for a RAM Circuit Having N-Nary Output Interface			
31876-0156/0 United States of America	ORD	09/206,906 07-Dec-1998		6,216,147 10-Apr-2001	Granted 07-Dec-2018
		Title: Method and Apparatus for an N-Nary Magnitude Comparator			
31876-0157/0 United States of America	ORD	09/206,631 07-Dec-1998		6,154,120 28-Nov-2000	Granted 07-Dec-2018
		Title: Method and Apparatus for an N-nary Equality Comparator			
31876-0159/0 United States of America	ORD	09/195,751 18-Nov-1998		6,272,514 07-Aug-2001	Granted 18-Nov-2018
		Title: Method and Apparatus for Interruption of Carry Propagation on Partition Boundaries			
31876-0160/0 United States of America	ORD	09/195,024 18-Nov-1998		6,301,597 09-Oct-2001	Granted 18-Nov-2018
		Title: Method and Apparatus for Saturation in an N-nary Adder/Subtractor			
31876-0161/0 United States of America	ORD	09/195,758 18-Nov-1998		6,370,632 09-Apr-2002	Granted 18-Nov-2018
		Title: Method and Apparatus that Enforces a Regional Memory Model in Hierarchical Memory Systems			
31876-0162/0 United States of America	ORD	09/210,410 11-Dec-1998		6,367,065 02-Apr-2002	Granted 11-Dec-2018
		Title: Method and Apparatus for N-nary Logic Circuit Design Tool with Precharge Circuit Evaluation			
31876-0163/0 United States of America	ORD	09/210,024 11-Dec-1998		6,345,381 05-Feb-2002	Granted 11-Dec-2018
		Title: Method and Apparatus for a Logic Circuit Design Tool			
31876-0164/0 United States of America	ORD	09/373,840 13-Aug-1999		6,457,170 24-Sep-2002	Granted 13-Aug-2019
		Title: Software System Build Method and Apparatus that Supports Multiple Users in a Software Development Environment			
31876-0165/1 United States of America	ORD	09/406,016 24-Sep-1999		6,594,803 15-Jul-2003	Granted 24-Sep-2019
		Title: Method and Apparatus that Reports Multiple Status Events with a Single Monitor			

Client-Matter/Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
31876-0167/0 United States of America	CON	09/291,659 14-Apr-1999		6,115,294 05-Sep-2000	Granted 09-Dec-2018
		Title: Method and Apparatus for Multi-bit Register Cell			
31876-0171/1 United States of America	ORD	09/468,760 21-Dec-1999		6,412,085 25-Jun-2002	Granted 21-Dec-2019
		Title: Method and Apparatus for a Special Stress Mode for N-Nary Logic that Initializes the Logic into a Functionally Illegal State			
31876-0172/0 United States of America	ORD	09/406,017 24-Sep-1999		6,889,180 03-May-2005	Granted 13-Mar-2021
		Title: Method and Apparatus for a Monitor that Detects and Reports a Status Event to a Database			
31876-0173/2 United States of America	CON	10/300,289 20-Nov-2002	US20040006753 08-Jan-2004	7,053,664 30-May-2006	Allowed 22-Mar-2024
		Title: Null Value Propagation for FAST14 Logic			
31876-0174/0 United States of America	CIP	09/468,972 21-Dec-1999		6,271,683 07-Aug-2001	Granted 21-Dec-2019
		Title: Dynamic Logic Scan Gate Method and Apparatus			
31876-0178/1 United States of America	ORD	09/496,008 01-Feb-2000		6,622,240 16-Sep-2003	Granted 01-Feb-2020
		Title: Method and Apparatus for Pre-Branch Instruction			
31876-0181/1 United States of America	ORD	09/398,618 17-Sep-1999		6,567,835 20-May-2003	Granted 17-Sep-2019
		Title: Method and Apparatus for a 5:2 Carry-Save-Adder (CSA)			
31876-0182/0 United States of America	ORD	09/374,588 13-Aug-1999		6,438,743 20-Aug-2002	Granted 13-Aug-2019
		Title: Method and Apparatus for Object Cache Registration and Maintenance in a Networked Software Development Environment			
31876-0183/0 United States of America	ORD	09/405,474 24-Sep-1999		6,604,065 05-Aug-2003	Granted 24-Sep-2019
		Title: Multiple-State Simulation for Non-Binary Logic			
31876-0185/2 European Patent Convention	PCT	EP19990951988 12-Oct-1999	EP1135859 26-Sep-2001	EP1135859 07-Apr-2004	Granted 12-Oct-2019
		Title: Method and Apparatus for Logic Synchronization			

Client-Matter/Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
31876-0185/2 France	EPC	EP19990951988 12-Oct-1999	EP1135859 26-Sep-2001	EP1135859 07-Apr-2004	Granted 12-Oct-2019
			Title: Method and Apparatus for Logic Synchronization		
31876-0185/2 Germany	EPC	EP19990951988 12-Oct-1999	EP1135859 26-Sep-2001	EP1135859 07-Apr-2004	Granted 12-Oct-2019
			Title: Method and Apparatus for Logic Synchronization		
31876-0185/1 Japan	PCT	2000-578908 12-Oct-1999			Pending
			Title: Method and Apparatus for Logic Synchronization		
31876-0185/2 United Kingdom	EPC	EP19990951988 12-Oct-1999	EP1135859 26-Sep-2001	EP1135859 07-Apr-2004	Granted 12-Oct-2019
			Title: Method and Apparatus for Logic Synchronization		
31876-0189/1 United States of America	ORD	09/527,653 17-Mar-2000		6,557,021 29-Apr-2003	Granted 17-Mar-2020
			Title: Rounding Anticipator for Floating Point Operations		
31876-0190/0 United States of America	CIP	09/468,759 21-Dec-1999		6,415,405 02-Jul-2002	Granted 21-Dec-2019
			Title: Method and Apparatus for Scan of Synchronized Dynamic Logic Using Embedded Scan Gates		
31876-0194/1 United States of America	ORD	09/546,412 10-Apr-2000		6,499,044 24-Dec-2002	Granted 10-Apr-2020
			Title: Leading Zero/One Anticipator for Floating Point Operations		
31876-0199/1 United States of America	ORD	10/155,042 24-May-2002	2002/0178428 28-Nov-2002	6,732,346 04-May-2004	Granted 12-Oct-2022
			Title: Generation of Route Rules		
31876-0206/1 European Patent Convention	PCT	EP19990966138 10-Jun-2002	EP1236278 04-Sep-2002		Published
			Title: Method and Apparatus for an N-Nary Logic Circuit		
31876-0206/2 Japan	PCT	2001-543857 09-Jun-2002	2004-524713 12-Aug-2004		Published
			Title: Method and Apparatus for an N-Nary Logic Circuit		
31876-0217/0 United States of America	CON	09/458,763 10-Dec-1999		6,252,425 26-Jun-2001	Granted 05-Feb-2018
			Title: Method and Apparatus for an N-Nary Logic Circuit		

Client-Matter/Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
31876-0219/0 United States of America	DIV	09/458,766 10-Dec-1999		6,181,596 30-Jan-2001	Granted 09-Sep-2018
		Title: Method and Apparatus for a RAM Circuit Having N-Nary Output Interface			
31876-0221/0 United States of America	CON	09/503,397 14-Feb-2000		6,349,387 19-Feb-2002	Granted 28-Jul-2018
		Title: Dynamic Adjustment of the Clock Rate in Logic Circuits			
31876-0223/0 United States of America	CON	09/587,729 05-Jun-2000		6,571,378 27-May-2003	Granted 10-Dec-2018
		Title: Method and Apparatus for a N-Nary Logic Circuit Using Capacitance Isolation			
31876-0224/0 United States of America	CON	09/586,638 05-Jun-2000		6,268,746 31-Jul-2001	Granted 27-Oct-2018
		Title: Method and Apparatus for Logic Synchronization			
31876-0230/1 United States of America	ORD	10/187,879 02-Jul-2002	US20030110404 12-Jun-2003	6,956,406 18-Oct-2005	Granted 11-Nov-2023
		Title: Static Storage Element for Dynamic Logic			
31876-0232/1 United States of America	ORD	09/844,686 27-Apr-2001	2002/0067187 06-Jun-2002	6,445,213 03-Sep-2002	Granted 27-Apr-2021
		Title: Method and Apparatus For Calculating Dynamic Logic Block Propagation Delay Targets Using Time Borrowing			
31876-0233/0 United States of America	CIP	09/901,411 09-Jul-2001	2001/0039635 08-Nov-2001	6,745,357 01-Jun-2004	Granted 20-Feb-2021
		Title: Dynamic Logic Scan Gate Method and Apparatus			
31876-0245/2 United States of America	ORD	10/164,040 06-Jun-2002	2002/0198911 26-Dec-2002	6,898,691 24-May-2005	Granted 27-Sep-2023
		Title: Rearranging Data Between Vector and Matrix Forms in a SIMD Matrix Processor			
31876-0262/1 United States of America	ORD	10/177,527 21-Jun-2002	2003/0046645 06-Mar-2003		Published
		Title: Monitor Manager that Creates and Executes State Machine-Based Monitor Instances in a Digital Simulation			
31876-0263/1 United States of America	ORD	09/966,049 28-Sep-2001	2002/0040285 04-Apr-2002	7,099,812 29-Aug-2006	Granted 08-May-2024
		Title: Grid that Tracks the Occurrence of a N-Dimensional Matrix of Combinatorial Events in a Simulation Using a Linear Index			

Client-Matter/Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
31876-0264/1	ORD	09/965,945	2003/0023396	6,728,654	Granted
United States of America		28-Sep-2001	30-Jan-2003	27-Apr-2004	03-Apr-2022
			Title: Random Number Indexing Method and Apparatus that Eliminates Software Call Sequence Dependency		
31876-0265/1	ORD	10/186,770	2003/0042935	6,714,045	Granted
United States of America		01-Jul-2002	06-Mar-2003	30-Mar-2004	01-Jul-2022
			Title: Static Transmission of FAST14 Logic 1 of N Signals		
31876-0267/0	ORD	10/177,448	2003/0122584		Published
United States of America		21-Jun-2002	03-Jul-2003		
			Title: Software Program that Transforms an N-Dimensional Matrix of Integers to a Linear Index		
31876-0274/1	ORD	10/738,281	US20040139423		Published
United States of America		16-Dec-2003	15-Jul-2004		
			Title: Expansion Syntax		
31876-0275/1	ORD	10/738,278	2005/0060128-A1		Published
United States of America		16-Dec-2003	17-Mar-2005		
			Title: Physical Realization of Dynamic Logic Using Parameterized Tile Partitioning		

EXHIBIT C

Trademarks

Description	Registration/Application Number	Registration/Application Date

Trademark	Client-Matter/Subcase Country Name	Status Class(es)	Application Number/Date	Registration Number/Date
ADAPTIVE SIGNAL PROCESSOR	31876-0269/ United States of America	Registered 009	78/114,358 12-Mar-2002	2,708,216 15-Apr-2003
Build14	31876-0283/ United States of America	Allowed 009, 041	78/465,981 11-Aug-2004	
FAST14	31876-0261/ United States of America	Registered 009	78/065,724 25-May-2001	2,738,968 15-Jul-2003
FASTCORE	31876-0288/0 United States of America	Pending 009	78/933,918 20-Jul-2006	
FASTMATH	31876-0268/ United States of America	Registered 009	78/114,059 11-Mar-2002	2,780,706 04-Nov-2003
FASTMATH-LP	31876-0278/ United States of America	Registered 009, 016	78/252,134 20-May-2003	2,906,315 30-Nov-2004
FASTWARE	31876-0289/0 United States of America	Pending 009	78/934,524 21-Jul-2006	
Finish14	31876-0284/ United States of America	Allowed 009, 041	78/466,651 12-Aug-2004	
IN	31876-0227/ United States of America	Registered 009	78/007,766 11-May-2000	2,801,275 30-Dec-2003
IN	31876-0228/ United States of America	Registered 009	78/032,605 26-Oct-2000	2,832,962 13-Apr-2004
INTRINSITY	31876-0220/ United States of America	Registered 009	75/895,354 13-Jan-2000	2,769,500 30-Sep-2003
INTRINSITY	31876-0225/ United States of America	Registered 009	78/007,731 11-May-2000	2,728,084 17-Jun-2003
INTRINSITY	31876-0226/ United States of America	Registered 009	78/007,760 11-May-2000	2,748,597 05-Aug-2003
ION RING	31876-0270/ United States of America	Registered 009	78/119,352 03-Apr-2002	2,765,942 16-Sep-2003
NDL	31876-0246/ United States of America	Registered 009	78/065,636 24-May-2001	2,799,110 23-Dec-2003

Trademark	Client-Matter/Subcase Country Name	Status Class(es)	Application Number/Date	Registration Number/Date
Plan14	31876-0285/ United States of America	Allowed 009, 041	78/466,678 12-Aug-2004	
Sim14	31876-0286/ United States of America	Allowed 009, 041	78/466,709 12-Aug-2004	

EXHIBIT D

Mask Works

Description	Registration/Application Number	Registration/Application Date
NONE		