TRADEMARK ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
T-RAM SEMICONDUCTOR INCORPORATED		08/01/2008	CORPORATION: CALIFORNIA

RECEIVING PARTY DATA

Name:	SILICON VALLEY BANK
Street Address:	3979 FREEDOM CIRCLE
Internal Address:	SUITE 600
City:	SANTA CLARA
State/Country:	CALIFORNIA
Postal Code:	95054
Entity Type:	CHARTERED BANK: CALIFORNIA

PROPERTY NUMBERS Total: 3

Property Type	Number	Word Mark
Serial Number:	77475213	T-RAM
Serial Number:	77472225	TCCT
Serial Number:	76395784	T-RAM

OP $90.00 77475213

CORRESPONDENCE DATA

Fax Number: (404)962-6736
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: (404) 885-3038
Email: michael.brignati@troutmansanders.com
Correspondent Name: MICHAEL J. BRIGNATI, PH.D.
Address Line 1: TROUTMAN SANDERS LLP
Address Line 2: 600 PEACHTREE STREET, N.E.
Address Line 4: ATLANTA, GEORGIA 30308-2216

ATTORNEY DOCKET NUMBER:	220763.000938

NAME OF SUBMITTER:	Michael J. Brignati, Ph.D.
Signature:	/Michael J. Brignati 60,890/
Date:	08/07/2008

Total Attachments: 12
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INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement is entered into as of August 1, 2008 by and between SILICON VALLEY BANK ("**Bank**") and T-RAM SEMICONDUCTOR INCORPORATED ("**Grantor**").

RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodation to Grantor (the "**Loans**") in the amounts and manner set forth in that certain Loan and Security Agreement by and between Bank and Grantor dated of even date herewith (as the same may be amended, modified or supplemented from time to time, the "**Loan Agreement**"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in certain Copyrights, Trademarks and Patents to secure the obligations of Grantor under the Loan Agreement.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

To secure its obligations under the Loan Agreement, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its Intellectual Property Collateral (including without limitation those Copyrights, Patents and Trademarks listed on Schedules A, B and C hereto), and including without limitation all proceeds thereof (such as, by way of example but not by way of limitation, license royalties and proceeds of infringement suits), the right to sue for past, present and future infringements, all rights corresponding thereto throughout the world and all re-issues, divisions continuations, renewals, extensions and continuations-in-part thereof.

This security interest is granted in conjunction with the security interest granted to Bank under the Loan Agreement. The rights and remedies of Bank with respect to the security interest granted hereby are in addition to those set forth in the Loan Agreement and the other Loan Documents, and those which are now or hereafter available to Bank as a matter of law or equity. Each right, power and remedy of Bank provided for herein or in the Loan Agreement or any of the Loan Documents, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right, power or remedy provided for herein and the

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exercise by Bank of any one or more of the rights, powers or remedies provided for in this Intellectual Property Security Agreement, the Loan Agreement or any of the other Loan Documents, or now or hereafter existing at law or in equity, shall not preclude the simultaneous or later exercise by any person, including Bank, of any or all other rights, powers or remedies.

[Signatures Appear on the Following Page]

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IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

Address of Grantor:

T-RAM SEMICONDUCTOR INCORPORATED

620 North McCarthy Boulevard
Milpitas, California 95035
Attn: Sam Nakib

By: _____
Name: SAM NAKIB
Title: President & CEO

BANK:

Address of Bank:

SILICON VALLEY BANK

3979 Freedom Circle, Suite 600
Santa Clara, California 95054
Attn: Samir Kaji

By: _____
Name:
Title:

TRADEMARK
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IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

Address of Grantor:

T-RAM SEMICONDUCTOR INCORPORATED

620 North McCarthy Boulevard
Milpitas, California 95035
Attn: Sam Nakib

By:_____
Name:
Title:

BANK:

Address of Bank:

SILICON VALLEY BANK

3979 Freedom Circle, Suite 600
Santa Clara, California 95054
Attn: Samir Kaji

By: [signature]
Name: Samir Kaji
Title: VP

TRADEMARK
REEL: 003831 FRAME: 0549

EXHIBIT A

Copyrights

Description	Registration/ Application Number	Registration/ Application Date
None		

EXHIBIT B

Patents

Title	Patent/Patent Application Number (Publication Number)	Issue/Filing Date
Workfunction-adjusted thyristor-based memory device	7,381,999	06/03/2008
State maintenance pulsing for a memory device	7,379,381	05/27/2008
Thyristor-based device with trench dielectric material	7,374,974	05/20/2008
Deep trench isolation for thyristor-based semiconductor device	7,351,614	04/01/2008
Semiconductor device incorporating thyristor-based memory and strained silicon	7,326,969	02/05/2008
Single data line sensing scheme for TCCT-based memory cells	7,324,394	01/29/2008
Thyristor-based device having dual control ports	7,320,895	01/22/2008
Bitline shielding for thyristor-based memory	7,319,622	01/15/2008
Semiconductor device with a MOSFET formed in close proximity to a bipolar device and method of manufacture	7,316,941	01/08/2008
Thyristor circuit and approach for temperature stability	7,304,327	12/04/2007
Method of manufacturing a thyristor semiconductor device	7,279,367	10/09/2007
Thyristor-based memory and its method of operation	7,268,373	09/11/2007
Silicide uniformity for lateral bipolar transistors	7,262,443	08/28/2007

TRADEMARK
REEL: 003831 FRAME: 0551

Thyristor semiconductor memory device and method of manufacture	7,256,430	08/14/2007
Data restore in thryistor based memory devices	7,245,525	07/17/2007
Read-modify-write memory using read-or-write banks	7,236,421	06/26/2007
Thyristor-based semiconductor device and method of fabrication	7,195,959	03/27/2007
Electrostatic discharge protection circuit	7,187,530	03/06/2007
Trench isolation for thyristor-based device	7,183,591	02/27/2007
Thyristor-based semiconductor memory device and its method of manufacture	7,157,342	01/02/2007
Fin thyristor-based semiconductor device	7,135,745	11/14/2006
Self-aligned thin capacitively-coupled thyristor structure	7,125,753	10/24/2006
Reference cells for TCCT based memory cells	7,123,508	10/17/2006
High ion/ioff soi MOSFET using body voltage control	7,109,532	09/19/2006
Digital signal sampler	7,096,144	08/22/2006
Architecture and method for output clock generation on a high speed memory device	7,089,439	08/08/2006
Thyristor-based memory and its method of operation	7,078,739	07/18/2006
Thyristor device with carbon lifetime adjustment implant and its method of fabrication	7,075,122	07/11/2006
Reference cells for TCCT based memory cells	7,064,977	06/20/2006

TRADEMARK
REEL: 003831 FRAME: 0552

Method and system for writing data to memory cells	7,054,191	05/30/2006
Thyristor having a first emitter with relatively lightly doped portion to the base	7,053,423	05/30/2006
Shunt connection to the emitter of a thyristor	7,049,182	05/23/2006
Dynamic data restore in thyristor-based memory device	7,042,759	05/09/2006
Gated-thyristor approach having angle-implanted base region	7,037,763	05/02/2006
Buried emitter contact for thyristor-based semiconductor device	7,030,425	04/18/2006
Varied trench depth for thyristor isolation	7,015,077	03/21/2006
Single data line sensing scheme for TCCT-based memory cells	7,006,398	02/28/2006
Trench isolation for thyristor-based device	6,998,652	02/14/2006
Thyristor semiconductor memory device and method of manufacture	6,998,298	02/14/2006
Thyristor-based device having a reduced-resistance contact to a buried emitter region	6,980,457	12/27/2005
Method for making a recessed thyristor control port	6,979,602	12/27/2005
Geometric D/A converter for a delay-locked loop	6,975,260	12/13/2005
Thyristor-based device having dual control ports	6,965,129	11/15/2005
Bit line control and sense amplification for TCCT-based memory cells	6,958,931	10/25/2005
Deep trench isolation for thyristor-based semiconductor device	6,953,953	10/11/2005

Apparatus and method for producing an output clock pulse and output clock generator using same	6,947,349	09/20/2005
Data restore in thryistor based memory devices	6,944,051	09/13/2005
Reference cells for TCCT based memory cells	6,940,772	09/06/2005
Sense amplifier based voltage comparator	6,937,085	08/30/2005
Method of manufacturing a thyristor device with a control port in a trench	6,913,955	04/05/2005
Self-aligned thin capacitively-coupled thyristor structure	6,911,680	06/28/2005
Single data line sensing scheme for TCCT-based memory cells	6,903,987	06/07/2005
Reference cells for TCCT based memory cells	6,901,021	05/31/2005
Delay line and output clock generator using same	6,891,774	05/10/2005
Stability in thyristor-based memory device	6,891,205	05/10/2005
Increased base-emitter capacitance	6,888,177	05/03/2005
Thyrister semiconductor device	6,888,176	05/03/2005
Dynamic data restore in thyristor-based memory device	6,885,581	04/26/2005
Carrier coupler for thyristor-based semiconductor device	6,872,602	03/29/2005
Reference cells for TCCT based memory cells	6,845,037	01/18/2005
Thyristor-based device with trench dielectric material	6,835,997	12/28/2004

Semiconductor region self-aligned with ion implant shadowing	6,828,202	12/07/2004
Thyristor having a first emitter with relatively lightly doped portion to the base	6,828,176	12/07/2004
Geometric D/A converter for a delay-locked loop	6,819,278	11/16/2004
Method for trench isolation for thyristor-based device	6,818,482	11/16/2004
Varied trench depth for thyristor isolation	6,815,734	11/09/2004
Read-modify-write memory using read-or-write banks	6,804,162	10/12/2004
Method for making an inlayed thyristor-based device	6,790,713	09/14/2004
Memory cell error recovery	6,785,169	08/31/2004
Reference cells for TCCT based memory cells	6,781,888	08/24/2004
Memory architecture for TCCT-based memory cells	6,778,435	08/17/2004
Thyristor-based device including trench isolation	6,777,271	08/17/2004
Method of forming self-aligned thin capacitively-coupled thyristor structure	6,767,770	07/27/2004
Charge pump based voltage regulator with smart power regulation	6,756,838	06/29/2004
Carrier coupler for thyristor-based semiconductor device	6,756,612	06/29/2004
Circuit and method for implementing a write operation with TCCT-based memory cells	6,735,113	05/11/2004
Geometric D/A converter for a delay-locked loop	6,734,815	05/11/2004

Thyristor-based device including trench dielectric isolation for thyristor-body regions	6,727,528	04/27/2004
Bit line control and sense amplification for TCCT-based memory cells	6,721,220	04/13/2004
Thyristor with lightly-doped emitter	6,703,646	03/09/2004
Thyristor-based device that inhibits undesirable conductive channel formation	6,690,039	02/10/2004
Thyristor-based device over substrate surface	6,690,038	02/10/2004
Thyristor-based device adapted to inhibit parasitic current	6,686,612	02/03/2004
Recessed thyristor control port	6,683,330	01/27/2004
Shunt connection to emitter	6,666,481	12/23/2003
Stability in thyristor-based memory device	6,653,175	11/25/2003
Thyristor-based device over substrate surface	6,653,174	11/25/2003
Reference cells for TCCT based memory cells	6,611,452	08/26/2003
Thyristor-based device having extended capacitive coupling	6,583,452	06/24/2003
Stability in thyristor-based memory device	6,462,359	10/08/2002
Dynamic data restore in thyristor-based memory device	11/361,334	02/24/2006
Semiconductor device with leakage implant and method of fabrication	11/159,514	06/22/2005

EXHIBIT C

Trademarks

Description	Registration/ Application Number	Registration/ Application Date
T-RAM (Pending)	77475213	May 15, 2008
TCCT (Pending)	77472225	May 12, 2008
T-RAM (Pending)	76395784	April 5, 2002
ZT (Abandoned)	76502193	March 28, 2003