TRADEMARK ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	Security Agreement

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
Catalyst Semiconductor, Inc.		10/10/2008	CORPORATION: DELAWARE

RECEIVING PARTY DATA

Name:	JPMorgan Chase Bank, N.A.
Street Address:	270 Park Avenue
City:	New York
State/Country:	NEW YORK
Postal Code:	10017
Entity Type:	Bank:

PROPERTY NUMBERS Total: 3

Property Type	Number	Word Mark
Serial Number:	78802766	CATALYST
Registration Number:	3192919	
Registration Number:	3447884	QUAD-MODE

OP $90.00 78802766

CORRESPONDENCE DATA

Fax Number: (866)826-5420
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: 3016380511
Email: ipresearchplus@comcast.net
Correspondent Name: IP Research Plus, Inc.
Address Line 1: 21 Tadcaster Circle
Address Line 2: Attn: Penelope J.A. Agodoa
Address Line 4: Waldorf, MARYLAND 20602

ATTORNEY DOCKET NUMBER:	33825
NAME OF SUBMITTER:	Penelope J.A. Agodoa

Signature:	/pja/
Date:	10/20/2008

Total Attachments: 11
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Form **PTO-1594** (Rev. 07/05)
OMB Collection 0651-0027 (exp. 6/30/2008)

U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

RECORDATION FORM COVER SHEET
TRADEMARKS ONLY

To the Director of the U. S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies):
Catalyst Semiconductor, Inc.

☐ Individual(s) ☐ Association
☐ General Partnership ☐ Limited Partnership
☑ Corporation- State: Delaware
☐ Other

Citizenship (see guidelines)

Additional names of conveying parties attached? ☐ Yes ☑ No

2. Name and address of receiving party(ies)
Additional names, addresses, or citizenship attached? ☐ Yes ☑ No

Name: JPMorgan Chase Bank, N.A.
Internal Address:
Street Address: 270 Park Avenue
City: New York
State: New York
Country: USA Zip: 10017

☐ Association Citizenship
☐ General Partnership Citizenship
☐ Limited Partnership Citizenship
☐ Corporation Citizenship
☑ Other Bank Citizenship

If assignee is not domiciled in the United States, a domestic representative designation is attached: ☐ Yes ☐ No
(Designations must be a separate document from assignment)

3. Nature of conveyance)/Execution Date(s) :
Execution Date(s) October 10, 2008

☐ Assignment ☐ Merger
☑ Security Agreement ☐ Change of Name
☐ Other

4. Application number(s) or registration number(s) and identification or description of the Trademark.

A. Trademark Application No.(s)
Please see attached Schedule A to the Patent and Trademark Security Agreement

B. Trademark Registration No.(s)
Please see attached Schedule A

Additional sheet(s) attached? ☑ Yes ☐ No

C. Identification or Description of Trademark(s) (and Filing Date if Application or Registration Number is unknown):

5. Name & address of party to whom correspondence concerning document should be mailed:
Name: IP Research Plus
Internal Address:
Attn: Penelope J.A. Agodoa
Street Address:
21 Tadcaster Circle
City: Waldorf
State: MD Zip: 20602
Phone Number: 301-638-0511
Fax Number: 866-826-5420
Email Address: orders@ipresearchplus.com

6. Total number of applications and registrations involved: 3

7. Total fee (37 CFR 2.6(b)(6) & 3.41) $

☐ Authorized to be charged by credit card
☐ Authorized to be charged to deposit account
☐ Enclosed

8. Payment Information:
a. Credit Card Last 4 Numbers
Expiration Date
b. Deposit Account Number
Authorized User Name

9. Signature:

Signature — October 16, 2008 (Date)

Lauren Sottile (Name of Person Signing)

Total number of pages including cover sheet, attachments, and document: 11

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O. Box 1450, Alexandria, VA 22313-1450

PATENT AND TRADEMARK SECURITY AGREEMENT, dated as of October 10, 2008 (this "Agreement"), among CATALYST SEMICONDUCTOR, INC. (the "Grantor") and JPMORGAN CHASE BANK, N.A., as Collateral Agent (the "Collateral Agent").

Reference is made to the Security Agreement dated as of August 4, 1999, as amended and restated as of March 3, 2003 (as amended, supplemented or otherwise modified from time to time, the "Security Agreement"), among Semiconductor Components Industries, LLC., (the "Borrower"), ON Semiconductor Corporation ("Holdings"), the subsidiaries of Holdings party thereto and the Collateral Agent. The Lenders have agreed to extend credit to the Borrower subject to the terms and conditions set forth in the Amended and Restated Credit Agreement dated as of August 4, 1999, as amended and restated as of March 6, 2007 (as amended, supplemented or otherwise modified from time to time (the "Amended and Restated Credit Agreement")). The obligations of the Lenders to continue to extend such credit are conditioned upon, among other things, the execution and delivery of this Agreement. Accordingly, the parties hereto agree as follows:

SECTION 1. Terms. Capitalized terms used in this Agreement and not otherwise defined herein have the meanings specified in the Security Agreement. The rules of construction specified in Section 1.03 of the Security Agreement also apply to this Agreement.

SECTION 2. Grant of Security Interest. As security for the payment or performance, as the case may be, in full of the Obligations, the Grantor, pursuant to the Security Agreement, did and hereby does grant to the Collateral Agent, its successors and assigns, for the benefit of the Secured Parties, a security interest in, all right, title or interest in or to any and all of the following assets and properties now owned or at any time hereafter acquired by the Grantor or in which the Grantor now has or at any time in the future may acquire any right, title or interest (collectively, the "Patent and Trademark Collateral"):

(a) all letters patent of the United States or the equivalent thereof in any other country, all registrations and recordings thereof, and all applications for letters patent of the United States or the equivalent thereof in any other country, including registrations, recordings and pending applications in the United States Patent and Trademark Office or any similar offices in any other country, including those listed on Schedule A (the "Patents") and all reissues, continuations, divisions, continuations-in-part, renewals or extensions thereof, and the inventions disclosed or claimed therein, including the right to make, use and/or sell the inventions disclosed or claimed therein;

(b) all trademarks, service marks, trade names, corporate names, company names, business names, fictitious business names, trade styles, trade dress, logos, other source or business identifiers, designs and general intangibles of like nature, now existing or hereafter adopted or acquired, all registrations and recordings

thereof, and all registration and recording applications filed in connection therewith, including registrations and registration applications in the United States Patent and Trademark Office, any State of the United States or any similar offices in any other country or any political subdivision thereof, and all extensions or renewals thereof, including, without limitation, those listed on Schedule A hereto (the "Trademarks");

(c) all goodwill associated with or symbolized by the Patents and Trademarks; and

(d) all other assets, rights and interests that uniquely reflect or embody the Patents and Trademarks.

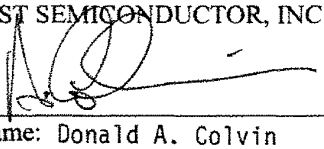
SECTION 3. Termination. This Agreement is made to secure the satisfactory performance and payment of the Obligations. Upon termination of the Security Agreement or release of a Grantor's obligations thereunder, this Agreement shall automatically terminate as to such Grantor.

SECTION 4. Security Agreement. The security interests granted to the Collateral Agent herein are granted in furtherance, and not in limitation of, the security interests granted to the Collateral Agent pursuant to the Security Agreement. The Grantor hereby acknowledges and affirms that the rights and remedies of the Collateral Agent with respect to the Patent and Trademark Collateral are more fully set forth in the Security Agreement, the terms and provisions of which are hereby incorporated herein by reference as if fully set forth herein. In the event of any conflict between the terms of this Agreement and the Security Agreement, the terms of the Security Agreement shall govern.

SECTION 5. Counterparts. This Agreement may be executed in any number of counterparts, each of which shall constitute an original but all of which, when taken together, shall constitute one agreement. Delivery of an executed counterpart of a signature page of this Agreement by facsimile or other customary means of electronic transmission shall be effective as delivery of a manually executed counterpart hereof.

IN WITNESS WHEREOF, the parties hereto have duly executed this Agreement as of the day and year first above written.

CATALYST SEMICONDUCTOR, INC.,

by 

Name: Donald A. Colvin
Title: Chief Financial Officer

JPMORGAN CHASE BANK, N.A., as Collateral Agent,

by

Name:
Title:

IN WITNESS WHEREOF, the parties hereto have duly executed this Agreement as of the day and year first above written.

CATALYST SEMICONDUCTOR, INC.,

by

_____

Name:
Title:

JPMORGAN CHASE BANK, N.A., as Collateral Agent,

by

_____

Name: Ann B. Kerns
Title: Vice President

Schedule A

Debtor Name (Registered Owner of I.P.)	Type of Intellectual Property (Patent, Trademark)	Title of Intellectual Property	Patent No./ Pub. App. No./ Serial No.	Issuance Date/ Date Filed
Catalyst Semiconductor, Inc.	Patent	Digital potentiometer including plural bulk impedance devices	Pat. No. 7,345,611	Issue Date 3/18/08 Filed 9/10/03
Catalyst Semiconductor, Inc.	Patent	Method for trimming the temperature coefficient of a floating gate voltage reference	Pat. No. 7,324,380	Issue Date 1/29/08 Filed 12/15/06
Catalyst Semiconductor, Inc.	Patent	LED driver with integrated bias and dimming control storage	Pat. No. 7,324,130	Issue Date 1/29/08 Filed 12/2/04
Catalyst Semiconductor, Inc.	Patent	LED current bias control using a step down regulator	Pat. No. 7,323,828	Issue Date 1/29/08 Filed 4/25/05
Catalyst Semiconductor, Inc.	Patent	Non-volatile memory integrated circuit	Pat. No. 7,323,742	Issue Date 1/29/08 Filed 10/27/05
Catalyst Semiconductor, Inc.	Patent	Precision non-volatile CMOS reference circuit	Pat. No. 7,245,536	Issue Date 7/17/07 Filed 2/15/06
Catalyst Semiconductor, Inc.	Patent	LED bias current control using adaptive fractional charge pump	Pat. No. 7,236,046	Issue Date 6/26/07 Filed 11/1/05
Catalyst Semiconductor, Inc.	Patent	Non-volatile CMOS reference circuit	Pat. No. 7,149,123	Issue Date 12/12/06 Filed 4/5/05
Catalyst Semiconductor, Inc.	Patent	Digital potentiometer with resistor binary weighting decoding	Pat. No. 7,042,380	Issue Date 05/9/06 Filed 6/2/04
Catalyst Semiconductor, Inc.	Patent	Digital potentiometer including at least one bulk impedance device	Pat. No. 7,012,555	Issue Date 3/14/06 Filed 9/10/03
Catalyst Semiconductor, Inc.	Patent	Digital potentiometer including output	Pat. No. 7,005,837	Issue Date 2/28/06

Debtor Name (Registered Owner of I.P.)	Type of Intellectual Property (Patent, Trademark)	Title of Intellectual Property	Patent No./ Pub. App. No./ Serial No.	Issuance Date/ Date Filed
		buffer		Filed 11/26/03
Catalyst Semiconductor, Inc.	Patent	Non-volatile memory integrated circuit	Pat. No. 6,989,562	Issue Date 1/24/06 Filed 6/20/03
Catalyst Semiconductor, Inc.	Patent	Programmable analog bias circuits using floating gate CMOS technology	Pat. No. 6,970,037	Issue Date 11/29/05 Filed 9/5/03
Catalyst Semiconductor, Inc.	Patent	System and method for programming non-volatile memory	Pat. No. 6,865,113	Issue Date 3/8/05 Filed 7/23/03
Catalyst Semiconductor, Inc.	Patent	Buffered configurable nonvolatile programmable digital potentiometer	Pat. No. 6,771,053	Issue Date 8/3/04 Filed 2/20/02
Catalyst Semiconductor, Inc.	Patent	Low dropout voltage regulator with non-miller frequency compensation	Pat. No. 6,710,583	Issue Date 3/23/04 Filed 1/10/03
Catalyst Semiconductor, Inc.	Patent	Low dropout voltage regulator with non-miller frequency compensation	Pat. No. 6,518,737	Issue Date 2/11/03 Filed 9/28/01
Catalyst Semiconductor, Inc.	Patent	Method for supervising software execution in a license restricted environment	Pat. No. 5,796,941	Issue Date 8/18/98 Filed 9/6/96
Catalyst Semiconductor, Inc.	Patent	Single transistor non-volatile electrically alterable semiconductor memory device	Pat. No. 5,793,079	Issue Date 8/11/98 Filed 7/22/96
Catalyst Semiconductor, Inc.	Patent	Structure and method for improved memory arrays and improved electrical contacts in semiconductor devices	Pat. No. 5,783,471	Issue Date 7/21/98 Filed 11/9/94
Catalyst Semiconductor, Inc.	Patent	Intermediate size non-volatile electrically alterable semiconductor memory device	Pat. No. 5,764,586	Issue Date 6/9/98 Filed 10/10/96
Catalyst Semiconductor, Inc.	Patent	Negative voltage decoding in non-	Pat. No. 5,548,551	Issue Date 8/20/96

Debtor Name (Registered Owner of I.P.)	Type of Intellectual Property (Patent, Trademark)	Title of Intellectual Property	Patent No./ Pub. App. No./ Serial No.	Issuance Date/ Date Filed
		volatile memories		Filed 3/24/95
Catalyst Semiconductor, Inc.	Patent	Charge stacking on-chip high-voltage generator and method	Pat. No. 5,543,668	Issue Date 8/9/96 Filed 9/16/94
Catalyst Semiconductor, Inc.	Patent	Structure and method for improved memory arrays and improved electrical contacts in semiconductor devices	Pat. No. 5,519,239	Issue Date 5/21/96 Filed 11/10/94
Catalyst Semiconductor, Inc.	Patent	Self-recovering erase scheme to enhance flash memory endurance	Pat. No. 5,400,286	Issue Date 3/21/95 Filed 8/17/93
Catalyst Semiconductor, Inc.	Patent	Memory circuit with pumped voltage for erase and program operations	Pat. No. 5,313,429	Issue Date 5/17/94 Filed 2/14/92
Catalyst Semiconductor, Inc.	Patent	Power stealing circuit	Pat. No. 5,218,235	Issue Date 6/8/93 Filed 1/4/91
Catalyst Semiconductor, Inc.	Patent	Charge pump with high output current	Pat. No. 5,216,588	Issue Date 6/1/93 Filed 2/14/92
Catalyst Semiconductor, Inc.	Patent	Memory array architecture for flash memory	Pat. No. 5,185,718	Issue Date 2/9/93 Filed 2/19/91
Catalyst Semiconductor, Inc.	Patent	High density EEPROM cell and process for making the cell	Pat. No. 5,033,023	Issue Date 7/16/91 Filed 4/8/88
Catalyst Semiconductor, Inc.	Patent	EEPROM utilizing single transistor per cell capable of both byte erase and flash erase	Pat. No. 4,949,309	Issue Date 8/14/90 Filed 5/11/88
Catalyst Semiconductor, Inc.	Patent	Differential sense amplifier circuit for high speed ROMS, and flash memory devices	Pat. No. 4,903,237	Issue Date 2/20/90 Filed 8/2/88
Catalyst Semiconductor, Inc.	Patent	Nonvolatile memory cell for eeprom	Pat. No. 4,894,802	Issue Date 2/16/90

Debtor Name (Registered Owner of I.P.)	Type of Intellectual Property (Patent, Trademark)	Title of Intellectual Property	Patent No./ Pub. App. No./ Serial No.	Issuance Date/ Date Filed
		including a floating gate to drain tunnel area positioned away from the channel region to prevent trapping of electrons in the gate oxide during cell erase		Filed 2/2/88
Catalyst Semiconductor, Inc.	Patent	Process for making a high density split gate nonvolatile memory cell	Pat. No. 4,861,730	Issue Date 8/29/89 Filed 1/25/88
Catalyst Semiconductor, Inc.	Patent	CMOS rectifier circuit	Pat. No. 4,811,191	Issue Date 7/3/89 Filed 3/28/88
Catalyst Semiconductor, Inc.	Patent	Redundancy circuit for high speed EPROM and flash memory devices	Pat. No. 5200922	Issue Date 4/6/93 Filed 10/24/90
Catalyst Semiconductor, Inc.	Patent	Scalable Electrically Eraseable And Programmable Memory	Pat. Pub. No. 20080165582	Filed 3/18/08
Catalyst Semiconductor, Inc.	Patent	Non-Volatile Memory Cell In Standard CMOS Process	Pat. Pub. No. 20080055965	Filed 9/1/06
Catalyst Semiconductor, Inc.	Patent	Digital Potentiometer Including Plural Bulk Impedance Devices	Pat. Pub. No. 20080048900	Filed 10/30/07
Catalyst Semiconductor, Inc.	Patent	Scalable Electrically Eraseable And Programmable Memory (EEPROM) Cell Array	Pat. Pub. No. 20070228451	Filed 3/30/06
Catalyst Semiconductor, Inc.	Patent	Programmable Fractional Charge Pump For DC-DC Converter	Pat. Pub. No. 20070222501	Filed 5/9/07
Catalyst Semiconductor, Inc.	Patent	Fractional Charge Pump For Step-Down DC-DC Converter	Pat. Pub. No. 20070194363	Filed 2/22/07
Catalyst Semiconductor, Inc.	Patent	Precision Non-Volatile CMOS Reference Circuit	Pat. Pub. No. 20070189069	Filed 12/15/06

Debtor Name (Registered Owner of I.P.)	Type of Intellectual Property (Patent, Trademark)	Title of Intellectual Property	Patent No./ Pub. App. No./ Serial No.	Issuance Date/ Date Filed
Catalyst Semiconductor, Inc.	Patent	LED bias current control using adaptive fractional charge pump	Pat. Pub. No. 20070096795	Filed 11/1/05
Catalyst Semiconductor, Inc.	Patent	LED current bias control using a step down regulator	Pat. Pub. No. 20060238174	Filed 4/25/05
Catalyst Semiconductor, Inc.	Patent	Non-volatile memory integrated circuit	Pat. Pub. No. 20060049451	Filed 10/27/05
Catalyst Semiconductor, Inc.	Patent	Non-volatile memory integrated circuit	Pat. Pub. No. 20060049450	Filed 10/27/05
Catalyst Semiconductor, Inc.	Patent	Digital potentiometer with resistor binary weighting decoding	Pat. Pub. No. 20050270043	Filed 6/2/04
Catalyst Semiconductor, Inc.	Patent	Non-volatile CMOS reference circuit	Pat. Pub. No. 20050219916	Filed 4/5/05
Catalyst Semiconductor, Inc.	Patent	LED driver with integrated bias and dimming control storage	Pat. Pub. No. 20050112801	Filed 12/2/04
Catalyst Semiconductor, Inc.	Patent	Digital potentiometer including at least one bulk impedance device	Pat. Pub. No. 20050052306	Filed 9/10/03
Catalyst Semiconductor, Inc.	Patent	Digital potentiometer including plural bulk impedance devices	Pat. Pub. No. 20050052305	Filed 9/10/03
Catalyst Semiconductor, Inc.	Patent	Programmable analog bias circuits using floating gate cmos technology	Pat. Pub. No. 20050052223	Filed 9/5/03
Catalyst Semiconductor, Inc.	Patent	SYSTEM AND METHOD FOR PROGRAMMING NON-VOLATILE MEMORY	Pat. Pub. No. 20050018487	Filed 7/23/03
Catalyst Semiconductor, Inc.	Patent	Led driver with integrated bias and dimming control storage	Pat. Pub. No. 20040256625	Filed 6/17/03

Debtor Name (Registered Owner of I.P.)	Type of Intellectual Property (Patent, Trademark)	Title of Intellectual Property	Patent No./ Pub. App. No./ Serial No.	Issuance Date/ Date Filed
Catalyst Semiconductor, Inc.	Patent	Non-volatile memory integrated circuit	Pat. Pub. No. 20040197993	Filed 6/20/03
Catalyst Semiconductor, Inc.	Patent	Scalable electrically eraseable and programmable memory	Pat. Pub. No. 20080054336	Filed 9/5/06
Catalyst Semiconductor, Inc.	Patent	Method for reducing charge loss in analog floating gate cell	Pat. Pub. No. 20080130362	Filed 11/20/07
Catalyst Semiconductor, Inc.	Trademark	CATALYST	Serial No. 78802766	Filed 1/30/06
Catalyst Semiconductor, Inc.	Trademark		Serial No. 78802771 Reg. No. 3192919	Filed 1/30/06 Reg. Date 1/2/07
Catalyst Semiconductor, Inc.	Trademark	QUAD-MODE	Serial No. 77166361 Reg. No. 3447884	Filed 4/26/07 Reg. Date 6/17/08