TRADEMARK ASSIGNMENT

Electronic Version v1.1 Stylesheet Version v1.1

SUBMISSION TYPE: NEW ASSIGNMENT

NATURE OF CONVEYANCE: SECURITY INTEREST

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
Luxtera, Inc.		06/15/2009	CORPORATION: DELAWARE

RECEIVING PARTY DATA

Name:	Silicon Valley Bank
Street Address:	3003 Tasman Drive
City:	Santa Clara
State/Country:	CALIFORNIA
Postal Code:	95054
Entity Type:	CORPORATION: CALIFORNIA

PROPERTY NUMBERS Total: 5

Property Type	Number	Word Mark
Serial Number:	78583030	
Serial Number:	78583028	LUXTERA
Serial Number:	78582939	LUXTERA
Serial Number:	77378412	VIDEOLYNX
Serial Number:	77516061	ОРТОРНУ

CORRESPONDENCE DATA

Fax Number: (858)638-5033

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

Phone: 8586386733

Email: karen.johanson@dlapiper.com

Correspondent Name: DLA Piper LLP (US)

Address Line 1: 4365 Executive Drive, Suite 1100

Address Line 2: Attn: Karen Johanson

Address Line 4: San Diego, CALIFORNIA 92121

ATTORNEY DOCKET NUMBER: 354271-100

TRADEMARK

REEL: 004006 FRAME: 0619

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NAME OF SUBMITTER:	Troy Zander	
Signature:	/Troy Zander/	
Date:	06/17/2009	
Total Attachments: 7 source=Luxtera IPSA#page1.tif		
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INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement is entered into as of June 15, 2009 by and between SILICON VALLEY BANK ("Bank") and LUXTERA, INC., a Delaware corporation ("Grantor").

RECITALS

- A. Bank has agreed to make certain advances of money and to extend certain financial accommodation to Grantor (the "Loans") in the amounts and manner set forth in that certain Loan and Security Agreement by and between Bank and Grantor dated the Effective Date (as the same may be amended, modified or supplemented from time to time, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in certain Copyrights, Trademarks, Patents, and Mask Works to secure the obligations of Grantor under the Loan Agreement.
- B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

To secure its obligations under the Loan Agreement, until the occurrence of a IP Collateral Release Event (as defined in the Loan Agreement), Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its intellectual property (including without limitation those Copyrights, Patents and Trademarks listed on Schedules A, B and C hereto), and including without limitation all proceeds thereof (such as, by way of example but not by way of limitation, license royalties and proceeds of infringement suits), the right to sue for past, present and future infringements, all rights corresponding thereto throughout the world and all re-issues, divisions continuations, renewals, extensions and continuations-in-part thereof.

This security interest is granted in conjunction with the security interest granted to Bank under the Loan Agreement. The rights and remedies of Bank with respect to the security interest granted hereby are in addition to those set forth in the Loan Agreement and the other Loan Documents, and those which are now or hereafter available to Bank as a matter of law or equity. Each right, power and remedy of Bank provided for herein or in the Loan Agreement or any of the Loan Documents, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right, power or remedy provided for herein and the exercise by Bank of any one or more of the rights, powers or remedies provided for in this Intellectual Property Security Agreement, the Loan Agreement or any of the other Loan Documents, or now or hereafter existing at law or in equity, shall not preclude the simultaneous or later exercise by any person, including Bank, of any or all other rights, powers or remedies.

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IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

	GRANTOR:
Address of Grantor:	LUXTERA, INC.
2320 Camino Vida Roble Carlsbad, CA 92011 Attn:	By:
	BANK:
Address of Bank:	SILICON VALLEY BANK
3003 Tasman Drive	By: LLICIAMIN
Santa Clara, CA 95054-1191	Title: Relation chro Menzan
Attn:	

EXHIBIT A

Copyrights

Description

Registration Number

Registration Date

None.

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EXHIBIT B

Patents

	Description	Patent/App. No.	File Date
1.	Polysilicon and silicon dioxide light scatterers for silicon waveguides on five layer substrates	6993236	1/31/06
2.	Active waveguides for optoelectronic devices	6999670	2/14/06
3.	Polarization splitting grating couplers	7006732	2/28/06
4.	Polysilicon light scatterers for silicon waveguides	7046894	5/16/06
5.	Active waveguides for optoelectronic devices	7046896	5/16/06
6.	Polysilicon light scatterers for silicon waveguides on five layer substrates	7058273	6/6/06
7.	Light scattering structures formed in lower layers of strip loaded waveguides	7079742	7/18/06
8.	Light scattering structures formed in upper layer of strip loaded waveguides	7082245	7/25/06
9.	CMOS process waveguide coupler	7082247	7/25/06
10.	Polysilicon and silicon dioxide light scatterers for silicon waveguides	7095936	8/22/06
11.	CMOS process polysilicon strip loaded waveguides with a two layer core	7136563	11/14/06
12.	Electronically controllable arrayed waveguide gratings	7139455	11/21/06
13.	Fiber to chip coupler	7162124	1/9/07
14.	Optical waveguide grating coupler incorporating reflective optical elements and anti-reflection elements	7184627	2/27/07
15.	Optical waveguide grating coupler	7245803	7/17/07
16.	Light scattering structures formed in silicon waveguides	7251403	7/31/07
17.	Doping profiles in PN diode optical modulators	7251408	7/31/07
18.	Integrated photonic-electronic circuits and systems	7259031	8/21/07
19.	Optical waveguide grating coupler with varying scatter cross sections	7260293	8/21/07
20.	Germanium integrated CMOS wafer and method for manufacturing the same	7262117	8/28/07
21.	Wafer-level testing of optical and optoelectronic chips	7262852	8/28/07

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	Description	Patent/App.	F4 5 .
22.	Description Photonic input/output port	<u>No.</u> 7269326	<u>File Date</u> 9/11/07
23.	Optoelectronic alignment structures for the wafer level testing of optical and optoelectronic chips	7298939	11/20/07
24.	Optical alignment loops for the wafer-level testing of optical and optoelectronic chips	7378861	5/27/08
25.	Littrow gratings as alignment structures for the wafer level testing of optical and optoelectronic chips	7024066	4/4/06
26.	External cavity laser source	10777702	2/11/04
27.	Flip-chip devices formed on photonic integrated circuit chips	11195357	8/2/05
28.	Design of CMOS integrated germanium photodiodes	11735251	4/13/07
29.	Photonic input/output port	6788847	9/7/04
30.	Methods of incorporating germanium within CMOS process	6887773	5/3/05
31.	CMOS process silicon waveguides	7010208	3/7/06
32.	Integrated dual waveguides	7027673	4/11/06
33.	Photonic input/output port	7031562	4/18/06
34.	Distributed amplifier optical modulators	7039258	5/2/06
35.	Active waveguides for optoelectronic devices	7046895	5/16/06
36.	Light scattering structures formed in upper layers of strip loaded waveguides	7054533	5/30/06
37.	Polarization splitting grating couplers	7068887	6/27/06
38.	CMOS process active waveguides	7072556	7/4/06
39.	Light scattering structures formed in lower layer of strip loaded waveguides	7082246	7/25/06
40.	Doping profiles in PN dode optical modulators	7085443	8/1/06
41.	Silicon on insulator resonator sensors and modulators and method of operating the same	7095010	8/22/06
42.	PN diode optical modulators fabricated in rib waveguides	7116853	10/3/06
43.	CMOS process polysilicon strip loaded waveguides with a three layer core	7116881	10/3/06
44.	PN diode optical modulators fabricated in strip loaded waveguides	7136544	11/14/06
45.	Optical probes with spacing sensors for the wafer level testing of	7183759	2/27/07

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	<u>Description</u> optical and optoelectronic chips	Patent/App. <u>No.</u>	File Date
46.	Optical waveguide grating coupler incorporating reflective optical elements and anti-reflection elements	7184625	2/27/07
47.	Wafer-level testing of optical and optoelectronic chips	7184626	2/27/07
48.	Use of waveguide grating couplers in an optical mux/demux system	7194166	3/20/07
49.	CMOS process active waveguides on five layer substrates	7218826	5/15/07
50.	Optical alignment loops for the wafer-level testing of optical and optoelectronic chips	7224174	5/29/07
51.	Integrated photonic-electronic circuits and systems	7251386	7/31/07
52.	Optical waveguide grating coupler with varying scatter cross sections	7260289	8/21/07
53.	Method of generating a geometrical rule for germanium integration within CMOS	7340709	3/4/08
54.	Systems and methods for testing germanium devices	7358527	4/15/08
55.	PLC for connecting optical fibers to optical or optoelectronic devices	7366380	4/29/08
56.	Optoelectronic alignment structures for the wafer level testing of optical and optoelectronic chips	7412138	8/12/08
57.	Waveguide photodetector with integrated electronics	7453132	11/18/08
58.	Distributed amplifier optical modulator	7515775	4/7/09

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EXHIBIT C

Trademarks

<u>Description</u>	Serial/Registration No.	File Date
DESIGN ONLY	78583030	3/8/05
LUXTERA	78583028	3/8/05
LUXTERA	78582939	3/8/05
VideoLynx	77378412	1/23/08
OptoPHY	77516061	7/7/08

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RECORDED: 06/17/2009