TRADEMARK ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
Vitesse Semiconductor Corporation		10/29/2007	CORPORATION: DELAWARE

RECEIVING PARTY DATA

Name:	Whitebox VSC, LTD.
Street Address:	3033 Excelsior Boulevard
Internal Address:	Suite 300
City:	Minneapolis
State/Country:	MINNESOTA
Postal Code:	55416
Entity Type:	LIMITED PARTNERSHIP: BRITISH VIRGIN ISLANDS

PROPERTY NUMBERS Total: 30

Property Type	Number	Word Mark
Registration Number:	3004768	ACTIPHY
Registration Number:	2543805	CROSSSTREAM
Registration Number:	2616224	FIBERSTREAM
Registration Number:	2526300	FIBRETIMER
Registration Number:	3007582	FOCUS CONNECT
Registration Number:	2744204	IQ10G
Registration Number:	2661839	IQ2000
Registration Number:	2692482	IQ2200
Registration Number:	2695613	MAGNIPHY
Registration Number:	2706045	MONITOR 4.8
Registration Number:	2694410	MULTILINK
Registration Number:	2697316	
Registration Number:	2607738	NETWORK ON A CHIP

CH $765.00 3004768

Registration Number:	2697054	PACEMAKER
Registration Number:	2890481	PACKET EXCHANGE MATRIX
Serial Number:	78638645	PIXEQ
Registration Number:	2695611	SIMPLIPHY
Registration Number:	2761196	SIMPLIPIN I/0
Registration Number:	2850240	SUPER FEC
Registration Number:	2451604	TERAPOWER
Registration Number:	2735775	TERASTREAM
Registration Number:	2511629	TIMESTREAM
Registration Number:	2695612	UNIPHY
Registration Number:	2487476	V
Registration Number:	2637927	V-DRIVE 2.5
Registration Number:	2766449	VERIPHY
Registration Number:	2637926	V-FRAME 2.5
Registration Number:	1959483	VITESSE
Registration Number:	2682324	VITESSE
Registration Number:	2641504	V-PHY 2.5

CORRESPONDENCE DATA

Fax Number: (612)340-8856
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: (612) 492-6842
Email: ip.docket@dorsey.com
Correspondent Name: Jeffrey R. Cadwell
Address Line 1: 50 South Sixth Street
Address Line 2: Suite 1500
Address Line 4: Minneapolis, MINNESOTA 55402-1498

ATTORNEY DOCKET NUMBER:	11,323
NAME OF SUBMITTER:	Jeffrey R. Cadwell
Signature:	/Jeffrey R. Cadwell/
Date:	10/22/2009

Total Attachments: 33
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COLLATERAL ASSIGNMENT (INTELLECTUAL PROPERTY)

THIS COLLATERAL ASSIGNMENT (INTELLECTUAL PROPERTY) (this "Collateral Assignment"), dated as of October 29, 2007, is executed by VITESSE SEMICONDUCTOR CORPORATION, a Delaware corporation (the "Assignor"), in favor of WHITEBOX VSC, LTD., a limited partnership organized under the law of the British Virgin Islands, as agent (in such capacity, and together with any successor in such capacity, the "Assignee") for the benefit of the Lenders (as such terms are defined below).

RECITALS

A. The Assignor executed a Loan Agreement dated as of August 23, 2007 (as the same may hereafter be amended, supplemented, extended, increased, restated or otherwise modified from time to time, and together with any substitutions, replacements or refinancings thereof, the "Loan Agreement "), among the Assignor, the lenders from time to time party thereto (the "Lenders ") and the Assignee, one of the Lenders, as agent for the Lenders.

B. The Assignor has pledged and granted to the Assignee a security interest in the property described in a Security Agreement dated concurrently herewith (the "Security Agreement") by and between Assignor and Assignee, which property includes general intangibles, including, without limitation, applications for patents, applications for trademarks, trademarks, trade names, domain names, copyrights, patents, inventions and trade secrets.

C. The Assignor owns the patent registrations set forth in Schedule 1 attached hereto, and the patents so listed are registered or application has been made for such registration as noted in Schedule 1 in the United States Patent and Trademark Office (the "Patent Registrations").

D. The Assignor owns the trademarks, domain names, and trade names set forth in Schedule 2 attached hereto, and the trademarks so listed are registered or application has been made for such registration, as noted in Schedule 2, in the United States Patent and Trademark Office (the "Trademark Registrations").

E. The Assignor owns the copyright registrations set forth in Schedule 3 attached hereto, and the copyrights so listed are registered in the United States Copyright Office (the "Copyright Registrations").

F. The Assignor expects to derive benefits from the extension of credit accommodations to the Assignor by the Lenders and finds it advantageous, desirable and in its best interest to execute this Collateral Assignment to the Assignee in order to secure the payment and performance of (a) all indebtedness, liabilities and obligations of the Assignor to the Lender or every kind, nature or description under the Loan Agreement, including the Assignor's obligation on any promissory note or notes under the Loan Agreement and any note or notes hereafter issued in substitution or replacement thereof, in all cases whether due or to become due, and whether now existing or hereafter arising or incurred and (b) any and all liabilities and obligations of the Assignor to the Lenders and the Agent of every kind, nature and description, whether direct or indirect or hereafter acquired by the Lenders from any Person, absolute or contingent, regardless of how such liabilities arise or by what agreement or instrument they may

be evidenced, and (c) in all of the foregoing cases whether due or to become due, and whether now existing or hereafter arising or incurred for the benefit of the Lenders (the "Liabilities").

AGREEMENT

NOW, THEREFORE, in consideration of the premises and to induce the Lenders to extend credit accommodations to the Assignor pursuant to the Loan Agreement, the parties hereto agree as follows:

1. The Assignor:

(a) does hereby assign all of its right, title and interest in and to all of the present United States patents and the registrations and applications therefor owned by the Assignor together with inventions disclosed therein, including but not limited to those registered patents set forth on Schedule 1, and including, without limitation, all proceeds thereof together with the right to recover for past, present and future infringements, all rights corresponding thereto throughout the world and all renewals and extensions thereof (the "Patents"), said Patents to be held and enjoyed by the Assignee, for its own use and behalf, and for its legal representatives, successors and assigns, as fully and entirely as the same would have been held by the Assignor had this Collateral Assignment not been made.

(b) does hereby assign all of its right, title and interest in and to all of the present trademarks, domain names, and trade names and the registrations and applications therefor owned by the Assignor, including but not limited to those set forth on Schedule 2, and including, without limitation, all proceeds thereof together with the right to recover for past, present and future infringements, all rights corresponding thereto throughout the world and all renewals and extensions thereof (the "Trademarks"), together with the goodwill of the business associated with said Trademarks, said Trademarks to be held and enjoyed by the Assignee or its designee for its use and behalf, and for the legal representatives, successors and assigns of the Assignee or its designee, as fully and entirely as the same would have been held by the Assignor had this Collateral Assignment not been made.

(c) does hereby assign all of its right, title and interest in and to all of the present United States copyrights, registered or unregistered, now or hereafter acquired, by Assignor in and to all copyrightable works, including, but not limited to, those copyright registrations identified on Schedule 3, and including all applications therefor, and (i) any renewals or extensions of the registrations therefor, (ii) all damages and payments for past, present and future infringements thereof, (iii) the right to sue and recover for past, present and future infringements thereof, and (iv) all rights corresponding thereto throughout the world (the "Copyrights").

The foregoing assignments shall be effective only upon the occurrence and continuance of an Event of Default under the Loan Agreement and upon written notice by the Assignee to the Assignor of the acceptance by the Assignee of this Collateral Assignment, which written notice shall constitute conclusive proof of the matters set forth therein; unless and until the occurrence of such an Event of Default, such assignments shall have no effect. After the occurrence and continuation of an Event of Default under the Loan Agreement, the Assignee shall be entitled to transfer (i) the Patent Registrations pursuant to the Assignment of Patents attached hereto as

Exhibit A, (ii) the Copyright Registrations pursuant to the Assignment of Copyrights attached hereto as Exhibit B, and (iii) the Trademark Registrations pursuant to an Assignment of Trademarks substantially in the form of Exhibit C. Assignor hereby irrevocably authorizes the Assignee to complete each of the undated Assignments of Patents, Assignment of Copyrights and Assignment of Trademarks at the time of transfer and agrees to sign whatever documents are necessary to transfer ownership of Assignor's domain names from Assignor to the new owner.

Notwithstanding the foregoing provisions of this Section 1, the Assignee acquires no security interest or other rights in the United States for any Trademark that is the subject of an intent-to-use application before the U.S. Patent and Trademark Office until such time as a verified amendment to allege use or statement of use is filed for such application or the Assignee arranges for an assignment of such Trademarks from the Assignee to a purchaser that would satisfy the requirements of Section 10 of the Lanham Act, 15 U.S.C. Section 1060. At the time that Assignee seeks to transfer all other Trademarks pursuant to an Assignment of Trademarks in the form of Exhibit C, it may also complete Exhibit D with respect to any U.S. intent-to-use applications and, provided that Exhibit D satisfies the conditions of the preceding sentence, Assignor agrees that it will promptly execute and return the same to Assignee.

2. The Assignor hereby covenants and warrants that:

(a) except for applications pending, the Patent Registrations listed on Schedule 1 and the Trademark Registrations listed on Schedule 2 have been duly issued and are registered and subsisting and have not been adjudged invalid or unenforceable in whole or in part;

(b) each of the Patent Registrations listed on Schedule 1, each of the Trademark Registrations listed on Schedule 2, and each of the Copyright Registrations listed on Schedule 3 is valid and enforceable;

(c) to the knowledge of the Assignor, no claim has been made to the Assignor or to any other person, that any of the Patent Registrations or use of the inventions described therein, any of the Trademark Registrations, or any of the Copyright Registrations does or may violate the rights of any third person and no claim has been made by the Assignor that any other person is infringing upon the rights of the Assignor under the Patent Registrations, the Trademark Registrations, or the Copyright Registrations;

(d) the Assignor has the unqualified right to enter into this Collateral Assignment and perform its terms;

(e) the Assignor will be, until the Liabilities shall have been satisfied in full and the Loan Documents (as such term is defined in the Loan Agreement, hereinafter the "Loan Documents") shall have been terminated, in compliance with statutory notice requirements relating to the Patent Registrations, the Trademark Registrations and the Copyright Registrations;

(f) the Assignor is the sole and exclusive owner of the entire and unencumbered right, title and interest in and to each of the Patent Registrations listed on Schedule 1, each of the Trademark Registrations listed on Schedule 2, and each of the Copyright Registrations listed on Schedule 3, free and clear of any liens, charges and encumbrances, including without limitation, licenses and covenants by the Assignor not to sue third persons but excluding Permitted Licenses (as defined below);

(g) the Patent Registrations listed on Schedule 1 are all of the United States Patents and applications therefor now owned by the Assignor, the Trademark Registrations listed on Schedule 2 are all of the United States trademark registrations and applications therefore owned by the Assignor, and the Copyright Registrations listed on Schedule 3 are all of the United States Copyright Registrations and applications therefore now owned by the Assignor;

(h) the Assignor has marked with an asterisk each U.S. intent-to-use trademark application listed on Schedule 2 for which a verified amendment to allege use or statement of use has not been filed; and

(i) the Assignor will, at any time upon request, communicate to the Assignee, its successors and assigns, any facts relating to the Patent Registrations, the Trademark Registrations, and Copyright Registrations or the history thereof as may be known to the Assignor or its officers, employees and agents, and cause such officers, employees and agents to testify as to the same in any infringement or other litigation at the request of the Assignee.

3. The Assignor agrees that, until the rights of the Assignee in the Patent Registrations, Trademark Registrations and Copyright Registrations are terminated pursuant to Section 6, it will not enter into any agreement that is in conflict with its obligations under this Collateral Assignment.

4. If, before the Liabilities shall have been satisfied in full, the Assignor shall obtain rights to any new patent, trademark, domain name, trade name, copyright or any enhancements or derivative works, or become entitled to the benefit of any patent, registration or any renewal or extension of any patent registration, such shall be included in the definition of "Patents" (except for purposes of Section 2 hereof) as used in this Collateral Assignment, or become entitled to the benefit of any trademark application, registration, trademark, domain name, or trade name or any renewal or extension of any trademark registration or domain name, such shall be included in the definition of "Trademarks" as used in this Collateral Assignment (except for purposes of Section 2 hereof), obtain any new copyright or any enhancements or derivative works therefrom, such copyrights shall be included in the definition of "Copyrights" (except for purposes of Section 2 hereof) as used in this Collateral Assignment, and Section 1 hereof shall automatically apply to the foregoing, and the Assignor shall give to the Assignee prompt notice thereof in writing, and the Assignor shall submit annual reports to the Assignee each year not later than December 31st notifying Assignee of (i) any new patents, (ii) any new trademarks, domain names, or trade names adopted, acquired, or applied for during the previous year and (iii) any changes to the status of any previously listed Trademarks, including without limitation U.S. trademark applications for which verified amendments to allege use and statements of use

have now been filed and (iv) any new copyrights. If the Assignee does not receive such a report within fifteen days after the deadline, then the Assignee is authorized to obtain updated information on the Trademarks from the appropriate trademark registrars or third party providers at the Assignor's expense. Upon the reasonable request of the Assignee, the Assignor shall have the duty to immediately apply for registration of any such Copyright with the Register of Copyrights. Any expenses incurred in connection with applications that constitute Copyrights shall be borne by the Assignor. The Assignor authorizes the Assignee to modify this Collateral Assignment by amending Schedule 1 to include any future patent, by amending Schedule 2 to include any future trademark, domain name, or trade name or by amending Schedule 3 to include to include any future copyright.

5. The Assignor agrees not to sell, assign or encumber its interest in, or grant any license with respect to, any of the Patent Registrations, Trademark Registrations or Copyright Registrations, except for the licenses listed on Schedule 4 attached hereto and except for licenses created after the date hereof in the ordinary course of the Assignor's business (collectively, the "Permitted Licenses").

6. The Assignor agrees that it will authorize, execute and deliver to Assignee all documents requested by Assignee to facilitate the purposes of this Collateral Assignment, including, but not limited to, documents required to record Assignee's interest in any appropriate office in any domestic or foreign jurisdiction. At the time the annual report is prepared in accordance with Section 4, Assignor agrees to provide Assignee with updated Schedules to this Agreement for filing with the U.S. Patent and Trademark Office. If the Assignee does not receive the updated Schedules within fifteen (15) days after the deadline, then Assignee is authorized to prepare and record such Schedules at the Assignor's expense. At such time as the Loan Agreement and the other Loan Documents shall have been terminated in accordance with their terms, the Assignee shall on demand of the Assignor execute and deliver to the Assignor all termination statements and other instruments as may be necessary or proper to terminate this Collateral Assignment and assign to the Assignor all the Assignee's rights in the Patent Registrations, Trademark Registrations and Copyright Registrations subject to any disposition thereof which may have been made by the Assignee pursuant hereto or pursuant to the Loan Agreement or any Loan Documents, as defined therein.

7. The Assignor shall have the duty, through counsel selected by the Assignor and reasonably acceptable to the Assignee, (i) to prosecute diligently any pending Patent or Trademark application as of the date of this Collateral Assignment or thereafter until the Loan Agreement and the Loan Documents shall have been terminated in accordance with their terms; provided, that the Assignor may abandon any such application upon thirty days' written notice to the Assignee, (ii) to make application on those patentable inventions, products and processes, trademarks and tradenames which are unregistered but capable of being registered and which a prudent person in the same line of business and similarly situated as the Assignor would reasonably cause to be registered and (iii) to preserve and maintain all rights in all Patent Registrations and Trademark Registrations which a prudent person would reasonably preserve and maintain. Any expenses incurred in connection with applications that constitute Patent Registrations shall be borne by the Assignor. The Assignor shall not abandon any application presently pending that constitutes a Patent or Trademark without the written consent of the Assignee.

8. The Assignee shall have the right but shall in no way be obligated to bring suit in its own name to enforce or to defend the Patent Registrations, Trademark Registrations and Copyright Registrations and any license thereunder if the Assignor has failed to bring such suit in circumstances in which a prudent person in the same line of business and similarly situated as the Assignor would have brought such suit. The Assignor shall at the request of the Assignee do any and all lawful acts and execute any and all proper documents required by the Assignee in aid of such enforcement or defense (including, without limitation, participation as a plaintiff or defendant in any proceeding) and, if Assignor has failed to bring such suit in circumstances in which a prudent person would have brought such suit, the Assignor shall promptly, upon demand, reimburse and indemnify the Assignee for all reasonable costs and expenses incurred by the Assignee in the exercise of its rights under this Section.

9. This Collateral Assignment shall also serve to further evidence the security interest in the Patent Registrations, Trademark Registrations and Copyright Registrations granted by the Assignor to the Assignee pursuant to the Security Agreement.

10. No course of dealing between the Assignor and the Assignee, failure to exercise, nor any delay in exercising, on the part of the Assignee, with respect to any right, power or privilege hereunder shall operate as a waiver thereof; nor shall any single or partial exercise of any right, power or privilege hereunder preclude any other or further exercise thereof or the exercise of any other right, power or privilege.

11. All of the Assignee's rights and remedies with respect to the Patent Registrations, Trademark Registrations and Copyright Registrations, whether established hereby, by any other agreements or by law shall be cumulative and may be exercised singularly or concurrently.

12. This Collateral Assignment is subject to modification only by a writing signed by the parties, except as provided in Section 4 hereof.

13. This Collateral Assignment shall inure to the benefit of and be binding upon the respective successors and permitted assigns of the Assignor and the Assignee.

14. Upon payment in full of all Liabilities (other than Assignor's unmatured indemnity obligations under any Loan Document) and the expiration or termination of any obligation of the Lenders to extend credit accommodations to the Assignor, this Collateral Assignment shall terminate and all rights to the Patent Registrations, Trademark Registrations and Copyright Registrations shall revert to the Assignor.

15. THIS COLLATERAL ASSIGNMENT AND THE RIGHTS AND OBLIGATIONS OF THE PARTIES HEREUNDER SHALL BE CONSTRUED IN ACCORDANCE WITH AND GOVERNED BY THE LAWS (WITHOUT GIVING EFFECT TO THE CONFLICTS OF LAW PRINCIPLES THEREOF) OF (I) ANY STATE AS TO RIGHTS OR INTEREST HEREUNDER WHICH ARISE UNDER THE LAWS OF SUCH STATE, (II) THE UNITED STATES OF AMERICA AS TO RIGHTS AND INTERESTS HEREUNDER WHICH ARE REGISTERED OR FOR THE REGISTRATION OF WHICH APPLICATION IS PENDING WITH THE UNITED STATES PATENT AND TRADEMARK OFFICE, (III) THE UNITED STATES OF AMERICA AS TO RIGHTS AND INTERESTS

HEREUNDER WHICH ARE REGISTERED OR FOR THE REGISTRATION OF WHICH APPLICATION IS PENDING WITH THE UNITED STATES COPYRIGHT OFFICE AND (IV) THE STATE OF NEW YORK IN ALL OTHER RESPECTS. WHENEVER POSSIBLE, EACH PROVISION OF THIS COLLATERAL ASSIGNMENT AND ANY OTHER STATEMENT, INSTRUMENT OR TRANSACTION CONTEMPLATED HEREBY OR RELATING HERETO SHALL BE INTERPRETED IN SUCH MANNER AS TO BE EFFECTIVE AND VALID UNDER APPLICABLE LAW, BUT IF ANY PROVISION OF THIS COLLATERAL ASSIGNMENT OR ANY OTHER STATEMENT, INSTRUMENT OR TRANSACTION CONTEMPLATED HEREBY OR RELATING HERETO SHALL BE HELD TO BE PROHIBITED OR INVALID UNDER APPLICABLE LAW, SUCH PROVISION SHALL BE INEFFECTIVE ONLY TO THE EXTENT OF SUCH PROHIBITION OR INVALIDITY, WITHOUT INVALIDATING THE REMAINDER OF SUCH PROVISION OR THE REMAINING PROVISIONS OF THIS COLLATERAL ASSIGNMENT OR ANY OTHER STATEMENT, INSTRUMENT OR TRANSACTION CONTEMPLATED HEREBY OR RELATING HERETO. IN THE EVENT OF ANY CONFLICT WITHIN, BETWEEN OR AMONG THE PROVISIONS OF THIS COLLATERAL ASSIGNMENT, ANY OTHER LOAN DOCUMENT OR ANY OTHER STATEMENT, INSTRUMENT OR TRANSACTION CONTEMPLATED HEREBY OR THEREBY OR RELATING HERETO OR THERETO, THOSE PROVISIONS GIVING THE ASSIGNEE THE GREATER RIGHT SHALL GOVERN.

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IN WITNESS WHEREOF, the Assignor has executed this assignment as of the date first set forth above.

VITESSE SEMICONDUCTOR CORPORATION

By: _____

Name: Richard C. Ganter

Title: CFO

[Signature Page to Collateral Assignment (Intellectual Property)]

EXHIBIT A TO
COLLATERAL ASSIGNMENT (INTELLECTUAL PROPERTY)

ASSIGNMENT OF PATENTS

This Assignment (this "Assignment") having an effective date of _____, _____ is executed by and between VITESSE SEMICONDUCTOR CORPORATION, a Delaware corporation (the "Assignor"), and _____, a _____, located and doing business at _____ (the "Assignee").

RECITALS

A. The Assignor is the owner by assignment of the entire right, title and interest in and to certain United States Letters Patent, together with the invention(s) disclosed therein.

B. The Assignee is desirous of acquiring the entire right, title, and interest in and to the aforesaid Letters Patent, together with the invention(s) disclosed therein, any and all causes of action and rights of recovery for past infringements of said Letters Patent, and all of the rights vested in said Assignor herein by virtue of the instruments of assignment and/or by virtue of other instruments pursuant to which Assignor became vested with said ownership, including the right, title, and interest in and to any and all improvements acquired pursuant to the terms of said instruments of assignment.

AGREEMENT

NOW, THEREFORE, for good and valuable consideration received by Assignor from Assignee, the receipt in full of which is hereby acknowledged:

1. Assignor hereby sells, assigns, transfers and conveys unto said Assignee the entire right, title and interest in and to said Letters Patent of the United States together with the invention(s) disclosed therein, including each and every Letters Patent which is granted on any application which is a division, substitution or continuation of said Letters Patent, and in and to each and every reissue or extension of said Letters Patent.

2. Assignor further sells, assigns, transfers and conveys unto said Assignee the entire right, title and interest in and to any and all causes of action and rights of recovery for past infringement of the Letters Patent herein assigned.

3. The terms, covenants and provisions of this Assignment shall inure to the benefit of Assignee, its successors, assigns, and/or legal representatives, and shall be binding upon said Assignor, its successors, assigns and/or other legal representatives.

4. Assignor hereby irrevocably authorizes Whitebox VSC, Ltd., or any successor collateral agent to date this undated Assignment and otherwise complete this Assignment at the time of transfer.

[The remainder of this page is intentionally left blank.]

IN WITNESS WHEREOF, the parties have executed this Collateral Assignment as of the dates identified below.

VITESSE SEMICONDUCTOR CORPORATION
(Assignor)

Date: _____

By: _____

Name: Richard C Yonker

Title: CFO

_____ (Assignee)

Date: _____

By: _____

Name: _____

Title: _____

[Signature Page to Collateral Assignment (Patents)]

EXHIBIT B TO
COLLATERAL ASSIGNMENT (INTELLECTUAL PROPERTY)

ASSIGNMENT OF COPYRIGHTS

This Assignment having an effective date of _____, _____ is executed by and between VITESSE SEMICONDUCTOR CORPORATION, a Delaware corporation (the "Assignor"), and _____, a _____, located and doing business at _____ (the "Assignee").

RECITALS

A. Assignor is the owner of copyrights in certain works (the "Works"), including, but not limited to, copyrights registered in the United States Copyright Office and,

B. Assignee desires to acquire all of Assignor's right, title and interest in and to the copyrights in such Works;

AGREEMENT

NOW, THEREFORE, for good and valuable consideration received by Assignor from Assignee, the receipt in full of which is hereby acknowledged:

1. Assignor does hereby sell, assign and transfer unto Assignee, and its successors and assigns, all of its right, title and interest in and to the Works, and the registrations therefor, together with Assignor's entire right, title and interest in and to any and all causes of action and rights of recovery for past infringement. Assignor hereby covenants that it has full right to convey the entire interest herein assigned, and that it has not executed, and will not execute, any agreements inconsistent herewith.

2. The terms, covenants and provisions of this Assignment shall inure to the benefit of Assignee, its successors, assigns, and/or legal representatives, and shall be binding upon said Assignor, its successors, assigns and/or other legal representatives.

3. Assignor hereby irrevocably authorizes Whitebox VSC, Ltd., or any successor collateral agent to date this undated Assignment and otherwise complete this Assignment at the time of transfer.

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IN WITNESS WHEREOF, the parties have executed and delivered this assignment this _____day of _____, _____.

VITESSE SEMICONDUCTOR CORPORATION, the Assignor

By: _____

Name: Richard C Yonker

Title: CFO

_____, the Assignee

By: _____

Name: _____

Title: _____

[Signature Page to Collateral Assignment (Copyrights)]

EXHIBIT C TO
COLLATERAL ASSIGNMENT (INTELLECTUAL PROPERTY)

ASSIGNMENT OF TRADEMARKS

(Registered and Pending Use-Based Applications)

This Assignment having an effective date of _____, _____ is executed by and between VITESSE SEMICONDUCTOR CORPORATION, a Delaware corporation (the "Assignor"), and _____, a _____, located and doing business at _____ (the "Assignee").

RECITALS

A. The Assignor has adopted and owns certain trademarks which are registered in the U.S. Patent and Trademark Office, or which are the subject of pending use-based applications in the U.S. Patent and Trademark Office (the "Marks").

B. The Assignee is desirous of acquiring the entire right, title, and interest in the Marks and registration therefor.

AGREEMENT

1. Assignor does hereby sell, assign and transfer unto Assignee, and its successors and assigns, all of its right, title and interest in and to the Marks, and the registrations therefor, together with that part of the good will of the business connected with the use of and symbolized by the Marks, together with Assignor's entire right, title and interest in and to any and all causes of action and rights of recovery for past infringement. Assignor hereby covenants that it has full right to convey the entire interest herein assigned, and that it has not executed, and will not execute, any agreements inconsistent herewith.

2. The terms, covenants and provisions of this Assignment shall inure to the benefit of Assignee, its successors, assigns, and/or legal representatives, and shall be binding upon said Assignor, its successors, assigns and/or other legal representatives.

3. Assignor hereby irrevocably authorizes Whitebox VSC, Ltd., or any successor collateral agent to date this undated Assignment and otherwise complete this Assignment at the time of transfer.

[The remainder of this page is intentionally left blank.]

IN WITNESS WHEREOF, the parties have executed this assignment as of the dates identified below.

VITESSE SEMICONDUCTOR CORPORATION

(Assignor)

Date: _____

By: _____

Name: Richard C. Yonker

Title: CFO

_____ (Assignee)

Date: _____

By: _____

Name: _____

Title: _____

[Signature Page to Collateral Assignment (Trademarks)]

EXHIBIT D TO
COLLATERAL ASSIGNMENT OF TRADEMARKS

ASSIGNMENT OF TRADEMARKS

(Intent-To-Use Applications)

This Collateral Assignment having an effective date of _____, _____ is executed by and between VITESSE SEMICONDUCTOR CORPORATION, a Delaware corporation (the "Assignor"), and _____, a _____, located and doing business at _____ (the "Assignee").

RECITALS

A. The Assignor has adopted and owns certain trademarks which are the subject of pending intent-to-use applications in the U.S. Patent and Trademark Office (the "Marks").

B. The Assignee is desirous of acquiring the entire right, title, and interest in the Marks and applications therefor.

AGREEMENT

NOW THEREFORE, in consideration of and in exchange for good and valuable consideration, the receipt of which is hereby acknowledged:

1. Assignor does hereby sell, assign and transfer unto Assignee, and its successors and assigns, all of its right, title and interest in and to the Marks, and the applications therefor, together with that part of the good will of the business connected with the use of and symbolized by the Marks, and including Assignor's entire right, title and interest in and to any and all causes of action and rights of recovery for past infringement of the Marks. Assignor hereby covenants that it has full right to convey the entire interest herein assigned, and that it has not executed, and will not execute, any agreements inconsistent herewith. As indicated below, each Mark is the subject of a verified allegation of use under §§ 1(c) or 1(d) of the Lanham Act that has been filed with the U.S. Patent and Trademark Office, or it is being assigned as part of a transfer of the entire business or portion thereof to which the Marks pertain as required by § 10 of the Lanham Act.

2. The terms, covenants and provisions of this Assignment shall inure to the benefit of Assignee, its successors, assigns, and/or legal representatives, and shall be binding upon said Assignor, its successors, assigns and/or other legal representatives.

3. Assignor hereby irrevocably authorizes Whitebox VSC, Ltd., or any successor collateral agent to date this undated Assignment and otherwise complete this Assignment at the time of transfer.

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IN WITNESS WHEREOF, the parties have executed this assignment as of the dates identified below.

VITESSE SEMICONDUCTOR CORPORATION

(Assignor)

Date: _____

By: _____

Name: Richard C. Yonker

Title: CFO

_____ (Assignee)

Date: _____

By: _____

Name: _____

Title: _____

[Signature Page to Collateral Assignment (Trademarks)]

SCHEDULE 1 TO THE COLLATERAL ASSIGNMENT
PATENT REGISTRATIONS

Patent No.		Title	Issue Date	Inventor
1	4,935,647	Group III - V Semiconductor Devices With Improved Switching Speeds	June 19, 1990	William Larkins
2	4,939,390	Current Steering Fet Logic Circuit	July 3, 1990	Timothy Coe
3	5,121,174	Gate-To-Ohmic Metal Contact Scheme For Iii-V Devices	June 9, 1992	C. David Forgerson II et al.
4	5,144,410	Ohmic Contact For III-V Semiconductor Devices	September 1, 1992	David A. Johnson
5	5,153,852	Static Ram Cell With High Speed And Improved Cell Stability	October 6, 1992	William C. Terrell
6	5,180,936	High Speed Logic Circuit	January 19, 1993	James McDonald
7	5,204,559	Method And Apparatus For Controlling Clock Skew	April 20, 1993	Ira Deyhimy et al.
8	5,600,266	Digital Logic Protocol Interface For Different Semiconductor Technologies	February 4, 1997	William C. Terrell et al.
9	5,694,070	Distributed Ramp Delay Generator	December 2, 1997	Alistair D. Black
10	5,849,630	Process For Forming Ohmic Contact For III-V Semiconductor Devices	December 15, 1998	David A. Johnson
11	5,983,303	Bus Arrangements For Interconnection Of Discrete And/Or Integrated Modules In A Digital System And Associated Method	November 9, 1999	Stephan J. Sheafor et al.
12	6,034,570	Gallium Arsenide Voltage-Controlled Oscillator And Oscillator Delay Cell	March 7, 2000	Greg Warwar
13	6,076,115	Media Access Control Receiver And Network Management System	June 13, 2000	Namakkal S. Sambamurthy et al.
14	6,078,194	Logic Gates For Reducing Power Consumption Of Gallium	June 20, 2000	Gary M. Lee
15	6,084,478	Transimpedance Amplifier With Automatic Gain Control	July 4, 2000	Balagopal Mayampurath
16	6,085,248	Media Access Control Transmitter And Parallel Network Management System	July 4, 2000	Namakkal S. Sambamurthy, et al.
17	6,088,753	Bus Arrangements For Interconnection Of Discrete And/Or Integrated Modules In A Digital System And Associated Method	July 11, 2000	Stephan J. Sheafor et al.
18	6,108,713	Media Access Control Architectures And Network Management Systems	August 22, 2000	Namakkal S. Sambamurthy et al.
19	6,115,416	Pulse Code Sequence Analyzer	September 5, 2000	Vladimir Katzman
20	6,119,188	Priority Allocation In A Bus Interconnected Discrete And/Or Integrated Digital Multi-Module System	September 12, 2000	Stephen J. Sheafor et al.
21	6,167,029	System And Method For Integrated Data Flow Control	December 26, 2000	Gopal Ramakrishnan
22	6,172,990	Media Access Control Micro-Risc Stream Processor And Method For Implementing The Same	January 9, 2001	Alak K. Deb et al.
23	6,178,213	Adaptive Data Recovery System And Methods	January 23, 2001	Gary D. Mccormack et al.
24	6,204,733	Multiple-Phase-Interpolation LC Voltage-Controlled Oscillator	March 20, 2001	Yijun Cai

Patent No.		Title	Issue Date	Inventor
25	6,218,905	Common-Gate Transimpedance Amplifier With Dynamically Controlled Input Impedance	April 17, 2001	Jeffrey W. Sanders et al.
26	6,223,242	Linearly Expandable Self-Routing Crossbar Switch	April 24, 2001	Stephen J. Sheafor et al.
27	6,229,344	Phase Selection Circuit	May 8, 2001	Greg Warwar
28	6,229,367	Method And Apparatus For Generating A Time Delayed Signal With A Minimum Data Dependency Error Using An Oscillator	May 8, 2001	Ashish K. Choudhury
29	6,232,844	Oscillator Using A Phase Detector And Phase Shifter	May 15, 2001	Ronald F. Talaga, Jr.
30	6,263,034	Circuit And Technique For Digital Reduction Of Jitter	July 17, 2001	Bradley M. Kanack et al.
31	6,311,244	Priority Allocation In A Bus Interconnected Discrete And/Or Integrated Digital Multi-Module System	October 30, 2001	Stephen J. Sheafor et al.
32	6,321,285	Bus Arrangements For Interconnection Of Discrete And/Or Integrated Modules In A Digital System And Associated Method	November 20, 2001	Stephen J. Sheafor et al.
33	6,366,140	Method And Circuitry For High Speed Buffering Of Clocks Signals	April 2, 2002	Greg Warwar
34	6,377,575	High Speed Cross Point Switch Routing Circuit With Word-Synchronous Serial Back Plane	April 23, 2002	John P. Mullaney et al.
35	6,393,489	Media Access Control Architectures And Network Management Systems	May 21, 2002	Namakkal S. Sambamurthy et al.
36	6,462,590	High Bandwidth Clock Buffer	October 8, 2002	Greg Warwar
37	6,463,109	Multiple Channel Adaptive Data Recovery System	October 8, 2002	Gary D. McCormack et al.
38	6,473,813	Module Based Address Translation Arrangement And Transaction Offloading In A Digital System	October 29, 2002	Stephan J. Sheafor
39	6,493,407	Synchronous Latching Bus Arrangement For Interfacing Discrete And/Or Integrated Modules In A Digital System And Associated Method	December 10, 2002	Stephan J. Sheafor et al.
40	6,545,567	Programmable Analog Tapped Delay Line Filter Having Cascaded Differential Delay Cells	April 8, 2003	Shanthi Pavan, et al.
41	6,559,682	Dual-Mixer Loss Of Signal Detection Circuit	May 6, 2003	Ian Kyles et al.
42	6,566,904	Pad Calibration Circuit With On-Chip Resistor	May 20, 2003	Nicholas van Bavel et al.
43	6,580,846	Actively-Controllable Optical Switches Based On Optical Position Sensing And Applications In Optical Switching Arrays	June 17, 2003	Alan C. Burroughs, et al.
44	6,604,206	Reduced GMII With Internal Timing Compensation	August 5, 2003	Mandeep Singh Chadha, et al.
45	6,605,958	Precision On-Chip Transmission Line Termination	August 12, 2003	Dave Bergman et al.
46	6,633,191	Clock Buffer With DC Offset Suppression	October 14, 2003	Yagi Hu
47	6,633,605	Pulse Code Sequence Analyzer	October 14, 2003	Vladimir Katsman, et al.
48	6,665,347	Output Driver For High Speed Ethernet Transceiver	December 16, 2003	Nicholas van Bavel, et al.
49	6,683,896	Method Of Controlling The Turn Off Characteristics Of A VCSEL Diode	January 27, 2004	Randy T. Heilman et al.
50	6,694,476	Reed-Solomon Encoder And Decoder	February 17, 2004	Satish Sridharan et

Patent No.		Title	Issue Date	Inventor
				al.
51	6,700,886	High Speed Cross Point Switch Routing Circuit With Word-Synchronous Serial Back Plane	March 2, 2004	John P. Mullaney et al.
52	6,713,749	Monolithic Loss-Of-Signal Detect Circuitry	March 30, 2004	Adam A. Wu et al.
53	6,727,777	Apparatus And Method For Angles Coaxial To Planar Structure Broadband Transition	April 27, 2004	Robert J. McDonough et al.
54	6,737,995	Clock and Data Recovery With A Feedback Loop To Adjust The Slice Level Of An Input Sampling Circuit	May 18, 2004	Devin Kenji Ng, et al.
55	6,738,173	Limiting Amplifier Modulator Driver	May 18, 2004	Bonthron et al.
56	6,738,922	Clock Recovery Unit Including A Frequency Detection	May 18, 2004	Greg Warwar et al.
57	6,738,942	Product Code Based Forward Error Correction System	May 18, 2004	Satish Sridharan
58	6,746,950	Low Temperature Aluminum Planarization Process	June 8, 2004	Ende Shan
59	6,768,347	Precise Phase Detector	July 27, 2004	John Khoury et al.
60	6,801,518	High Speed Cross Point Switch Routing Circuit With Word-Synchronous Serial Back Plane	October 5, 2004	John P. Mullaney et al.
61	6,810,499	Product Code Based Forward Error Correction System	October 26, 2004	Satish Sridharan et al.
62	6,833,743	Adjustment Of A Clock Duty Cycle	December 21, 2004	Gong Gu, et al.
63	6,844,952	Actuator-Controlled Mirror With Z-Stop Mechanism	January 18, 2005	Warren Dalziel
64	6,850,661	Multiple Element Controlled Optical Coupling	February 1, 2005	Daljeet Singh
65	6,873,029	Self-Aligned Bipolar Transistor	March 29, 2005	Gang He et al.
66	6,904,061	Transparent Transport Overhead Mapping	June 7, 2005	Andrew Schmitt et al.
67	6,925,218	Control-Techniques And Devices For An Optical Switch Array	August 2, 2005	Alan C. Burroughs
68	6,933,793	Method Of Overtone Selection And Level Control In An Integrated Circuit CMOS Negative Resistance Oscillator To Achieve Low Jitter	August 23, 2005	Raymond B. Patterson, III, et al.
69	6,946,948	Crosspoint Switch With Switch Matrix Module	September 20, 2005	Gary McCormack, et al.
70	6,948,109	Low-Density Parity Check Forward Error Correction	September 20, 2005	Tim Coe
71	6,967,471	Switching Mode Regular For SFP Ethernet Adaptor	November 22, 2005	John James Paulos
72	6,990,162	Scalable Clock Distribution For Multiple CRU On The Same Chip	January 24, 2006	Chuong D. Vu
73	6,996,202	Multiple Channel Adaptive Data Recovery System	February 7, 2006	Gary D. McCormack, et al.
74	6,998,292	Apparatus And Method For Interchip Or Chip-To-Substrate Connection With A Sub-Carrier	February 14, 2006	Robert J. McDonough, et al.
75	7,003,228	Method And Apparatus For Improved High-Speed Adaptive Equalization	February 21, 2006	John S. Wang, et al.
76	7,119,611	On-Chip Calibrated Source Termination For Voltage Mode Driver and Method Of Calibration Thereof	October 10, 2006	Eric James Wyers, et al.
77	7,123,678	RZ Recovery	October 17, 2006	Norm Hendrickson

Patent No.		Title	Issue Date	Inventor
78	7,132,849	Method And Apparatus For Configuring The Operation Of An Integrated Circuit	November 7, 2006	John Tucker, et al.
79	7,142,596	Integrated Circuit Implementation For Power And Area Efficient Adaptive Equalization	November 28, 2006	Shanthi Pavan, et al.
80	7,158,567	Method And Apparatus For Improved High-Speed FEC Adaptive Equalization	January 2, 2007	John S. Wang, et al.
81	7,161,901	Automatic Load Balancing In Switch Fabrics	January 9, 2007	Chuong D. Vu
82	7,164,677	Data Switching System	January 16, 2007	Jens P. Tagore-Brage
83	7,200,176	Transformerless Ethernet Controller	April 3, 2007	John Paulos et al.
84	7,227,878	Differential Opto-Electronics Transmitter	June 5, 2007	Lawrence Choi et al.
85	7,230,923	Time Based Packet Scheduling And Sorting System	June 12, 2007	O. Raif Onvural et al.
86	7,231,008	Fast Locking Clock And Data Recovery Unit	June 12, 2007	Ashish K. Choudhury et al.
87	7,236,084	Crosspoint Switch With Switch Matrix Module	June 26, 2007	Gary McCormack et al.

SCHEDULE 2 TO THE COLLATERAL ASSIGNMENT
TRADEMARK REGISTRATIONS

MARK	S/N or R/N	STATUS	PENDING ACTION
ACTIPHY	3004768	Registered	This mark was registered on 10/04/05. The next step is to file an Affidavit of Use, which is due between ***10/04/10*** and ***10/04/11***.
CROSSSTREAM	2543805	Registered	This mark was registered on 03/05/02. The next step is to file an Affidavit of Use, which is due between ***03/05/07*** and ***03/05/08***. 03/26/07: Email to Jenny Bryan requesting specimens of use or confirmation that mark is to be abandoned. ***Awaiting client response.***
FIBERSTREAM	2616224	Registered	This mark was registered on 09/10/02. An Affidavit of Use is due between ***09/10/07*** and ***09/10/08***.
FIBRETIMER	2526300	Registered [on Supplemental Register]	This mark was registered on 01/01/02 on the Supplemental Register. Assuming five years continuous use of the mark, the next step is to refile the application for registration on the Principal Register on ***01/01/07*** *and* ***01/01/08***. 01/04/07: Michelle Morris advised J. Bryan re: deadline to file Declaration of Use & recommended filing of application to register mark on the Principal Register. ***Awaiting client response.***
FOCUS CONNECT	3007582	Registered	This mark was registered on 10/18/05. The next step is to file an Affidavit of Use, which is due between ***10/18/10*** and ***10/18/11***.
IQ10G	2744204	Registered	This mark was registered on 07/29/03. The next step is to file an Affidavit of Use, which is due between ***07/29/08*** and ***07/29/09***
IQ2000	2661839	Registered	This mark was registered on 2/17/02. The next step is to file an Affidavit of Use between ***12/17/07*** and ***12/17/08***.
IQ2200	2692482	Registered	This mark was registered on 03/04/03. The next step is to file an Affidavit of Use between ***03/04/08*** and ***03/04/09***
MAGNIPHY	2695613	Registered	This mark was registered on 03/11/03. The next step is to file an Affidavit of Use between ***03/11/08*** and ***03/11/09***
MONITOR 4.8	2706045	Registered	This mark was registered on 04/15/03. The next step is to file an Affidavit of Use between ***04/15/08*** and ***04/15/09***

MARK	S/N or R/N	STATUS	PENDING ACTION
MULTILINK	2694410	Registered	Owned by Multilink Technology Corporation which was acquired by Vitesse in August 2003. Client to advise whether mark is to be maintained. This mark was registered on 03/11/03. The next step is to file an Affidavit of Use between ***03/11/08*** and ***03/11/09***
	2697316	Registered	Owned by Multilink Technology Corporation which was acquired by Vitesse in August 2003. Client to advise whether mark is to be maintained. This mark was registered on 03/18/03. The next step is to file an Affidavit of Use between ***03/18/08*** and ***03/18/09***
NETWORK ON A CHIP	2607738	Registered	This mark was registered on 08/13/02. The next step is to file an Affidavit of Use, which is due between ***08/13/07*** and ***08/13/08***.
PACEMAKER	2697054	Registered	This mark was registered on 03/18/03. The next step is to file an Affidavit of Use, which is due between ***03/18/08*** and ***03/18/09***.
PACKET EXCHANGE MATRIX	2890481	Registered [on Supplemental Register]	This mark was registered on 09/28/04 on the Supplemental Register. Assuming five years continuous use of the mark, the next step is to refile the application for registration on the Principal Register on ***09/28/09***.
PIXEQ	78/638645	Pending	04/26/07: Second Request for Extension of Time to File Statement of Use filed and accepted. The next deadline to file a Statement of Use, or the Third Extension of Time to File a Statement of Use is ***11/02/07***.
SIMPLIPHY	2695611	Registered	This mark was registered on 03/11/03. The next step is to file an Affidavit of Use between ***03/11/08*** and ***03/11/09***
SIMPLIPIN I/O	2761196	Registered	This mark was registered on 09/09/03. The next step is to file an Affidavit of Use between ***09/09/08*** and ***09/09/09***
SUPER FEC	2850240	Registered	Owned by Multilink Technology Corporation which was acquired by Vitesse in August 2003. Client to advise whether mark is to be maintained. This mark was registered on 06/08/04. The next step is to file an Affidavit of Use between ***06/08/09*** and ***06/08/10***

MARK	S/N or R/N	STATUS	PENDING ACTION
TERAPOWER	2451604	Registered (not being renewed)	This mark was registered on 05/15/01. The next step is to submit an Affidavit of Use, which is due between ***05/15/06*** and ***05/15/07***. On 05/05/06 Lynn Jones advised that client has abandoned the mark. Awaiting issuance of Notice of Cancellation.
TERASTREAM	2735775	Registered	This mark was registered on 07/15/03. The next step is to submit an Affidavit of Use, which is due between ***07/15/08*** and ***07/15/09***.
TIMESTREAM	2511629	Registered	This mark was registered on 11/27/01. The next step is to submit an Affidavit of Use, which is due between ***11/27/06*** and ***11/27/07***. 02/28/07: Letter to client advising Affidavit of Use deadline & requesting specimens. ***Awaiting client response.***
UNIPHY	2695612	Registered	This mark was registered on 03/11/03. The next step is to file an Affidavit of Use between ***03/11/08*** and ***03/11/09***
V (STYLIZED) 	2487476	Registered	This mark was registered on 09/11/01. On 06/22/07, the Combined Declaration of Use & Incontestability was filed. Awaiting USPTO issuance of Notices of Acceptance and Acknowledgement.
V-DRIVE 2.5	2637927	Registered	This mark was registered on 10/22/02. The next step is to submit an Affidavit of Use between ***10/22/07*** and ***10/22/08***.
VERIPHY	2766449	Registered	This mark was registered on 09/23/03. The next step is to file an Affidavit of Use between ***09/23/08*** and ***09/23/09***
V-FRAME 2.5	2637926	Registered	This mark was registered on 10/22/02 The next step is to submit an Affidavit of Use between ***10/22/07*** and ***10/22/08***.
VITESSE	1959483	Registered in Class 9	04/19/06: USPTO issued Notice of Acceptance of Use/Renewal. The next step is to submit an Affidavit of Use/Renewal Application between **03/15/15** and **03/15/16**.
VITESSE	2682324	Registered in Classes 9, 35, 40 & 42	This mark was registered on 02/04/03. The next step is to submit an Affidavit of Use between ***02/04/08*** and ***02/04/09***.

MARK	S/N or R/N	STATUS	PENDING ACTION
V-PHY 2.5	2641504	Registered	This mark was registered on 10/29/02. The next step is to submit an Affidavit of Use between ***10/29/07*** and ***10/29/08***.

SCHEDULE 3 TO
COLLATERAL ASSIGNMENT (INTELLECTUAL PROPERTY)

UNITED STATES COPYRIGHTS

None.

SCHEDULE 4 TO
COLLATERAL ASSIGNMENT (INTELLECTUAL PROPERTY)

LICENSES

See attached.

PARTIES	START	TERMINATION	ASSIGNABLE Y/N
ANSYS	1/29/2001	N/A	Non-assignable
ARANT COMMUNICATIONS	6/18/2001	N/A	Assignable
ARC	12/29/1999	N/A	Assignment needs written consent.
ARM	12/1/2005	12/1/2008	Yes/with prior written consent
Avocent	April, 2006	1/31/2011	VSC452 Assignability needs written consent.
Avocent	1/31/2006	1/31/2011	KVM Technology. Assignability needs written consent.
BMC	8/26/2002	8/26/2007	Yes, w/written consent
DATA BAHN	10/29/2003	N/A	Multilink 6205 Project, VSC9128 Denali Asic Technology. Assignability w/written consent.
DENALI SOFTWARE	12/18/2001	N/A	Yes
EXPRESS LOGIC	11/16/2005	N/A	Yes/with prior written consent
i2 TECHNOLOGY US, INC.	4/17/2006	N/A	Yes, w/written consent
INSILICON	3/30/2001	N/A	Yes, w/written consent
INTEL	11/16/2005	N/A	Yes, w/written consent
INTOTO	5/24/2006	N/A	Yes, w/written consent
ISI	6/26/2000	N/A	Yes, w/written consent
LVL7	10/1/2004	N/A	Yes, w/written consent

LVL7	3/3/2003	N/A	Yes, w/written consent
MELLANOX TECH			
MENTOR GRAPHICS	6/5/2006	N/A	Yes, w/written consent
NETLOGIC	11/16/2001	N/A	Yes, w/written consent
PLD Applications	4/6/2006	N/A	N/A - agreement is silent.
QUALCORE	4/5/2006	4/5/2008	No.
RAD DATA COMMUNICATIONS			
RALINK TECHNOLOGY	3/23/2006	3/23/2009	Yes, w/written consent
SOCLE	3/31/2006	6/30/2008	Yes, w/written consent
STAR SEMICONDUCTOR	2/17/2006	N/A	Yes, w/written consent
SUN MICROSYSTEMS	3/14/2002	N/A	Yes, w/written consent
SYNOPSYS	3/22/1999	N/A	Yes, w/written consent
TEAM 1	3/27/2006	3/27/2007	Yes, w/written consent
TEKELEC	1/1/2004	N/A	No assignability.
TROIKA NETWORKS	3/12/2003	N/A	yes-assignability - VB owns end product.

TROIKA NETWORKS TROPIC NETWORKS TSMC TSMC TSMC TSMC TSMC TURK & TURK ELECTRONIC GMBH UNIVERSITY OF CALIFORNIA UT STARCOM WIND RIVER SYSTEMS XILINX XIOTECH CORP	8/22/2003	8/22/2008	Yes, w/written consent

PRODUCT LICENSED
001 Professional Core, Lan License. ANSYS Professional V5.6 Asic Cores - belonging to Arant RPOH. Receive Path Overhead Termination core (RPOH). Frame Generator/Transmit Path Overhead Generation core (FG/TPOH). Tributary Unit 3 Pointer Interpreter (TU-3 PI) core. VSC9198 Chip, VSC9186,VSC9188, ARC-3, or ARCTANGENT -A4 Architecture. Artisan Physical IP - Ethernet division. Avocent Software Source Code. BMC/KVM interface requirements and pin assignments. Analysis of KVM driver port to BMC and network interface. Definition of KVM feature stack. Analysis of Virtual Media feasibility and performance. Decision on internal memory interface and memory sharing. External memory (Flash & RAM) requirements. KVM subsystem silicon interface spec. Gate level netlist for KVM integration w/memory interface. Standalone test bench for KVM design verification. KVM tests suite and tests specifications. KVM and vMedia executable firmware. ESD Designs, CL013 VSC 9118 Asic Technology, DDR Controller. Semiconductor circuit and logic designs in Verilog. Synthesizable RTL form VSC 9118. EL Licensed Products - ThreadX, MIPS OEM License. - V3000 products storage division. Factory Planner System. PCI-X 64 Bit Core Verilog Platform environment control Interface Specs. VSC 7174 Residential and Solto Broadband Router Software Package. For Demonstration Purposes Only. Rapid control for Web.Mibway Interface. SNMP VI, VZ & MIB Compiler Liason Switch E. Fastpath Software 2000. Solution Version 4.3

Vitesse SDK and HDS. SDK - Software Developer Kits
HDS - Hardware Development Systems
Fastpath Switching, Fastpath Routing, Fastpath Management

ESD Software - Storage Division

MPSI2001V,RTL design, NLEVB2001V Schematics, Interface Code. 1.0, Vitesse IQ 2000 or IQ 2200 N Processors.
ALIC/RSPXP8 Software - Storage division.
Analog IP - Storgae division.

Linux Device Driver
Cetus Plus, Service Agreemtn to Implement ARM926 EJ IP Usage and Netlist-to-Wafer
ARM9 with a 32 bit DDR DRAM interface and 16-bit Static Memory Controller Interface. One RGMII MAC interface, UART, GPIO and integrated regulator, HNAT engine, IDP engine - Ethernet division.
Sunspectrum Support Program Module.
See attached exhibit A.
BSP software package for the VSC7385.
Assembly language/Ct & Source Code for the Expansion Rom Bios
Software. One machine readable copy of all reasonably necessary Software used for the FC Endec to function as a Fibre Channel Arbitrated Loop NL-Port. This does not include the Host Side Driver Code. **Source Code.** RTL Source Code for the FC Endec function including the Buffer Controls and Register Map (including the Python Script). This will not include the PCI/Host Interface. **Verification Code.** All reasonably necessary verification code including without limitation NL Port Model, test benches and stimulus files. **Documentation.** All reasonably necessary documentation and specifications relating to the FC Endec and firmware as well as any reference material showing examples of how it is driven. **Scripts.** All reasonably necessary synthesis scripts including without limitation timing constraints, false paths and multi-cycle paths. **Hardware.** One FPGA Board implementing the FC Endec Function. **Bug Fixes and Workarounds.** List of all known (a) errata, (b) bugs, (C) incompatibilities and tested compatibilities, and (d) all known software workarounds.

TA - 10A5 - 4101, T - 018 - ES - CL - 001

Synopsys

Vitesse Semiconductor Corp. technology pool

Product	Synopsys Product Code	perpetual list price	quantity	totals
DC Ultra		$163,000	10	$1,630,000
DC Expert		$98,000	10	$980,000
DFT Compiler		$45,000	20	$900,000
Verilog Compiler		$26,000	20	$520,000
VHDL Compiler		$26,000	10	$260,000
Design Analyzer		$8,400	20	$168,000
DW Foundation		$48,500	20	$970,000
Primetime		$60,000	14	$840,000
PathMill		$115,000	1	$115,000
PathMill Plus		$185,000	1	$185,000
TimeMill (includes ACE)		$90,000	2	$180,000
PowerMill (includes ACE)		$140,000	4	$560,000
TurboWave-NOVAS		$5,500	5	$27,500
Verilog Netlist Reader		$2,500	2	$5,000
VTRAN		$5,400	2	$10,800
SLE-XP		$80,000	1	$80,000
Antenna Diode		$40,000	1	$40,000
TetraMax		$96,000	3	$288,000
VCS		$45,000	6	$270,000
VMC		~~$150,000~~ 175,000	2 1	$300,000
Scirocco		$45,000	5	$225,000
IDDQ Test		$60,000	2	$120,000
BSD Compiler		$30,000	2	$60,000
VERA Developers kit		$50,400	0	$0
VERA Rutime		$12,000	0	$0
SONET WB++ CORE w/ STS1 binary		$153,000	1	$153,000
SONET WB++ STS3		$3,100	10	$31,000
SONETWB++ STS12		$3,100	10	$31,000
SONET WB++ STS48		$3,100	10	$31,000
SONET WB++ STS192		$3,100	10	$31,000
SONET WB++ ATM_SPE		$7,700	10	$77,000
SONET WB++ DS1_VT_SPE		$7,700	10	$77,000
SONET WB++ DS2_VT_SPE		$4,600	10	$46,000
SONET WB++ DS3_SPE		$4,600	10	$46,000
SONET WB++DS4_SPE		$4,600	10	$46,000
SONET WB++ E1_VT_SPE		$4,600	10	$46,000
SDH WB++ CORE w/ STM1 binary		$153,000	1	$153,000
SDH WB++ STM0		$3,100	10	$31,000
SDH WB++ STM4		$3,100	10	$31,000
SDH WB++ STM16		$3,100	10	$31,000
SDH WB++STM64		$3,100	10	$31,000
SDH WB++ ATM_HVC		$7,700	10	$77,000
SDH WB++ ATM_LVC		$7,700	10	$77,000
SDH WB++ DS1		$4,600	10	$46,000
SDH WB++ E4		$4,600	10	$46,000
SDH WB++ E1		$4,600	10	$46,000
SDH WB++ DS2		$4,600	10	$46,000
SDH WB++ DS3_HVC		$4,600	10	$46,000
SDH WB++ DS3_LVC		$4,600	10	$46,000
SDH WB++ E3_HVC		$4,600	10	$46,000
SDH WB++ E3_LVC		$4,600	10	$46,000
SDH WB++ VC4		$4,600	10	$46,000
SDH WB++ VC12		$4,600	10	$46,000
New licenses perpetual list (not including updates & support)				$10,240,300
Customer Education training (student days)		$600	100	$60,000
licenses + training credits				$10,300,300

Exhibit A.