TRADEMARK ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNS THE ENTIRE INTEREST AND THE GOODWILL

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
Innovative Silicon, Inc.		12/09/2010	CORPORATION: DELAWARE
Innovative Silicon ISi S.A.		12/09/2010	CORPORATION: SWITZERLAND

RECEIVING PARTY DATA

Name:	Micron Technology, Inc.
Street Address:	8000 S. Federal Way
City:	Boise
State/Country:	IDAHO
Postal Code:	83707
Entity Type:	CORPORATION: DELAWARE

PROPERTY NUMBERS Total: 1

Property Type	Number	Word Mark
Serial Number:	78490817	Z-RAM

CH $40.00 78490817

CORRESPONDENCE DATA

Fax Number: 8324462424
Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent via US Mail.
Email: wcpatent@counselip.com
Correspondent Name: Wong Cabello
Address Line 1: 20333 SH 249 Suite 600
Address Line 4: Houston, TEXAS 77070

ATTORNEY DOCKET NUMBER:	102-0068
NAME OF SUBMITTER:	John C. Cain
Signature:	/John C. Cain/
Date:	05/23/2012

Total Attachments: 49
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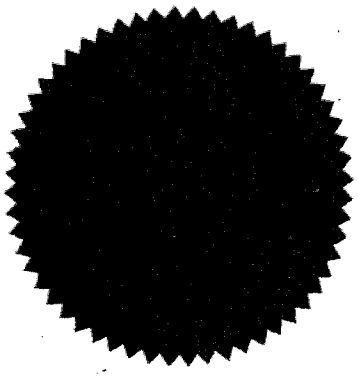
IN THE KINGDOM OF ENGLAND

TO ALL TO WHOM these presents shall come I **ADRIAN BRYAN PATRICK O'LOUGHLIN** of The Tunsgate 128 High Street Guildford Surrey England Notary Public by Royal Authority duly admitted and sworn **DO HEREBY CERTIFY** that on the day of the date hereof before me personally came and appeared **MARK ERIC JONES** holder of UK Passport No. 761311840 in my presence signed in due form of law the document annexed hereto

IN WITNESS whereof I the said Notary have subscribed my name and set and affixed my seal of Office this ninth day of December Two thousand and ten

Adria O'Laghl

ADRIAN BRYAN PATRICK O'LOUGHLIN
Notary Public



ASSIGNMENT OF REGISTERED INTELLECTUAL PROPERTY

This Assignment of Registered Intellectual Property effective as of December 9, 2010, (this "Assignment"), is made by Innovative Silicon, Inc., a Delaware corporation; Innovative Silicon ISi S.A. (collectively "Seller") in favor of Micron Technology, Inc., a Delaware corporation ("Buyer"). All capitalized words and terms used in this Assignment and not defined herein shall have the respective meanings ascribed to them in the Asset Purchase Agreement dated and effective December 9, 2010, by and between the Seller and the Buyer (the "Asset Purchase Agreement").

WHEREAS, pursuant to the Asset Purchase Agreement, the Seller has agreed to sell, transfer, convey, assign and deliver to the Buyer certain assets of the Seller, including all of the intellectual property assets of the Seller listed on Schedule A attached hereto; and

WHEREAS, in consideration therefor, the Asset Purchase Agreement requires that the Buyer pay, and Buyer has agreed to pay, the Purchase Price.

NOW, THEREFORE, in consideration of the mutual promises set forth in the Agreement and other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the Seller hereby agrees as follows:

1. Seller does hereby sell, assign, transfer, and convey to Buyer all of Seller's right, title and interest in and to all rights in Intellectual Property listed on Schedule A attached hereto (the "Intellectual Property Rights"). Seller conveys to the maximum extent provided under law, all of Seller's entire worldwide right, title and interest in, to, and under the rights arising from or related to the Intellectual Property Rights, the same to be held and enjoyed by Buyer for its own use and enjoyment and the use and enjoyment of its successors, assigns or other legal representatives, as fully and entirely as the same would have been held and enjoyed by Seller if this assignment and sale had not been made. The foregoing includes the assignment, transfer and conveyance of all causes of actions, claims, and demands or other rights for, or arising from, any infringement, including past infringement, all rights of priority under any international conventions and any other international agreements to which the United States adheres, all income, royalties, damages, claims, and payments now or hereafter due or payable with respect to the Intellectual Property Rights, and all rights corresponding thereto throughout the world. Seller hereby transfers all goodwill associated with any of the Intellectual Property Rights consisting of trademarks.

2. Seller hereby covenants and agrees that Seller will not execute any writing or do any act whatsoever conflicting with this Assignment, and that Seller will, at any time upon request, without further or additional consideration but at the expense of Buyer, execute such additional assignments and other writings and do such additional acts as Buyer, in its reasonable discretion, may deem necessary or desirable to perfect Buyer's enjoyment of this grant, and render reasonably necessary or desirable assistance in making application for and obtaining original, divisional, continuations, continuation-in-part, reexamined, reissued, or extended letters patent or of any and all foreign countries on said inventions, and in enforcing any rights or

causes of action accruing as a result of such applications or patents, by giving testimony in any proceedings or transactions involving such applications or patents, and/or by executing preliminary statements and other affidavits.

3. The Buyer and the Seller authorize and request that the Commissioner of Patents and Trademarks of the United States, and the corresponding entities or agencies in any applicable foreign countries, record Buyer as the owner of record for any of the Intellectual Property Rights consisting of patents or trademarks.

4. All disputes, claims or controversies arising out of this Assignment, or the negotiation, validity or performance of this Assignment, or the transactions contemplated hereby shall be governed by and construed in accordance with the laws of the State of Delaware, without giving effect to that State's principles governing conflicts of laws.

5. This Assignment shall be binding upon and inure to the benefit of the Buyer and the Seller and their respective successors and assigns.

6. If any provision of this Assignment or the application of any such provision to any person or circumstance shall be held invalid, illegal or unenforceable in any respect by a court of competent jurisdiction, such invalidity, illegality or unenforceability shall not affect any other provision hereof.

7. This Assignment may be executed in any number of counterparts, each of which when so executed and delivered shall be deemed an original, and such counterparts together shall constitute one and the same instrument.

[Remainder of Page Left Intentionally Blank]

IN WITNESS WHEREOF, the Buyer and the Seller have caused this instrument to be duly executed under seal as of and on the date first above written.

Seller:

Innovative Silicon, Inc.

By: _____
Name: MARK-ERIC JONES
Title: CEO

Innovative Silicon ISi S.A.

By: _____
Name: MARK-ERIC JONES
Title: CEO

ACCEPTED:

Buyer:

Micron Technology, Inc.

By: _____
Name:
Title:

STATE OF ENGLAND & WALES)
) SS.
COUNTY OF SURREY)

I, a notary public, in and for the county and state aforesaid, do hereby certify that MARK ERIC JONES appeared before me this day in person and acknowledged that he signed the above and foregoing instrument as his free and voluntary act for the uses and purposes therein set forth.

IN WITNESS WHEREOF, I have hereunto set my hand and notarial seal this 9th day of December, 2010

_____ Adrian Bryan Patrick O'Loughlin
Notary Public

My commission ~~expires on:~~ does not expire

IN WITNESS WHEREOF, the Buyer and the Seller have caused this instrument to be duly executed under seal as of and on the date first above written.

Seller:

Innovative Silicon, Inc.

By: _____
Name:
Title:

Innovative Silicon ISi S.A.

By: _____
Name:
Title:

ACCEPTED:

Buyer:

Micron Technology, Inc.

By: _____
Name: BRIAN SHIRLEY
Title: VP DRAM SOLUTIONS GROUP

REVIEWED
MTI LEGAL
KMD

STATE OF Idaho)
) SS.
COUNTY OF Ada)

I, a notary public, in and for the county and state aforesaid, do hereby certify that Brian Shirley appeared before me this day in person and acknowledged that he signed the above and foregoing instrument as his free and voluntary act for the uses and purposes therein set forth.

IN WITNESS WHEREOF, I have hereunto set my hand and notarial seal this 9th day of December, 2010.

Patty Baggenstos
Notary Public

My commission expires on: 5/22/2013

NOTARY PUBLIC STATE OF IDAHO

SCHEDULE A

REGISTERED INTELLECTUAL PROPERTY

Registered Intellectual Property

List of Patents

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
73885.000001		General Representation				TEA	
73885.000002	2008-001-US	Reduced Sourceline Swing	Eric Carman Ping Wang	12/244,183 Filed 10/2/2008		TEA DDD	Pending
73885.000003	2008-002-P	Floating Body Differential Amplifier Having Thyristor Sense And Block Refresh	Robert Murray	61/117,331 Filed 11/24/2008		TEA DDD	Abandoned per client request
73885.000004	2008-003-P	Source Line Plane	Betina Hold	61/153,437 Filed 2/18/2009	Parent of: 73885.000029	TEA DDD	Converted
73885.000005	2008-004-US	Ganged Source Lines	Eric Carman	12/251,944 Filed 10/15/2008		TEA DDD	Pending
73885.000006	2008-005-P	Method of Ultra Low Power Block Refresh	Vivek Nautiyal	61/111,658 Filed 11/5/2008		TEA DDD	Abandoned per client request
73885.000007	2008-006-P	Two Pass Block Refresh	Vivek Nautiyal Serguei Okhonin	61/111,665 Filed 11/5/2008	Parent of: 73885.000019	TEA DDD	Converted
73885.000008	2008-007	Charge Sharing Circuit to Generate VWLRD Voltage for Z-RAM Operation	Yogesh Luthra			TEA	Hold per client request
73885.000009	2009-001-P	Techniques For Forming Contact to Buried Layer in	Wayne Ellis John Kim	61/157,504	Parent of:	TEA	Converted

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		Semiconductor Memory Device		Filed 3/4/2009	73885.000027 73885.000032		
73885.000010	2009-002-P	Pseudo Pillar Memory Device and Method For Using Same	Mike Van Buskirk Christian Caillat Viktor Koldiaev J.T. Kwon Pierre Fazan	61/165,346 Filed 3/31/2009	Parent of: 73885.000028	TEA	Converted
73885.000011	2009-003-P	Techniques for Direct Injection of Charge Carriers	Yogesh Luthra Serguei Okhonin Mikhail Nagoga Srinivasa Banna Mike Van Buskirk Eric Carman Christian Caillat	61/173,014 Filed 4/27/2009	Parent of: 73885.000020 73885.000021 73885.000022	TEA	Converted
73885.000012	2009-004-US	Disturb Recovery Scheme for Floating Body Memory	Yogesh Luthra David Fisch	12/639,547 Filed 12/16/09		TEA DDD	Pending
73885.000013	2009-005-US	Z-RAM With Low and High Sensing Schemes With Incorporated Feedback	Betina Hold Robert Murray	12/718,310 Filed 3/5/2010		TEA DDD	Pending
73885.000014	2009-006-P	Direct Injection Z-RAM Cell Using SOI FinFET	Srinivasa Banna Mike Van Buskirk	61/180,810 Filed 5/22/2009	Parent of: 73885.000030	TEA	Converted
73885.000015	2009-007-P	Semiconductor Device (GAMED I)	Serguei Okhonin Viktor Koldiaev Mikhail Nagoga	61/224,741 Filed 7/10/2009	Parent of: 73885.000026	TEA	Converted
73885.000016	2009-009-P	Low Voltage Direct Injection Floating Body Memory Cell	Mike Van Buskirk Eric Carman	61/228,934	Parent of:	TEA	Converted

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
			Betina Hold Wayne Ellis Yogesh Luthra	Filed 7/27/2009	73885.000023 73885.000024 73885.000025		
73885.000017	2009-008-US	Techniques for Reducing Disturbance in a Semiconductor Memory Device	J.T. Kwon David Kim Sunil Bhardwaj	12/624,856 Filed 11/24/2009		TEA DDD	Pending
73885.000018	2009-010-P	Current Spike Sense Amplifier	Philippe Bruno Bauser Jean-Michel Daga	61/239,999 Filed 9/4/2009	Parent of: 73885.000064	TEA	Converted
73885.000019	2008-006-US	Two Pass Block Refresh	Vivek Nautiyal Serguei Okhonin	12/801,171 Filed 10/15/2009	Claims Priority to: 73885.000007	TEA DDD	Pending
73885.000020	2009-003-US1	Techniques for Direct Injection of Charge Carriers and Low Voltage Direct Injection Floating Body Memory Cell	Yogesh Luthra Serguei Okhonin Mikhail Nagoga	12/768,322 Filed 4/27/2010	Claims Priority to: 73885.000011	TEA DDD	Pending
73885.000021	2009-003-US2	Techniques for Direct Injection of Charge Carriers and Low Voltage Direct Injection Floating Body Memory Cell	Eric Carman	12/725,057 Filed 3/16/2010	Claims Priority to: 73885.000011	TEA DDD	Pending
73885.000022	2009-003-US3	Techniques for Direct Injection of Charge Carriers	Mike Van Buskirk Yogesh Luthra	12/768,363 Filed 4/27/2010	Claims Priority to: 73885.000011	TEA DDD	Pending

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		and Low Voltage Direct Injection Floating Body Memory Cell	Eric Carman				
73885.000023	2009-009-US1	Low Voltage Direct Injection Floating Body Memory Cell	Yogesh Luthra	12/843,212 Filed 7/26/2010	Claims Priority to: 73885.000016	TEA DDD	Pending
73885.000024	2009-009-US2	Low Voltage Direct Injection Floating Body Memory Cell	Eric Carman	12/697,780 Filed 2/1/2010	Claims Priority to: 73885.000016	TEA DDD	Pending
73885.000025	2009-009-US3	Low Voltage Direct Injection Floating Body Memory Cell	Mike Van Buskirk Betina Hold Wayne Ellis	12/844,477 Filed 7/27/2010	Claims Priority to: 73885.000016	TEA DDD	Pending
73885.000026	2009-007-US	Semiconductor Device (GAMED I & II)	Serguei Okhonin Viktor Koldiaev Mikhail Nagoga Yogesh Luthra	12/834,418 Filed 7/12/1010	Claims Priority to: 73885.000015 73885.000031	TEA	Pending
73885.000027	2009-001-US	Techniques For Forming Contact to Buried Layer in Semiconductor Memory Device	Wayne Ellis John Kim	12/717,776 Filed 3/4/2010	Claims Priority to: 73885.000009	TEA ERD	Pending
73885.000028	2009-002-US	Pseudo Pillar Memory Device and Method For Using Same	Mike Van Buskirk Christian Caillat Viktor Koldiaev J.T. Kwon Pierre Fazan	12/751,245 Filed 3/31/2010	Claims Priority to: 73885.000010	TEA	Pending
73885.000029	2008-003-US	Source Line Plane	Betina Hold	12/695,964 Filed 1/28/2010	Claims Priority to: 73885.000004	TEA DDD	Pending

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
73885.000030	2009-006-US	Direct Injection Z-RAM Cell Using SOI FinFET	Srinivasa Banna Mike Van Buskirk	12/785,971 Filed 5/24/2010	Claims Priority to: 73885.000014	TEA	Pending
73885.000031	2010-001-P	Semiconductor Device (GAMED II)	Serguei Okhonin Viktor Koldiaev Mikhail Nagoga Yogesh Luthra	61/314,532 Filed 3/16/2010	Parent of: 73885.000026	TEA	Converted (but still Pending until 3/16/2011)
73885.000032	2009-001-PCT	Techniques For Forming Contact to Buried Layer in Semiconductor Memory Device	Wayne Ellis John Kim	PCT/US2010/26209 Filed 3/4/2010	Claims Priority to: 73885.000009	TEA	Pending
73885.000033	2010-002-P	Read Circuitry for P-Stripe Z-RAM-LV Architecture	Jean-Michel Daga Eric Carman Philippe Bauser	61/304,067 Filed 2/12/2010	Parent of: 73885.000065	TEA	Pending Convert by 2/12/2011 Foreign Filing?
73885.000034	2010-003-P	Current Mode Sense Amplifier	Jean-Michel Daga	61/310,509 Filed 3/4/2010	Parent of: 73885.000066	TEA	Pending Convert by 3/4/2011 Foreign Filing?
73885.000035	2010-004-P	Hierarchical Bit Line (BL) With P-Stripe Architecture	Eric Carman	61/310,573 Filed 3/4/2010	Parent of: 73885.000067	TEA	Pending Convert by 3/4/2011 Foreign Filing?
73885.000036	2007-001-US (Formerly ISIL.P001)	Method and Apparatus for Variable Memory Cell Refresh	David Fisch Eric Carman	11/650,101 Filed 1/5/2007	Parent of: 73885.000037	RG	Patent Issued 11/17/2009 U.S. Patent No. 7,619,944
73885.000037	2007-001-PCT (Formerly ISIL.P001WO)	Method and Apparatus for Variable Memory Cell Refresh	David Fisch Eric Carman	PCT/US2007/88529 Filed 12/21/2007	Claims Priority to: 73885.000036	RG	Expired
73885.000038	2007-002-P (Formerly	Manufacturing Process for Zero-Capacitor Random	Pierre Fazan	60/921,151	Parent of:	RG	Converted

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
	ISIL.P002P)	Access Memory Circuits		Filed 3/29/2007	73885.000039 73885.000040		
73885.000039	2007-002-US Formerly ISIL.P002	Manufacturing Process for Zero-Capacitor Random Access Memory Circuits	Pierre Fazan	12/053,398 Filed 3/21/2008	Claims Priority to: 73885.000038	RG	Pending
73885.000040	2007-002-PCT (Formerly ISIL.P002WO)	Manufacturing Process for Zero-Capacitor Random Access Memory Circuits	Pierre Fazan	PCT/IB2008/03284 Filed 3/21/2008	Claims Priority to: 73885.000038	RG	Expired
73885.000041	2007-003-P (Formerly ISIL.P003P)	Semiconductor Device with Electrically Floating Body	Serguei Okhonin	60/897,686 Filed 1/26/2007	Parent of: 73885.000042 73885.000043	RG	Converted
73885.000042	2007-003-US (Formerly ISIL.P003)	Semiconductor Device with Electrically Floating Body	Serguei Okhonin	12/019,320 Filed 1/24/2008	Claims Priority to: 73885.000041	RG	Pending
73885.000043	2007-003-PCT (Formerly ISIL.P003WO)	Semiconductor Device with Electrically Floating Body	Serguei Okhonin	PCT/IB2008/00980 Filed 1/24/2008	Claims Priority to: 73885.000041 Parent of: 73885.000044	RG	Expired
73885.000044	2007-003-KR (Formerly ISIL.P003KR)	Semiconductor Device with Electrically Floating Body	Serguei Okhonin	10-2009-7017742 Filed 8/26/2009	Claims Priority to: 73885.000043	RG	Pending
73885.000045	2007-004-P (Formerly ISIL.P004P)	Reading Technique for Memory Cell with Electrically Floating Body Transistor	Serguei Okhonin Mikhail Nagoga Cedric Bassin	60/932,771 Filed 6/1/2007	Parent of: 73885.000046	RG	Converted

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
73885.000046	2007-004-US (Formerly ISIL.P004)	Reading Technique for Memory Cell with Electrically Floating Body Transistor	Serguei Okhonin Mikhail Nagoga Cedric Bassin	12/130,011 Filed 5/30/2008	Claims Priority to: 73885.000045	RG	Pending
73885.000047	2007-005-P (Formerly ISIL.P005P)	Refreshing Data of Memory Cells With Electrically Floating Body Transistors	Eric Carman Mikhail Nagoga Serguei Okhonin	60/973,139 Filed 9/17/2007	Parent of: 73885.000048 73885.000049	RG	Converted
73885.000048	2007-005-US (Formerly ISIL.P005)	Refreshing Data of Memory Cells With Electrically Floating Body Transistors	Eric Carman Mikhail Nagoga Serguei Okhonin	12/212,326 Filed 9/17/2008	Claims Priority to: 73885.000047	RG	Pending
73885.000049	2007-005-PCT (Formerly ISIL.P005WO)	Refreshing Data of Memory Cells With Electrically Floating Body Transistors	Eric Carman Mikhail Nagoga Serguei Okhonin	PCT/US2008/76666 Filed 9/17/2008	Claims Priority to: 73885.000047	RG	Expired
73885.000050	2008-008-P (Formerly ISIL.P006P)	Single Transistor Memory Cell	Serguei Okhonin Mikhail Nagoga	61/026,705 Filed 2/6/2008	Parent of: 73885.000051	RG	Converted
73885.000051	2008-008-US (Formerly ISIL.P006)	Single Transistor Memory Cell	Serguei Okhonin Mikhail Nagoga	12/367,154 Filed 2/6/2009	Claims Priority to: 73885.000050	RG	Pending
73885.000052	2008-009-P (Formerly ISIL.P007P)	Z-RAM Using Vertical Transistor Bit Cell	Eric Carman	61/120,173 Filed 12/5/2008	Parent of: 73885.000053	RG	Converted
73885.000053	2008-009-US (Formerly ISIL.P007)	Z-RAM Using Vertical Transistor Bit Cell	Eric Carman	12/632,394 Filed 12/7/2009	Claims Priority to: 73885.000052	RG	Pending
73885.000054	2008-010-P (Formerly	Recessed Gate Silicon-On-Insulator Floating Body	John Kim	61/100,040 Filed 9/25/2008	Parent of: 73885.000055	RG	Converted

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
	ISIL.P011P)	Device With Self-Aligned Lateral Isolation					
73885.000055	2008-010-US (Formerly ISIL.P011)	Recessed Gate Silicon-On-Insulator Floating Body Device With Self-Aligned Lateral Isolation	John Kim	12/567,202 Filed 9/25/2009	Claims Priority to: 73885.000054	RG	Pending
73885.000056	2009-011-P (Formerly ISIL.P012P)	Semiconductor Device with Floating Gate and Electrically Floating Body	Serguei Okhonin	61/174,075 Filed 4/30/2009	Parent of: 73885.000057	RG	Converted
73885.000057	2009-011-US (Formerly ISIL.P012)	Semiconductor Device with Floating Gate and Electrically Floating Body	Serguei Okhonin	12/770,249 Filed 4/29/2010	Claims Priority to: 73885.000057	TEA	Pending
73885.000058	2010-005-P	Junction-Less P-Stripe Cell	Srinivasa R. Banna Michael A. Van Buskirk Timothy Thurgate	61/313,986 Filed 3/15/2010	Parent of: 73885.000068	TEA	Pending Convert by 3/15/2011 Foreign Filing?
73885.000059	2009-002-PCT	Pseudo Pillar Memory Device and Method For Using Same	Mike Van Buskirk Christian Caillat Viktor Koldiaev J.T. Kwon Pierre Fazan	PCT/US2010/29380 Filed 3/31/2010	Claims Priority to: 73885.000010	TEA	Pending
73885.000060	2008-011 (Formerly ISIL.P008P)	1.5 Transistor Static RAM	Eric Carman			RG	Hold per client request
73885.000061	2008-012 (Formerly ISIL.P009P)	Z-RAM Memory Architecture Using DC Source Line	Eric Carman			RG	Hold per client request

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
73885.000062	2008-013 (Formerly ISIL.P010P)	Parallel Source Line Base Line Architecture	David Fisch			RG	Hold per client request
73885.000063	2010-006-P	Techniques for Semiconductor Memory Refresh	Eric Carman Yogesh Luthra	61/332,037 Filed 5/6/2010	Parent of: 73885.000069 73885.000070	TEA	Pending Convert by 5/6/2011 Foreign Filing?
73885.000064	2009-010-US	Current Spike Sense Amplifier	Philippe Bruno Bauser Jean-Michel Daga	12/877,044 Filed 9/7/2010	Claims Priority to: 73885.000018	TEA DDD	Pending
73885.000065	2010-002-US	Read Circuitry for P-Stripe Z-RAM-LV Architecture	Jean-Michel Daga Eric Carman Philippe Bauser		Claims Priority to: 73885.000033	TEA DDD	File by 2/12/2011 Foreign Filing?
73885.000066	2010-003-US	Current Mode Sense Amplifier	Jean-Michel Daga		Claims Priority to: 73885.000034	TEA DDD	File by 3/4/2011 Foreign Filing?
73885.000067	2010-004-US	Hierarchical Bit Line (BL) With P-Stripe Architecture	Eric Carman		Claims Priority to: 73885.000035	TEA DDD	File by 3/4/2011 Foreign Filing?
73885.000068	2010-005-US	Junction-Less P-Stripe Cell	Srinivasa R. Banna Michael A. Van Buskirk Timothy Thurgate		Claims Priority to: 73885.000058	TEA DDD	File by 3/15/2011 Foreign Filing?
73885.000069	2010-006-US1	Techniques for Semiconductor Memory Refresh	Eric Carman Yogesh Luthra		Claims Priority to: 73885.000063	TEA DDD	File by 5/6/2011 Foreign Filing?
73885.000070	2010-006-US2	Techniques for Semiconductor Memory Refresh	Eric Carman Yogesh Luthra		Claims Priority to: 73885.000063	TEA DDD	File by 5/6/2011 Foreign Filing?

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
73885.000071	2010-007-US	Highly Scalable Vertical NOR Flash Cell and Its Operation	Srinivasa R. Banna Michael A. Van Buskirk Timothy Thurgate			TEA	
73885.000072	2010-008-US	3D NAND String Structures and Their Operation	Srinivasa R. Banna Michael A. Van Buskirk Timothy Thurgate			TEA	
73885.001001	211.001-EP1	Semiconductor Device	Pierre Fazan Serguei Okhonin	EP 01810587.4 Filed 6/18/2001	Parent of: PCT/EP2002/06495 TW 91111316	NAS	Inactive
73885.001002	211.001-EP2	Semiconductor Device	Pierre Fazan Serguei Okhonin	EP 02405247.4 Filed 3/28/2002	Parent of: PCT/EP2002/06495 TW 91111316	NAS	Inactive
73885.001003	211.001-EP3	Semiconductor Device	Pierre Fazan Serguei Okhonin	EP 02405315.9 Filed 4/18/2002	Parent of: PCT/EP2002/06495 TW 91111316	NAS	Inactive
73885.001004	211.001-TW	Semiconductor Device	Pierre Fazan Serguei Okhonin	TW 91111316 Filed 5/28/2002	Claims Priority to: EP 01810587.4 EP 02405247.4 EP 02405315.9	NAS	Patent Issued 4/1/2005 TW Patent No. I230392
73885.001005	211.001-PCT	Semiconductor Device	Pierre Fazan Serguei Okhonin	PCT/EP2002/06495 Filed 6/5/2002	Claims Priority to: EP 01810587.4	NAS	Expired

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
					EP 02405247.4 EP 02405315.9 Parent of: 10/450,238 JP 505932 EP 02745383.6-1233		
73885.001006	211.001-EP4	Semiconductor Device	Pierre Fazan Serguei Okhonin	EP 02745383.6-1233 Filed 12/19/2003	Claims Priority to: PCT/EP2002/06495 Parent of: HK 04103533.4	NAS	Abandoned per client request
73885.001007	211.001-HK	Semiconductor Device	Pierre Fazan Serguei Okhonin	HK 04103533.4 Filed 5/19/2004	Claims Priority to: EP 02745383.6-1233	NAS	Abandoned per client request
73885.001008	211.001-JP	Semiconductor Device	Pierre Fazan Serguei Okhonin	JP 505932 Filed 6/5/2002	Claims Priority to: PCT/EP2002/06495	NAS	Abandoned per client request
73885.001009	211.001-US	Semiconductor Device	Pierre Fazan Serguei Okhonin	10/450,238 Filed 6/10/2003	Claims Priority to: PCT/EP2002/06495 Parent of: 11/201,483 11/132,979	NAS	Patent Issued 11/29/2005 U.S. Patent No. 6,969,662

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
					10/741,804 10/727,742 10/724,648 10/724,377 10/694,689		
73885.001010	211.001-D1	Semiconductor Device	Pierre Fazan Serguei Okhonin	10/694,689 Filed 10/28/2003	Divisional of: 10/450,238	NAS	Patent Issued 8/30/2005 U.S. Patent No. 6,937,516
73885.001011	211.001-D2	Semiconductor Device	Pierre Fazan Serguei Okhonin	10/724,377 Filed 11/28/2003	Divisional of: 10/450,238	NAS	Patent Issued 8/2/2005 U.S. Patent No. 6,925,006
73885.001012	211.001-D3	Semiconductor Device	Pierre Fazan Serguei Okhonin	10/724,648 Filed 12/1/2003	Divisional of: 10/450,238	NAS	Patent Issued 8/16/2005 U.S. Patent No. 6,930,918
73885.001013	211.001-D4	Semiconductor Device	Pierre Fazan Serguei Okhonin	10/727,742 Filed 12/4/2003	Divisional of: 10/450,238	NAS	Patent Issued 3/29/2005 U.S. Patent No. 6,873,539
73885.001014	211.001-D5	Semiconductor Device	Pierre Fazan Serguei Okhonin	10/741,804 Filed 12/19/2003	Divisional of: 10/450,238	NAS	Patent Issued 8/23/2005 U.S. Patent No. 6,934,186
73885.001015	211.001-D6	Semiconductor Device	Pierre Fazan Serguei Okhonin	11/132,979 Filed 5/19/2005	Divisional of: 10/450,238	NAS	Patent Issued 7/3/2007 U.S. Patent No. 7,239,549
73885.001016	211.001-D7	Semiconductor Device	Pierre Fazan Serguei Okhonin	11/201,483 Filed 8/11/2005	Divisional of: 10/450,238 Parent of: 11/904,978	NAS	Patent Issued 10/9/2007 U.S. Patent No. 7,280,399

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
					11/904,977		
73885.001017	211.001-D8	Semiconductor Device	Pierre Fazan Serguei Okhonin	11/904,978 Filed 9/28/2007	Divisional of: 11/201,483	NAS	Abandoned per client request
73885.001018	211.001-D9	Semiconductor Device	Pierre Fazan Serguei Okhonin	11/904,977 Filed 9/28/2007	Divisional of: 11/201,483 Parent of: 11/977,705 11/975,862	NAS	Abandoned per client request
73885.001019	211.001-D10	Semiconductor Device	Pierre Fazan Serguei Okhonin	11/975,862 Filed 10/22/2007	Divisional of: 11/904,977	NAS	Patent Issued 6/2/2009 U.S. Patent No. 7,541,616
73885.001020	211.001-D11	Semiconductor Device	Pierre Fazan Serguei Okhonin	11/977,705 Filed 10/25/2007	Divisional of: 11/904,977	NAS	Patent Issued 6/8/2010 U.S. Patent No. 7,732,816
73885.001021	211.002-CN	Data Storage Device and Refreshing Method for Use with Such Device	Pierre Fazan Serguei Okhonin	CN 03808739.1 Filed 10/18/2004	Claims Priority to: PCT/EP2003/02747	NAS	Patent Issued 3/4/2009 CN Patent No. ZL2003808739.1
73885.001022	211.002-EP1	Data Storage Device and Refreshing Method for Use with Such Device	Pierre Fazan Serguei Okhonin	EP 02405314.2 Filed 4/18/2002	Parent of: PCT/EP2003/02747	NAS	Abandoned per client request
73885.001023	211.002-EP2	Data Storage Device and Refreshing Method for Use with Such Device	Pierre Fazan Serguei Okhonin	EP 02077116.8 Filed 5/29/2002	Parent of: PCT/EP2003/02747 DE 02077116.8 UK 02077116.8	NAS	Patent Issued 2/21/2007 EP Patent No. 1355316

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
73885.001024	211.002-DE	Data Storage Device and Refreshing Method for Use with Such Device	Pierre Fazan Serguei Okhonin	DE 02077116.8 Filed 5/29/2002	Claims Priority to: EP 02077116.8	NAS	Patent Issued 2/21/2007 DE Patent No. 60218283.2-08
73885.001025	211.002-GB	Data Storage Device and Refreshing Method for Use with Such Device	Pierre Fazan Serguei Okhonin	UK 02077116.8 Filed 5/29/2002	Claims Priority to: EP 02077116.8	NAS	Patent Issued 2/21/2007 UK Patent No. 1355316
73885.001026	211.002-PCT	Data Storage Device and Refreshing Method for Use with Such Device	Pierre Fazan Serguei Okhonin	PCT/EP2003/02747 Filed 3/17/2003	Claims Priority to: EP 02405314.2 EP 02077116.8 Parent of: 10/487,162 CN 03808739.1	NAS	Expired
73885.001027	211.002-US	Data Storage Device and Refreshing Method for Use with Such Device	Pierre Fazan Serguei Okhonin	10/487,162 Filed 2/17/2004	Claims Priority to: PCT/EP2003/02747 Parent of: 11/048,387	NAS	Patent Issued 1/3/2006 U.S. Patent No. 6,982,918
73885.001028	211.002-D1	Data Storage Device and Refreshing Method for Use with Such Device	Pierre Fazan Serguei Okhonin	11/048,387 Filed 2/1/2005	Divisional of: 10/487,162 Parent of:	NAS	Patent Issued 1/30/2007 U.S. Patent No. 7,170,807

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
					11/649,945		
73885.001029	211.002-D2	Data Storage Device and Refreshing Method for Use with Such Device	Pierre Fazan Serguei Okhonin	11/649,945 Filed 1/5/2007	Divisional of: 11/048,387	NAS	Patent Issued 3/11/2008 U.S. Patent No. 7,342,842
73885.001030	211.003-EP1	Semiconductor Device	Pierre Fazan Serguei Okhonin	EP 02405316.7 Filed 4/18/2002	Parent of: PCT/EP2003/02748	NAS	Abandoned per client request
73885.001031	211.003-EP2	Semiconductor Device	Pierre Fazan Serguei Okhonin	EP 02078585.3 Filed 8/27/2002	Parent of: PCT/EP2003/02748	NAS	Abandoned per client request
73885.001032	211.003-PCT	Semiconductor Device	Pierre Fazan Serguei Okhonin	PCT/EP2003/02748 Filed 3/17/2003	Claims Priority to: EP 02405316.7 EP 02078585.3 Parent of: 10/487,157 CN 03808738.3	NAS	Expired
73885.001033	211.003-CN	Semiconductor Device	Pierre Fazan Serguei Okhonin	CN 03808738.3 Filed 10/18/2004	Claims Priority to: PCT/EP2003/02748	NAS	Abandoned per client request
73885.001034	211.003-US	Semiconductor Device	Pierre Fazan Serguei Okhonin	10/487,157 Filed 2/18/2004	Claims Priority to: PCT/EP2003/02748 Parent of: 11/226,978	NAS	Patent Issued 6/13/2006 U.S. Patent No. 7,061,050
73885.001035	211.003-D1	Semiconductor Device	Pierre Fazan	11/226,978	Divisional of:	NAS	Patent Issued 4/7/2009

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
			Serguei Okhonin	Filed 9/15/2005	10/487,157		U.S. Patent No. 7,514,748
73885.001036	211.004-P1	Semiconductor Memory Device and Method of Operating Same	Richard Ferrant Serguei Okhonin Pierre Fazan Michel Bron	60/470,384 Filed 5/13/2003	Parent of: 10/840,009	NAS	Converted
73885.001037	211.004-P2	Semiconductor Memory Device and Method of Operating Same	Richard Ferrant Serguei Okhonin Pierre Fazan Michel Bron	60/470,318 Filed 5/13/2003	Parent of: 10/840,009	NAS	Converted
73885.001038	211.004-PCT	Semiconductor Memory Device and Method of Operating Same	Richard Ferrant Serguei Okhonin Pierre Fazan Michel Bron	PCT/US2004/14691 Filed 5/11/2004	Claims Priority to: 60/470,384 60/470,318 Parent of: CN 200480001678.6 EP 04760984.7 JP 532947/2006	NAS	Expired
73885.001039	211.004-CN	Semiconductor Memory Device and Method of Operating Same	Richard Ferrant Serguei Okhonin Pierre Fazan Michel Bron	CN 200480001678.6 Filed 6/24/2005	Claims Priority to: PCT/US2004/14691	NAS	Patent Issued 7/22/2009 CN Patent No. ZL200480001678.6
73885.001040	211.004-EP	Semiconductor Memory Device and Method of Operating Same	Richard Ferrant Serguei Okhonin Pierre Fazan Michel Bron	EP 04760984.7 Filed 5/11/2004	Claims Priority to: PCT/US2004/14691	NAS	Abandoned per client request

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
73885.001041	211.004-JP	Semiconductor Memory Device and Method of Operating Same	Richard Ferrant Serguei Okhonin Pierre Fazan Michel Bron	JP 532947/2006 Filed 8/22/2005	Claims Priority to: PCT/US2004/14691	NAS	Pending
73885.001042	211.004-US	Semiconductor Memory Device and Method of Operating Same	Richard Ferrant Serguei Okhonin Pierre Fazan Michel Bron	10/840,009 Filed 5/6/2004	Claims Priority to: 60/470,384 60/470,318 Parent of: 11/079,590 11/096,970	NAS	Abandoned per client request
73885.001043	211.004-D1	Semiconductor Memory Device and Method of Operating Same	Richard Ferrant Serguei Okhonin Pierre Fazan Michel Bron	11/079,590 Filed 3/14/2005	Divisional of: 10/840,009	NAS	Patent Issued 03/06/2007 U.S. Patent No. 7,187,581
73885.001044	211.004-D2	Semiconductor Memory Device and Method of Operating Same	Richard Ferrant Serguei Okhonin Pierre Fazan Michel Bron	11/096,970 Filed 4/1/2005	Divisional of: 10/840,009	NAS	Patent Issued 08/01/2006 U.S. Patent No. 7,085,156
73885.001045	211.004-D3	Semiconductor Memory Device and Method of Operating Same	Richard Ferrant Serguei Okhonin Pierre Fazan Michel Bron	11/713,284 Filed 3/2/2007	Divisional of: 11/079,590	NAS	Patent Issued 4/15/2008 U.S. Patent No. 7,359,229
73885.001046	211.004-D4	Semiconductor Memory Device and Method of Operating Same	Richard Ferrant Serguei Okhonin Pierre Fazan	12/082,020 Filed 4/8/2008	Divisional of: 11/713,284	NAS	Patent Issued 6/8/2010 U.S. Patent No. 7,733,693

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
			Michel Bron				
73885.001047	211.005-P	Semiconductor Memory Cell, Array, Architecture and Device, and Method of Operating Same	Richard Ferrant Serguei Okhonin Eric Carman Michel Bron	60/470,385 Filed 5/13/2003	Parent of: 10/829,877 PCT/US2004/14363	NAS	Converted
73885.001048	211.005-PCT	Semiconductor Memory Cell, Array, Architecture and Device, and Method of Operating Same	Richard Ferrant Serguei Okhonin Eric Carman Michel Bron	PCT/US2004/14363 Filed 5/7/2004	Claims Priority to: 60/470,385 Parent of: JP 532866/2006 EP 04751661.2 CN 200480001693.0	NAS	Expired
73885.001049	211.005-CN	Semiconductor Memory Cell, Array, Architecture and Device, and Method of Operating Same	Richard Ferrant Serguei Okhonin Eric Carman Michel Bron	CN 200480001693.0 Filed 6/24/2005	Claims Priority to: PCT/US2004/14363	NAS	Patent Issued 7/29/2009 CN Patent No. ZL200480001693.0
73885.001050	211.005-EP	Semiconductor Memory Cell, Array, Architecture and Device, and Method of Operating Same	Richard Ferrant Serguei Okhonin Eric Carman Michel Bron	EP 04751661.2 Filed 5/7/2004	Claims Priority to: PCT/US2004/14363	NAS	Abandoned per client request
73885.001051	211.005-JP	Semiconductor Memory Cell, Array, Architecture and Device, and Method of Operating Same	Richard Ferrant Serguei Okhonin Eric Carman Michel Bron	JP 532866/2006 Filed 9/5/2005	Claims Priority to: PCT/US2004/14363	NAS	Abandoned per client request
73885.001052	211.005-US	Semiconductor Memory Cell, Array, Architecture and	Richard Ferrant Serguei Okhonin	10/829,877	Claims Priority to:	NAS	Patent Issued 08/01/2006 U.S. Patent No. 7,085,153

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		Device, and Method of Operating Same	Eric Carman Michel Bron	Filed 4/22/2004	60/470,385		
73885.001053	211.006-P1	Reference Current Generator, and Method of Programming, Adjusting and/or Operating Same	Lionel Portmann Maher Kayal Marc Pastre Marija Blagojevic Michel Declercq	60/470,462 Filed 5/13/2003	Parent of: 10/840,902 PCT/US2004/14843	NAS	Converted
73885.001054	211.006-P2	Reference Current Generator, and Method of Programming, Adjusting and/or Operating Same	Lionel Portmann Maher Kayal Marc Pastre Marija Blagojevic Michel Declercq	60/470,276 Filed 5/14/2003	Parent of: 10/840,902 PCT/US2004/14843	NAS	Converted
73885.001055	211.006-PCT	Reference Current Generator, and Method of Programming, Adjusting and/or Operating Same	Lionel Portmann Maher Kayal Marc Pastre Marija Blagojevic Michel Declercq	PCT/US2004/14843 Filed 05/12/2004	Claims Priority to: 60/470,462 60/470,276 Parent of: EP 04751987.1 DE 04751987.1 UK 04751987.1	NAS	Expired
73885.001056	211.006-EP	Reference Current Generator, and Method of Programming, Adjusting and/or Operating Same	Lionel Portmann Maher Kayal Marc Pastre Marija Blagojevic Michel Declercq	EP 04751987.1 Filed 05/12/2004	Claims Priority to: PCT/US2004/14843	NAS	Patent Issued 06/04/2008 EP Patent No. EP1620859B1

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
73885.001057	211.006-DE	Reference Current Generator, and Method of Programming, Adjusting and/or Operating Same	Lionel Portmann Maher Kayal Marc Pastre Marija Blagojevic Michel Declercq	DE 04751987.1 Filed 05/12/2004	Claims Priority to: PCT/US2004/14843	NAS	Patent Issued 06/04/2008 DE Patent No. 602004014269.7-08
73885.001058	211.006-GB	Reference Current Generator, and Method of Programming, Adjusting and/or Operating Same	Lionel Portmann Maher Kayal Marc Pastre Marija Blagojevic Michel Declercq	UK 04751987.1 Filed 5/12/2004	Claims Priority to: PCT/US2004/14843	NAS	Patent Issued 06/04/2008 UK Patent No. 1620859
73885.001059	211.006-US	Reference Current Generator, and Method of Programming, Adjusting and/or Operating Same	Lionel Portmann Maher Kayal Marc Pastre Marija Blagojevic Michel Declercq	10/840,902 Filed 5/07/2004	Claims Priority to: 60/470,462 60/470,276 Parent of: 11/061,069	NAS	Patent Issued 06/28/2005 U.S. Patent No. 6,912,150
73885.001060	211.006-D1	Reference Current Generator, and Method of Programming, Adjusting and/or Operating Same	Lionel Portmann Maher Kayal Marc Pastre Marija Blagojevic Michel Declercq	11/061,069 Filed 2/18/2005	Divisional of: 10/840,902	NAS	Patent Issued 12/27/2005 U.S. Patent No. 6,980,461
73885.001061	211.007-P	Integrated Circuit Device, and Method of Fabricating Same	Pierre Fazan	60/489,266 Filed 7/22/2003	Parent of: 10/884,481 PCT/IB2004/002702	NAS	Converted
73885.001062	211.007-PCT	Integrated Circuit Device, and	Pierre Fazan	PCT/IB2004/002702	Claims Priority to:	NAS	Expired

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		Method of Fabricating Same		Filed 7/21/2004	60/489,266		
73885.001063	211.007-US	Integrated Circuit Device, and Method of Fabricating Same	Pierre Fazan	10/884,481 Filed 7/2/2004	Claims Priority to: 60/489,266 Parent of: 12/069,704	NAS	Patent Issued 2/26/2008 U.S. Patent No. 7,335,934
73885.001064	211.007-D1	Integrated Circuit Device, and Method of Fabricating Same	Pierre Fazan	12/069,704 Filed 2/12/2008	Divisional of: 10/884,481	NAS	Patent Issued 6/15/2010 U.S. Patent No. 7,736,959
73885.001065	211.008-P	Low Power Programming Technique for a One Transistor SOI Memory Device	Pierre Fazan Serguei Okhonin	60/505,679 Filed 9/24/2003	Parent of: 10/941,692 PCT/IB2004/003721	NAS	Converted
73885.001066	211.008-PCT	Low Power Programming Technique for a Floating Body Memory Transistor, Memory Cell, and Memory Array	Pierre Fazan Serguei Okhonin	PCT/IB2004/003721 Filed 9/23/2004	Claims Priority to: 60/505,679 Parent of: EP 04787565.3 DE 04787565.3 UK 04787565.3	NAS	Expired
73885.001067	211.008-EP	Low Power Programming Technique for a Floating Body Memory Transistor, Memory Cell, and Memory Array	Pierre Fazan Serguei Okhonin	EP 04787565.3 Filed 9/23/2004	Claims Priority to: PCT/IB2004/003721	NAS	Patent Issued 7/11/2007 EP Patent No. 1671331
73885.001068	211.008-DE	Low Power Programming	Pierre Fazan	DE 04787565.3	Claims Priority to:	NAS	Patent Issued 7/11/2007

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		Technique for a Floating Body Memory Transistor, Memory Cell, and Memory Array	Serguei Okhonin	Filed 9/23/2004	PCT/IB2004/003721		DE Patent No. 602004007536
73885.001069	211.008-GB	Low Power Programming Technique for a Floating Body Memory Transistor, Memory Cell, and Memory Array	Pierre Fazan Serguei Okhonin	UK 04787565.3 Filed 9/23/2004	Claims Priority to: PCT/IB2004/003721	NAS	Patent Issued 7/11/2007 UK Patent No. 1671331
73885.001070	211.008-US	Low Power Programming Technique for a Floating Body Memory Transistor, Memory Cell, and Memory Array	Pierre Fazan Serguei Okhonin	10/941,692 Filed 9/15/2004	Claims Priority to: 60/505,679 Parent of: 11/334,338	NAS	Patent Issued 2/27/2007 U.S. Patent No. 7,184,298
73885.001071	211.008-D1	Low Power Programming Technique for a Floating Body Memory Transistor, Memory Cell, and Memory Array	Pierre Fazan Serguei Okhonin	11/334,338 Filed 1/17/2006	Divisional of: 10/941,692	NAS	Patent Issued 2/13/2007 U.S. Patent No. 7,177,175
73885.001072	211.009-P	Programming Technique for a Memory Cell Having an Electrically Floating Body Transistor	Serguei Okhonin Mikhail Nagoga	60/625,248 Filed 11/4/2004	Parent of: 11/247,727	NAS	Converted
73885.001073	211.009-US	Memory Cell Having an Electrically Floating Body Transistor and Programming Technique Therefor	Serguei Okhonin Mikhail Nagoga	11/247,727 Filed 10/11/2005	Claims Priority to: 60/625,248	NAS	Patent Issued 1/13/2009 U.S. Patent No. 7,476,939
73885.001074	211.010-P	Method of Implementing Statistical Distribution of IC	Serguei Okhonin Mikhail Nagoga	60/626,745 Filed 11/10/2004	Parent of: 11/247,774	NAS	Converted

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		and IC Device Implementing Same					
73885.001075	211.010-US	Circuitry for and Method of Improving Statistical Distribution of Integrated Circuits	Serguei Okhonin Mikhail Nagoga	11/247,774 Filed 10/11/2005	Claims Priority to: 60/626,745	NAS	Patent Issued 7/31/2007 U.S. Patent No. 7,251,164
73885.001076	211.011-P	Sense Amplifier Circuitry and Architecture to Write Data into and/or Read from Memory Cells	William K. Waller Eric Carman	60/635,709 Filed 12/13/2004	Parent of: 11/299,590 PCT/US2005/44791	NAS	Converted
73885.001077	211.011-PCT	Sense Amplifier Circuitry and Architecture to Write Data into and/or Read from Memory Cells	William K. Waller Eric Carman	PCT/US2005/44791 Filed 12/12/2005	Claims Priority to: 60/635,709	NAS	Expired
73885.001078	211.011-US	Sense Amplifier Circuitry and Architecture to Write Data into and/or Read from Memory Cells	William K. Waller Eric Carman	11/299,590 Filed 12/12/2005	Claims Priority to: 60/635,709 Parent of: 11/982,807	NAS	Patent Issued 11/27/2007 U.S. Patent No. 7,301,838
73885.001079	211.011-D1	Sense Amplifier Circuitry and Architecture to Write Data into and/or Read from Memory Cells	William K. Waller Eric Carman	11/982,807 Filed 11/5/2007	Divisional of: 11/299,590	NAS	Patent Issued 2/3/2009 U.S. Patent No. 7,486,563
73885.001080	211.012-P	Bipolar Reading Technique for a Memory Cell Having an Electrically Floating Body	Serguei Okhonin Mikhail Nagoga	60/638,663 Filed 12/22/2004	Parent of: 11/304,387	NAS	Converted

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		Transistor			PCT/EP2005/013755		
73885.001081	211.012-PCT	Bipolar Reading Technique for a Memory Cell Having an Electrically Floating Body Transistor	Serguei Okhonin Mikhail Nagoga	PCT/EP2005/013755 Filed 12/21/2005	Claims Priority to: 60/638,663 Parent of: EP 05850314.5 KR 2007-7014246	NAS	Expired
73885.001082	211.012-EP	Bipolar Reading Technique for a Memory Cell Having an Electrically Floating Body Transistor	Serguei Okhonin Mikhail Nagoga	EP 05850314.5 Filed 12/21/2005	Claims Priority to: PCT/EP2005/013755	NAS	Abandoned per client request
73885.001083	211.012-KR	Bipolar Reading Technique for a Memory Cell Having an Electrically Floating Body Transistor	Serguei Okhonin Mikhail Nagoga	KR 2007-7014246 Filed 6/22/2007	Claims Priority to: PCT/EP2005/013755	NAS	Pending
73885.001084	211.012-US	Bipolar Reading Technique for a Memory Cell Having an Electrically Floating Body Transistor	Serguei Okhonin Mikhail Nagoga	11/304,387 Filed 12/15/2005	Claims Priority to: 60/638,663 Parent of: 11/906,036	NAS	Patent Issued 11/27/2007 U.S. Patent No. 7,301,803
73885.001085	211.012-D1	Bipolar Reading Technique for a Memory Cell Having an Electrically Floating Body Transistor	Serguei Okhonin Mikhail Nagoga	11/906,036 Filed 9/28/2007	Divisional of: 11/304,387	NAS	Patent Issued 1/13/2009 U.S. Patent No. 7,477,540

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
73885.001086	211.013-P	Method for Reading a Memory Cell Having an Electrically Floating Body Transistor and Array Having Same, and Memory Cell and Array Implementing Same	Serguei Okhonin Mikhail Nagoga	60/703,142 Filed 7/28/2005	Parent of: 11/453,594	NAS	Converted
73885.001087	211.013-US	Method for Reading a Memory Cell Having an Electrically Floating Body Transistor and Array Having Same, and Memory Cell and Array Implementing Same	Serguei Okhonin Mikhail Nagoga	11/453,594 Filed 6/15/2006	Claims Priority to: 60/703,142	NAS	Abandoned per client request
73885.001088	211.014-P1	Memory Cell and Memory Cell Array Having an Electrically Floating Body Transistor, and Methods of Operating Same	Serguei Okhonin	60/714,917 Filed 9/7/2005	Parent of: 11/509,188 PCT/EP2006/008668	NAS	Converted
73885.001089	211.014-P2	Semiconductor Memory Cell and Array using Bipolar Transistor Current to Program Same	Serguei Okhonin Mikhail Nagoga	60/722,139 Filed 9/30/2005	Parent of: 11/509,188 PCT/EP2006/008668	NAS	Converted
73885.001090	211.014-P3	Semiconductor Memory Device and Method of Operating Same	Serguei Okhonin Mikhail Nagoga	60/728,061 Filed 10/19/2005	Parent of: 11/509,188 PCT/EP2006/008668	NAS	Converted
73885.001091	211.014-P4	Semiconductor Memory Cell and Array using Bipolar	Serguei Okhonin Mikhail Nagoga	60/749,385 Filed 12/12/2005	Parent of: 11/509,188	NAS	Converted

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		Transistor Currents to Program and Read Same			PCT/EP2006/008668		
73885.001092	211.014-P5	Multilevel Memory Cell and Method for Programming and Reading Same	Serguei Okhonin Mikhail Nagoga	60/774,275 Filed 2/16/2006	Parent of: 11/509,188 PCT/EP2006/008668	NAS	Converted
73885.001093	211.014-PCT	Memory Cell and Memory Cell Array Having an Electrically Floating Body Transistor, and Methods of Operating Same	Serguei Okhonin	PCT/EP2006/008668 Filed 9/6/2006	Claims Priority to: 60/714,917 60/722,139 60/728,061 60/749,385 60/774,275 Parent of: CN 2006 8002 6285.X EP 06777170.9 JP 529531/2008 KR 2008-7006459	NAS	Expired
73885.001094	211.014-CN	Memory Cell and Memory Cell Array Having an Electrically Floating Body Transistor, and Methods of Operating Same	Serguei Okhonin	CN 2006 8002 6285.X Filed 9/6/2006	Claims Priority to: PCT/EP2006/008668	NAS	Patent Issued 9/1/2010 CN Patent No. ZL200680026285.X
73885.001095	211.014-EP	Memory Cell and Memory Cell Array Having an	Serguei Okhonin	EP 06777170.9 Filed 9/6/2006	Claims Priority to: PCT/EP2006/008668	NAS	Abandoned per client request

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		Electrically Floating Body Transistor, and Methods of Operating Same					
73885.001096	211.014-JP	Memory Cell and Memory Cell Array Having an Electrically Floating Body Transistor, and Methods of Operating Same	Serguei Okhonin	JP 529531/2008 Filed 9/6/2006	Claims Priority to: PCT/EP2006/008668	NAS	Pending
73885.001097	211.014-KR	Memory Cell and Memory Cell Array Having an Electrically Floating Body Transistor, and Methods of Operating Same	Serguei Okhonin	KR 2008-7006459 Filed 9/6/2006	Claims Priority to: PCT/EP2006/008668	NAS	Pending
73885.001098	211.014-US	Memory Cell and Memory Cell Array Having an Electrically Floating Body Transistor, and Methods of Operating Same	Serguei Okhonin	11/509,188 Filed 8/24/2006	Claims Priority to: 60/714,917 60/722,139 60/728,061 60/749,385 60/774,275 Parent of: 12/573,203	NAS	Patent Issued 10/20/2009 U.S. Patent No. 7,606,066
73885.001099	211.014-D1	Memory Cell and Memory Cell Array Having an Electrically Floating Body	Serguei Okhonin	12/573,203 Filed 10/5/2009	Continuation of: 11/509,188	NAS	Pending

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		Transistor, and Methods of Operating Same					
73885.001100	211.015-P	Method and Circuitry to Generate a Reference Current for Reading a Memory Cell, and Device Implementing Same	Philippe Bauser	60/718,417 Filed 9/19/2005	Parent of: 11/515,667 PCT/EP2006/009070	NAS	Converted
73885.001101	211.015-PCT	Method and Circuitry to Generate a Reference Current for Reading a Memory Cell, and Device Implementing Same	Philippe Bauser	PCT/EP2006/009070 Filed 9/16/2006	Claims Priority to: 60/718,417 Parent of: EP 06805759.5	NAS	Expired
73885.001102	211.015-EP	Method and Circuitry to Generate a Reference Current for Reading a Memory Cell, and Device Implementing Same	Philippe Bauser	EP 06805759.5 Filed 9/19/2006	Claims Priority to: PCT/EP2006/009070	NAS	Patent Issued 7/3/2009 EP Patent No. 1927111
73885.001103	211.015-DE	Method and Circuitry to Generate a Reference Current for Reading a Memory Cell, and Device Implementing Same	Philippe Bauser	DE 06805759.5 Filed 9/19/2006	Claims Priority to: PCT/EP2006/009070	NAS	Patent Issued 7/3/2009 DE Patent No. 602006007155.8
73885.001104	211.015-US	Method and Circuitry to Generate a Reference Current for Reading a Memory Cell, and Device Implementing	Philippe Bauser	11/515,667 Filed 9/5/2006	Claims Priority to: 60/718,417	NAS	Patent Issued 4/8/2008 U.S. Patent No. 7,355,916

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		Same			Parent of: 12/070,499		
73885.001105	211.015-D1	Method and Circuitry to Generate a Reference Current for Reading a Memory Cell, and Device Implementing Same	Philippe Bauser	12/070,499 Filed 2/19/2008	Divisional of: 11/515,667	NAS	Patent Issued 3/3/2009 U.S. Patent No. 7,499,358
73885.001106	211.016-P	One Transistor Memory Having a Mechanically Strained electrically Floating Body Region, and Method of Operating Same	Cédric Bassin	60/728,060 Filed 10/19/2005	Parent of: 11/580,169	NAS	Converted
73885.001107	211.016-US	One Transistor Memory Having A Strained Electrically Floating Body Region, and Method of Operating Same	Cédric Bassin	11/580,169 Filed 10/12/2006	Claims Priority to: 60/728,060	NAS	Abandoned per client request
73885.001108	211.017-P1	Method and Apparatus for Varying the Programming Duration of a Floating Body Transistor, and Memory Cell, Array, and/or Device Implementing Same	Gregory A. Popoff Paul de Champs Hamid Daghighian	60/731,668 Filed 10/31/2005	Parent of: 11/590,147 PCT/EP2006/067968	NAS	Converted
73885.001109	211.017-P2	Method and Apparatus for Varying the Programming Duration of a Floating Body Transistor, and Memory Cell, Array, and/or Device	Gregory A. Popoff	60/736,613 Filed 11/14/2005	Parent of: 11/590,147 PCT/EP2006/067968	NAS	Converted

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		Implementing Same					
73885.001110	211.017-PCT	Method and Apparatus for Varying the Programming Duration of a Floating Body Transistor, and Memory Cell, Array, and/or Device Implementing Same	Gregory A. Popoff Paul de Champ Hamid Daghighian	PCT/EP2006/067968 Filed 10/31/2006	Claims Priority to: 60/731,668 60/736,613 Parent of: CN 2006 8002 6259.7	NAS	Expired
73885.001111	211.017-CN	Method and Apparatus for Varying the Programming Duration of a Floating Body Transistor, and Memory Cell, Array, and/or Device Implementing Same	Gregory A. Popoff Paul de Champ Hamid Daghighian	CN 2006 8002 6259.7 Filed 10/31/2006	Claims Priority to: PCT/EP2006/067968	NAS	Pending
73885.001112	211.017-US	Method and Apparatus for Varying the Programming Duration of a Floating Body Transistor, and Memory Cell, Array, and/or Device Implementing Same	Gregory A. Popoff Paul de Champs Hamid Daghighian	11/590,147 Filed 10/31/2006	Claims Priority to: 60/731,668 60/736,613	NAS	Patent Issued 10/14/2008 U.S. Patent No. 7,436,706
73885.001113	211.017-D1	Method and Apparatus for Varying the Programming Duration of a Floating Body Transistor, and Memory Cell, Array, and/or Device Implementing Same	Gregory A. Popoff Paul de Champs Hamid Daghighian	12/284,961 Filed 9/26/2008		NAS	Patent Issued 10/13/2009 U.S. Patent No. 7,602,645
73885.001114	211.018-P	Floating Body Memory Cell	Serguei Okhonin	60/751,505	Parent of:	NAS	Converted

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		and Array, and Method of Operating or Controlling Same		Filed 12/19/2005	11/633,311		
73885.001115	211.018-US	Electrically Floating Body Memory Cell and Array, and Method of Operating or Controlling Same	Serguei Okhonin	11/633,311 Filed 12/4/2006	Claims Priority to: 60/751,505	NAS	Patent Issued 3/23/2010 U.S. Patent No. 7,683,430
73885.001116	211.019-P	Multilevel Memory Cell and Method for Programming and Reading Same	Serguei Okhonin Erik Carman Mark-Eric Jones	60/774,275 Filed 2/16/2006	Parent of: 11/703,429 PCT/US2007/04163	NAS	Converted
73885.001117	211.019-PCT	Multi-Bit Memory Cell Having Electrically Floating Body Transistor, and Method of Programming and Reading Same	Serguei Okhonin Eric Carman Mark-Eric Jones	PCT/US2007/04163 Filed 2/15/2007	Claims Priority to: 60/774,275 Parent of: EP 07750961.0	NAS	Expired
73885.001118	211.019-EP	Multi-Bit Memory Cell Having Electrically Floating Body Transistor, and Method of Programming and Reading Same	Serguei Okhonin Eric Carman Mark-Eric Jones	EP 07750961.0 Filed 2/15/2007	Claims Priority to: PCT/US2007/04163	NAS	Abandoned per client request
73885.001119	211.019-US	Multi-Bit Memory Cell Having Electrically Floating Body Transistor, and Method of Programming and Reading Same	Serguei Okhonin Eric Carman Mark-Eric Jones	11/703,429 Filed 2/7/2007	Claims Priority to: 60/774,275	NAS	Patent Issued 6/2/2009 U.S. Patent No. 7,542,345
73885.001120	211.020-P	Memory Array Having a	Eric Carman	60/790,111	Parent of:	NAS	Converted

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		Programmable Word Length, and Technique of Implementing Same		Filed 4/7/2006	11/724,552 PCT/US2007/07591		
73885.001121	211.020-PCT	Memory Array Having a Programmable Word Length, and Technique of Implementing Same	Eric Carman	PCT/US2007/07591 Filed 3/29/2007	Claims Priority to: 60/790,111 Parent of: CN 2007 8000 7134.4	NAS	Expired
73885.001122	211.020-CN	Memory Array Having a Programmable Word Length, and Technique of Implementing Same	Eric Carman	CN 2007 8000 7134.4 Filed 3/29/2007	Claims Priority to: PCT/US2007/07591	NAS	Pending
73885.001123	211.020-US	Memory Array Having a Programmable Word Length, and Method of Implementing Same	Eric Carman	11/724,552 Filed 3/15/2007	Claims Priority to: 60/790,111 Parent of: 12/371,551	NAS	Patent Issued 2/17/2009 U.S. Patent No. 7,492,632
73885.001124	211.020-D1	Memory Array Having a Programmable Word Length, and Method of Implementing Same	Eric Carman	12/371,551 Filed 2/13/2009	Claims Priority to: 11/724,552	NAS	Pending
73885.001125	211.021-P	Semiconductor Memory Array Architecture, and Method of Controlling Same	Gregory A. Popoff	60/792,820 Filed 4/18/2006	Parent of: 11/787,718	NAS	Converted
73885.001126	211.021-US	Semiconductor Memory Array	Gregory A. Popoff	11/787,718	Claims Priority to:	NAS	Patent Issued 10/20/2009

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		Architecture, and Method of Controlling Same		Filed 4/17/2007	60/792,820		U.S. Patent No. 7,606,098
73885.001127	211.022-P	Semiconductor Memory Cell and Array Using Punch-Through to Program and Read Same	Serguei Okhonin Mikhail Nagoga	60/796,671 Filed 5/2/2006	Parent of: 11/796,935 PCT/EP2007/054227	NAS	Converted
73885.001128	211.022-PCT	Semiconductor Memory Cell and Array Using Punch-Through to Program and Read Same	Serguei Okhonin Mikhail Nagoga	PCT/EP2007/054227 Filed 4/30/2007	Claims Priority to: 60/796,671	NAS	Expired
73885.001129	211.022-US	Semiconductor Memory Cell and Array Using Punch-Through to Program and Read Same	Serguei Okhonin Mikhail Nagoga	11/796,935 Filed 4/30/2007	Claims Priority to: 60/796,671	NAS	Pending
73885.001130	211.023-P	Memory Array Having Row Redundancy, and Method of Programming, Controlling and/or Operating Same	Anant P Singh	60/801,809 Filed 5/19/2006	Parent to: 11/804,098 PCT/US2007/12026	NAS	Converted
73885.001131	211.023-PCT	Integrated Circuit Having Memory Array Including Row Redundancy, and Method of Programming, Controlling and/or Operating Same	Anant P Singh	PCT/US2007/12026 Filed 5/18/2007	Claims Priority to: 60/801,809	NAS	Expired
73885.001132	211.023-US	Integrated Circuit Having Memory Array Including Row Redundancy, and Method of Programming, Controlling	Anant P Singh	11/804,098 Filed 5/17/2007	Claims Priority to: 60/801,809	NAS	Patent Issued 3/3/2009 U.S. Patent No. 7,499,352

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		and/or Operating Same					
73885.001133	211.024-P	Integrated Circuit Having Memory Array Including ECC and/or Column Redundancy, and Method of Programming, Controlling and/or Operating Same	Anant P. Singh	60/816,416 Filed 6/26/2006	Parent of: 11/821,469 PCT/US2007/14679	NAS	Converted
73885.001134	211.024-PCT	Integrated Circuit Having Memory Array Including ECC and/or Column Redundancy, and Method of Programming, Controlling and/or Operating Same	Anant P. Singh	PCT/US2007/14679 Filed 6/25/2007	Claims Priority to: 60/816,416	NAS	Expired
73885.001135	211.024-US	Integrated Circuit Having Memory Array Including ECC and/or Column Redundancy, and Method of Programming, Controlling and/or Operating Same	Anant P. Singh	11/821,469 Filed 6/22/2007	Claims Priority to: 60/816,416	NAS	Pending
73885.001136	211.025-P	Integrated Circuit Having Memory Array Having a Segmented Bit Line Architecture and Method of Controlling and/or Operating Same	David Fisch Michel Bron	60/830,084 Filed 7/11/2006	Parent to: 11/821,848 PCT/US2007/15717	NAS	Converted
73885.001137	211.025-PCT	Integrated Circuit Having a Segmented Bit Line	David Fisch Michel Bron	PCT/US2007/15717 Filed 7/10/2007	Claims Priority to: 60/830,084	NAS	Expired

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		Architecture and Method of Controlling and/or Operating Same			Parent of: CN 2007 8001 9731.9 EP 07810300.9		
73885.001138	211.025-EP	Integrated Circuit Having a Segmented Bit Line Architecture and Method of Controlling and/or Operating Same	David Fisch Michel Bron	EP 07810300.9 Filed 7/10/2007	Claims Priority to: PCT/US2007/15717	NAS	Pending
73885.001139	211.025-CN	Integrated Circuit Having a Segmented Bit Line Architecture and Method of Controlling and/or Operating Same	David Fisch Michel Bron	CN 2007 8001 9731.9 Filed 7/10/2007	Claims Priority to: PCT/US2007/15717	NAS	Pending
73885.001140	211.025-US	Integrated Circuit Having a Segmented Bit Line Architecture and Method of Controlling and/or Operating Same	David Fisch Michel Bron	11/821,848 Filed 6/26/2007	Claims Priority to: 60/830,084 Parent of: 12/467,331	NAS	Patent Issued 6/2/2009 U.S. Patent No. 7,542,340
73885.001141	211.025-D1	Integrated Circuit Having a Segmented Bit Line Architecture and Method of Controlling and/or Operating Same	David Fisch Michel Bron	12/467,331 Filed 5/18/2009	Divisional of: 11/821,848	NAS	Pending
73885.001142	211.026-US	Read Circuitry for an	Philippe Bauser	12/080,642		NAS	Pending

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		Integrated Circuit Having Memory Cells and/or Memory Cell Array, and Method of Operating Same		Filed 4/4/2008			
73885.001143	211.027-P	Integrated Circuit Having Voltage Generation Circuitry for Memory Cell Array, and Method of Operating and/or Controlling Same	David Fisch Philippe Bauser	60/932,223 Filed 5/30/2007	Parent of: 12/154,835 PCT/US2008/006743	NAS	Converted
73885.001144	211.027-PCT	Integrated Circuit Having Voltage Generation Circuitry for Memory Cell Array, and Method of Operating and/or Controlling Same	David Fisch Philippe Bauser	PCT/US2008/006743 Filed 5/28/2008	Claim Priority to: 60/932,223	NAS	Expired
73885.001145	211.027-US	Integrated Circuit Having Voltage Generation Circuitry for Memory Cell Array, and Method of Operating and/or Controlling Same	David Fisch Philippe Bauser	12/154,835 Filed 5/27/2008	Claim Priority to: 60/932,223	NAS	Pending
73885.001146	211.027-KR	Integrated Circuit Having Voltage Generation Circuitry for Memory Cell Array, and Method of Operating and/or Controlling Same	David Fisch Philippe Bauser	2009-7024854 Filed 11/27/2009	Claim Priority to: PCT/US2008/006743 12/154,835	NAS	Pending
73885.001147	211.028-P	Sense Amplifier Circuitry for Integrated Circuit Having Memory Cell Array, and	Philippe Graber	60/967,605 Filed 9/6/2007	Parent of: PCT/EP2008/061270	NAS	Converted

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		Method of Operating Same			12/218,895		
73885.001148	211.028-PCT	Sense Amplifier Circuitry for Integrated Circuit Having Memory Cell Array, and Method of Operating Same	Philippe Graber	PCT/EP2008/061270 Filed 8/28/2008	Claims Priority to: 60/967,605	NAS	Expired
73885.001149	211.028-US	Sense Amplifier Circuitry for Integrated Circuit Having Memory Cell Array, and Method of Operating Same	Philippe Graber	12/218,895 Filed 7/18/2008	Claims Priority to: 60/967,605	NAS	Patent Issued 8/31/2010 U.S. Patent No. 7,787,319
73885.001150	211.029-P	Integrated Circuit Having Memory Cell Array Including Barriers, and Method of Manufacturing Same	Pierre Fazan	61/004,672 Filed 11/29/2007	Parent of: PCT/EP2008/006620 12/268,671	NAS	Converted
73885.001151	211.029-PCT	Integrated Circuit Having Memory Cell Array Including Barriers, and Method of Manufacturing Same	Pierre Fazan	PCT/EP2008/006620 Filed 11/26/2008	Claims Priority to: 61/004,672 12/268,671	NAS	Expired
73885.001152	211.029-US	Integrated Circuit Having Memory Cell Array Including Barriers, and Method of Manufacturing Same	Pierre Fazan	12/268,671 Filed 11/11/2008	Claims Priority to: 61/004,672	NAS	Pending
73885.001153	211.030-P	Integrated Circuit Having Memory Cell Array, and Method of Manufacturing Same	Danngis Liu	61/007,103 Filed 12/11/2007	Parent of: 12/332,413	NAS	Converted
73885.001154	211.030-US	Integrated Circuit Having Memory Cell Array, and	Danngis Liu	12/332,413	Claims Priority to:	NAS	Pending

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		Method of Manufacturing Same		Filed 12/11/2008	61/007,103		
73885.001155	211.031-P	Integrated Circuit Having Memory Cells Including Gate Including Gate Material Having High Work Function, and Method of Manufacturing Same	Viktor Koldiaev	61/065,025 Filed 2/8/2008	Parent of: PCT/US2009/032938 12/363,841	NAS	Converted
73885.001156	211.031-PCT	Integrated Circuit Having Memory Cells Including Gate Including Gate Material Having High Work Function, and Method of Manufacturing Same	Viktor Koldiaev	PCT/US2009/032938 Filed 2/3/2009	Claims Priority to: 61/065,025	NAS	Expired
73885.001157	211.031-US	Integrated Circuit Having Memory Cells Including Gate Including Gate Material Having High Work Function, and Method of Manufacturing Same	Viktor Koldiaev	12/363,841 Filed 2/2/2009	Claims Priority to: 61/065,025	NAS	Pending
73885.001158	211.032-P	Integrated Circuit Having Electrical Isolation Trenches, Mask Technology and Method of Manufacturing Same	Viktor Koldiaev	61/065,485 Filed 2/12/2008	Parent of: 12/368,333	NAS	Converted
73885.001159	211.032-US	Integrated Circuit Having Electrical Isolation Trenches, Mask Technology and Method	Viktor Koldiaev	12/368,333 Filed 2/10/2009	Claims Priority to: 61/065,485	NAS	Abandoned per client request

Attorney Docket No.	Client Ref. No.	Title	Inventor(s)	Appln. No. Filing Date	Affiliation(s)	Atty.	Status/Comments
		of Manufacturing Same					

List of Trademarks

Owner / Applicant	ES Ref.	Trademark	Class(es)	Country	Priority	Filinge Date	Registration Date	Serial Number	Your Ref.	Next Renewal Due	Status
Innovative Silicon ISi SA	IH 180-01EU	Z-RAM	EU 09	**Community Trademark:** Austria, Belgium, Bulgaria, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Netherlands, Poland, Portugal, Romania, Slovak Republic, Slovenia, Spain, Sweden, United Kingdom		10 November 2004	7 December 2005	004115796		30 November 2014 1st renewal fee	registered
Innovative Silicon ISi SA	IH 180-02WO	Wort: Z-RAM	WO 09	**International:** Switzerland, China, Korea, Singapore		10 February 2006	10 February 2006	884 231		10 February 2016 1st renewal fee	registered
Innovative Silicon ISi SA	IH 180-03HK	Z-RAM	HK 09	Hong Kong	European Community Countries 10.11.2004 004115796	9 May 2005	9 May 2005	300417096		10 November 2014 1st renewal fee	registered

Owner / Applicant	ES Ref.	Trademark	Class(es)	Country	Priority	Filinge Date	Registration Date	Serial Number	Your Ref.	Next Renewal Due	Status
Innovative Silicon ISi SA	IH 180-04TW	Z-RAM	**TW** 09	Taiwan	European Community Countries 10.11.2004 004115796	9 May 2005	16 January 2007	1246603		15 January 2017 1st renewal fee	registered

Word Mark	**Z-RAM**
Goods and Services	IC 009. US 021 023 026 036 038. G & S: Computer memory hardware. FIRST USE: 20050100. FIRST USE IN COMMERCE: 20050100
Serial Number	78490817
Filing Date	September 28, 2004
Published for Opposition	September 27, 2005
Registration Number	3245372
Registration Date	May 22, 2007
Owner	(REGISTRANT) Innovative Silicon ISi S.A. CORPORATION SWITZERLAND PSE - Batiment B Lausanne SWITZERLAND CH-1015
Attorney of Record	James M. McCarthy
Type of Mark	TRADEMARK
Register	PRINCIPAL

List of Domain Names

Domain Name	Expiration
Z-RAM.COM	11/20/2011
INNOVATIVESILICON.COM	11/20/2011