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OMB Collection 0651-0027 (exp. 03/31/2012)

U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

RECORDATION FORM COVER SHEET
TRADEMARKS ONLY

To the Director of the U. S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies):

JPMorgan Chase Bank, N.A., as Administrative Agent

☐ Individual(s) ☐ Association
☐ General Partnership ☐ Limited Partnership
☐ Corporation- State:
☒ Other National Association

Citizenship (see guidelines) United States

Additional names of conveying parties attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies)

Additional names, addresses, or citizenship attached? ☐ Yes ☒ No

Name: Endicott Interconnect Technologies, Inc.
Internal Address: 1093 Clark Street
Street Address:
City: Endicott
State: NY
Country: U.S.A. Zip: 13760

☐ Association Citizenship
☐ General Partnership Citizenship
☐ Limited Partnership Citizenship
☒ Corporation Citizenship New York
☐ Other Citizenship

If assignee is not domiciled in the United States, a domestic representative designation is attached: ☐ Yes ☐ No
(Designations must be a separate document from assignment)

3. Nature of conveyance)/Execution Date(s) :

Execution Date(s) 2/10/2012

☐ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☒ Other Release by Secured Party

4. Application number(s) or registration number(s) and identification or description of the Trademark.

A. Trademark Application No.(s)

B. Trademark Registration No.(s)
3,564,994; 3,619,679; 2,829,453; 2,831,497; 2,632,339
2,594,509; 2,881,049; 2,829,454

Additional sheet(s) attached? ☐ Yes ☒ No

C. Identification or Description of Trademark(s) (and Filing Date if Application or Registration Number is unknown):

5. Name & address of party to whom correspondence concerning document should be mailed:

Name: Olivia H. Tarbox, Paralegal
Internal Address: One Logan Square
Street Address: Blank Rome LLP - 8th Floor
City: Philadelphia
State: Pennsylvania Zip: 19103-6998
Phone Number: (215) 988-6991
Fax Number: (215) 832-5500
Email Address: tarbox@blankrome.com

6. Total number of applications and registrations involved: 8

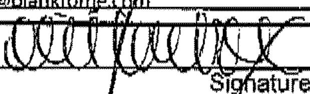
7. Total fee (37 CFR 2.6(b)(6) & 3.41) $215.00

☒ Authorized to be charged to deposit account
☐ Enclosed

8. Payment Information:

Deposit Account Number 022555
Authorized User Name Olivia Tarbox

9. Signature:



Signature

4/30/2012
Date

Olivia H. Tarbox, Paralegal
Name of Person Signing

Total number of pages including cover sheet, attachments, and document: 21

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O. Box 1450, Alexandria, VA 22313-1450

CH $215.00 022555 3564994

NOTICE OF RELEASE OF SECURITY INTEREST

This Notice of Release of Security Interest (this "Release") is effective as of February 10, 2012, by JPMorgan Chase Bank, N.A., as Administrative Agent (the "Administrative Agent").

WHEREAS, reference is made to (i) a certain Confirmatory Grant of Security Interest in United States Trademarks dated as of September 30, 2008 (the "Trademark Confirmatory Grant") by Endicott Interconnect Technologies, Inc., a New York corporation (the "Grantor") in favor of the Administrative Agent and (ii) a certain Confirmatory Grant of Security Interest in United States Patents, dated as of September 30, 2008 (the "Patent Confirmatory Grant" and, together with the Trademark Confirmatory Grant, the "Confirmatory Grants"), by the Grantor in favor of the Administrative Agent;

WHEREAS, pursuant to the Confirmatory Grants, the Grantor granted to the Administrative Agent a security interest in certain of the Grantor's assets, including, without limitation, all of the trademarks and patents ("Trademarks and Patents") owned by Grantor as described in the Confirmatory Grants and as set forth in Exhibit A attached hereto; and

WHEREAS, the Trademark Confirmatory Grant and the Patent Confirmatory Grant were recorded with the United States Patent and Trademark Office on November 26, 2008 at Reel/Frame 3894/0733 and on December 3, 2008 at Reel/Frame 021912/0908, respectively.

NOW, THEREFORE, intending to be legally bound hereby and in connection with the Confirmatory Grants, Administrative Agent hereby releases and remits, without any recourse, representation or warranty, any and all rights, title and interests in and to the Trademarks and Patents, and hereby authorizes the Grantor or Grantor's authorized representative to record this Release with the United States Patent and Trademark Office as evidence of such release.

[SIGNATURE PAGE FOLLOWS]

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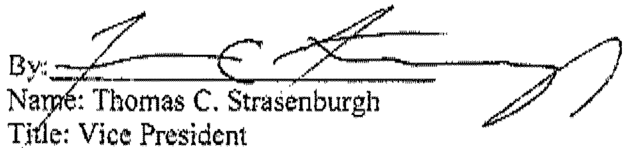
IN WITNESS WHEREOF, the Administrative Agent duly executes this Release, which is effective as of the day and year first written above.

JPMORGAN CHASE BANK, N.A., as Administrative Agent



By: ____________________
Name: Thomas C. Strasenburgh
Title: Vice President

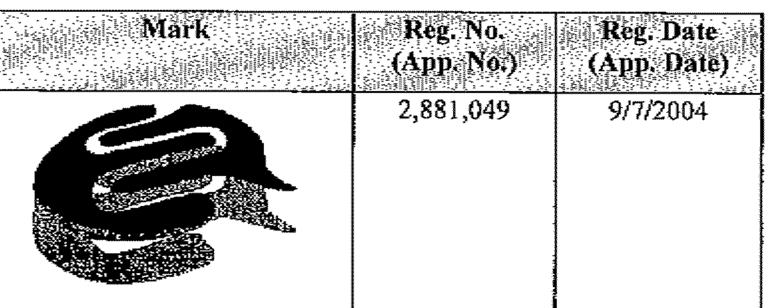
[SIGNATURE PAGE TO NOTICE OF RELEASE OF SECURITY INTEREST]

EXHIBIT A TO NOTICE OF RELEASE OF SECURITY INTEREST

Active U.S. Trademark Registrations and Applications:

Mark	Reg. No. (App. No.)	Reg. Date (App. Date)
CoreEZ	3,564,994	1/20/2009
COREEZ	3,619,679	5/12/2009
ENDICOTT INTERCONNECT TECHNOLOGIES	2,829,453	4/6/2006
ENDICOTT INTERCONNECT	2,831,497	4/13/2006
HYPERBGA	2,632,339	10/2/2002
DRICLAD	2,594,509	7/16/2002

Inactive U.S. Trademark Registrations and Applications:

Mark	Reg. No. (App. No.)	Reg. Date (App. Date)
	2,881,049	9/7/2004

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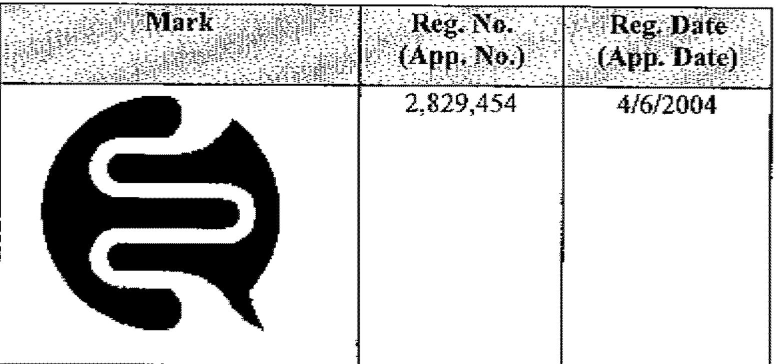
Mark	Reg. No. (App. No.)	Reg. Date (App. Date)
	2,829,454	4/6/2004

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Active U.S. Patents and Patent Applications:

Title	Patent No. (App. No.)	Issue Date (App. Date)
Circuitized substrate utilizing three smooth-sided conductive layers as part thereof and electrical assemblies and information handling systems utilizing same	(11/215,206)	(8/31/2005)
Capacitor material with metal component for use in circuitized substrates, circuitized substrate utilizing same, method of making said circuitized substrate, and information handling system utilizing said circuitized substrate	(11/324,273)	(1/4/2006)
Method of making printed circuit board having varying depth conductive holes	(11/334,445)	(1/19/2006)
Solder mask application process	(11/500,328)	(8/8/2006)
Method of making circuitized substrate with solder balls having roughened surfaces, method of making electrical assembly including said circuitized substrate, and method of making multiple	(11/650,520)	(1/8/2007)

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Title	Patent No. (App. No.)	Issue Date (App. Date)
circuitized substrate assembly		
Non-flaking capacitor material, capacitive substrate having an internal capacitor therein including said non-flaking capacitor material, and method of making a capacitor member for use in a capacitive substrate	(11/730,761)	(4/4/2007)
Method of making a circuitized substrate having at least one capacitor therein	(11/878,673)	(7/26/2007)
Adhesive bleed prevention method and product produced from same	(11/882,149)	(7/31/2007)
Circuitized substrate with dielectric layer having dielectric composition not including continuous or semi-continuous fibers	(11/896,786)	(9/6/2007)
Circuitized substrate with increased roughness conductive layer as part thereof	(11/976,629)	(10/26/2007)
Circuitized substrate with sintered paste connections and multilayered substrate assembly having said substrate as part thereof	(12/007,178)	(1/8/2008)
Method of making circuitized assembly including a plurality of circuitized substrates	(12/007,704)	(1/15/2008)

Title	Patent No. (App. No.)	Issue Date (App. Date)
Method of making circuitized substrates having film resistors as part thereof	(12/007,820)	(1/16/2008)
Method of making high speed interposer	(12/010,469)	(1/25/2008)
Circuitized, multilayer substrate	(12/078,206)	(3/28/2008)
Circuitized substrate assembly and method of making same	6,809,269	10/26/2004
Electronic package with strengthened conductive pad	6,815,837	11/9/2004
High speed circuit board and method for fabrication	6,828,514	12/7/2004
Information handling system utilizing circuitized substrate	6,872,894	3/29/2005
Information handling system utilizing circuitized substrate	6,900,392	5/31/2005
Circuitized substrate and method of making same	6,905,589	6/14/2005
Material separation to form segmented product	6,958,106	10/25/2005
Circuitized substrates utilizing three smooth-sided conductive layers as part thereof, method of making same, and electrical assemblies and information handling systems utilizing same	6,964,884	11/15/2005
Stacked chip electronic package having laminate carrier and method of	6,992,896	1/31/2006

Title	Patent No. (App. No.)	Issue Date (App. Date)
making same		
High speed circuitized substrate with reduced thru-hole stub, method for fabrication and information handling system utilizing same	6,995,322	2/7/2006
Method of testing spacings in pattern of openings in PCB conductive layer	7,013,563	3/21/2006
Information handling system	7,023,707	4/4/2006
Capacitor material with metal component for use in circuitized substrates, circuitized substrate utilizing same, method of making said circuitized substrate, and information handling system utilizing said circuitized substrate	7,025,607	4/11/2006
Multi-chip electronic package having laminate carrier and method of making same	7,035,113	4/25/2006
Electrical assembly with internal memory circuitized substrate having electronic components positioned thereon, method of making same, and information handling system utilizing same	7,045,897	5/16/2006
Method of making	7,047,630	5/23/2006

Title	Patent No. (App. No.)	Issue Date (App. Date)
circuitized substrate assembly		
Circuitized substrate and method of making same	7,063,762	6/20/2006
Circuitized substrate assembly and method of making same	7,071,423	7/4/2006
Circuitized substrate	7,078,816	7/18/2006
Method of making circuitized substrate	7,084,014	8/1/2006
Method of making a circuitized substrate having a plurality of solder connection sites thereon	7,087,441	8/8/2006
Pinned electronic package with strengthened conductive pad	7,087,846	8/8/2006
Method of making circuitized substrate	7,091,066	8/15/2006
Electronic component test apparatus	7,109,732	9/19/2006
Substrate test apparatus and method of testing substrates	7,129,732	10/31/2006
Radio frequency device for tracking goods	7,142,121	11/28/2006
Low moisture absorptive circuitized substrate, method of making same, electrical assembly utilizing same, and information handling system utilizing same	7,145,221	12/5/2006
Method of making high speed circuit board	7,152,319	12/26/2006

Title	Patent No. (App. No.)	Issue Date (App. Date)
Circuitized substrate with split conductive layer, method of making same, electrical assembly utilizing same, and information handling system utilizing same	7,157,646	1/2/2007
Circuitized substrate with filled isolation border, method of making same, electrical assembly utilizing same, and information handling system utilizing same	7,157,647	1/2/2007
Stacked chip electronic package having laminate carrier and method of making same	7,161,810	1/9/2007
Method of making circuitized substrate	7,163,847	1/16/2007
Plating method for circuitized substrates	7,169,313	1/30/2007
Printed circuit board with low cross-talk noise	7,176,383	2/13/2007
Circuitized substrate with signal wire shielding, electrical assembly utilizing same and method of making	7,209,368	4/24/2007
Method of making multilayered printed circuit board with filled conductive holes	7,211,289	5/1/2007
Method and apparatus for depositing conductive paste	7,211,470	5/1/2007

Title	Patent No. (App. No.)	Issue Date (App. Date)
in circuitized substrate openings		
Resistor material with metal component for use in circuitized substrates, circuitized substrate utilizing same, method of making said circuitized substrate, and information handling system utilizing said circuitized substrate	7,235,745	6/26/2007
Circuitized substrate with internal organic memory device, electrical assembly utilizing same, and information handling system utilizing same	7,253,502	8/7/2007
Wirebond electronic package with enhanced chip pad design, method of making same, and information handling system utilizing same	7,253,518	8/7/2007
Dielectric composition for forming dielectric layer for use in circuitized substrates	7,270,845	9/18/2007
Interposer for use with test apparatus	7,292,055	11/6/2007
Apparatus and method for making circuitized substrates in a continuous manner	7,293,355	11/13/2007
Circuitized substrate with improved impedance contol circuitry, method of making	7,294,791	11/13/2007

Title	Patent No. (App. No.)	Issue Date (App. Date)
same, electrical assembly and information handling system		
Method of treating conductive layer for use in a circuitized substrate and method of making said substrate having said conductive layer as part thereof	7,307,022	12/11/2007
Method of making circuitized substrate with internal organic memory device	7,326,643	2/5/2008
Apparatus for making circuitized substrates in a continuous manner	7,328,502	2/12/2008
Circuitized substrate with conductive polymer and seed material adhesion layer	7,332,212	2/19/2008
Multi-chip electronic package with reduced line skew and circuitized substrate for use therein	7,332,818	2/19/2008
Method of making multilayered circuitized substrate assembly having sintered paste connections	7,334,323	2/26/2008
Circuitized substrate with sintered paste connections, multilayered substrate assembly, electrical assembly and information handling system utilizing	7,342,183	3/11/2008

Title	Patent No. (App. No.)	Issue Date (App. Date)
same		
Method of making circuitized substrate assembly	7,343,674	3/18/2008
Method of providing printed circuit board with conductive holes and board resulting therefrom	7,348,677	3/25/2008
Method of making circuitized substrate with split conductive layer and information handling system utilizing same	7,377,033	5/27/2008
Method of making circuitized substrate	7,381,587	6/3/2008
Method of making circuitized substrates utilizing smooth-sided conductive layers as part thereof	7,383,629	6/10/2008
Method of making an internal capacitative substrate for use in a circuitized substrate and method of making said circuitized substrate	7,384,856	6/10/2008
Method of making same low moisture absorptive circuitized subtrave with reduced thermal expansion	7,416,972	8/26/2008
Method of making circuitized substrate	7,416,996	8/26/2008

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Title	Patent No. (App. No.)	Issue Date (App. Date)
Method of making a capacitative substrate using photoimageable dielectric for use as part of a larger circuitized substrate, method of making said circuitized substrate and method of making an information handling system including said circuitized substrate	7,429,510	9/30/2008
Fluoropolymer dielectric composition for use in circuitized substrates and circuitized substrate including same	7,429,789	9/30/2008
Electronic card assembly	7,441,709	10/28/2008
Circuitized substrate with soler-coated microparticle paste connections, multilayered substrate assembly, electrical assembly and information handling system utilizing same and method of making said substrate	7,442,879	10/28/2008

Title	Patent No. (App. No.)	Issue Date (App. Date)
Method of making a capacitative substrate for use as part of a larger circuitized substrate, method of making said circuitized substrate and method of making an information handling system including said circuitized substrate	7,449,381	11/11/2008
Low moisture absorptive circuitized substrate with reduced thermal expansion, method of making same, electrical assembly utilizing same, and information handling system utilizing same	7,470,990	12/30/2008
Method of making circuitized substrate with signal wire shielding	7,478,472	1/20/2009
Information handling system utilizing circuitized substrate with split conductive layer	7,491,896	2/17/2009
Interposer and test assembly for testing electronic devices	7,501,839	3/10/2009
Information handling system including a circuitized substrate having a dielectric layer without continuous fibers	7,508,076	3/24/2009
Method of making wirebond electronic package with enhanced chip pad design	7,510,912	3/31/2009

Title	Patent No. (App. No.)	Issue Date (App. Date)
Method of making an interposer	7,511,518	3/31/2009
Method of making a printed circuit board with low cross-talk noise	7,530,167	5/12/2009
Method of making circuitized substrate with internal optical pathway	7,541,058	6/2/2009
Capacitor material for use in circuitized substrates, circuitized substrate utilizing same, method of making said circuitized substrate, and information handling system utilizing said circuitized substrate	7,541,265	6/2/2009
Method of making circuitized substrate with solder paste connections	7,547,577	6/16/2009
Method and system for tracking goods	7,552,091	6/23/2009
Method of making circuitized substrate with improved impedance control circuitry, electrical assembly and information handling system	7,589,283	9/15/2009
Method of making a circuitized substrate with enhanced circuitry and electrical assembly utilizing said substrate	7,595,454	9/29/2009
Method of providing a printed circuit board with an	7,596,863	10/6/2009

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Title	Patent No. (App. No.)	Issue Date (App. Date)
edge connection portion and/or a plurality of caivities therein		
Method of making multi-chip electronic package with reduced line skew	7,622,384	11/24/2009
Method for making a multilayered circuitized substrate	7,627,947	12/8/2009
High speed interposer	7,629,541	12/8/2009
Method of improving electrical connections in circuitized substrates	7,629,559	12/8/2009
Adjustable thickness thermal interposer and electronic package utilizing same	7,629,684	12/8/2009
Photoresist composition with antibacterial agent	7,635,552	12/22/2009
Multilayered circuitized substrate with p-aramid dielectric layers and method of making same	7,646,098	1/12/2010
Method of making a multi-chip electronic package having laminate carrier	7,665,207	2/23/2010
Circuitized substrate with shielded signal lines and plated-thru-holes and method of making same, and electrical assembly and information handling system utilizing same	7,679,005	3/16/2010
Halogen-free circuitized	7,687,722	3/30/2010

Title	Patent No. (App. No.)	Issue Date (App. Date)
substrate with reduced thermal expansion, method of making same, multilayered substrate structure utilizing same, and information handling system utilizing		
Circuitized substrate with internal resistor, method of making said circuitized substrate, and electrical assembly utilizing said circuitized substrate	7,687,724	3/30/2010
Method of providing a printed circuit board with an edge connection portion	7,712,210	5/11/2010
Method of making circuitized substrate with internal optical pathway using photolithography	7,713,767	5/11/2010
Circuitized substrate with internal cooling structure and electrical assembly utilizing same	7,738,249	6/15/2010
Circuitized substrate with internal stacked semiconductor chips, method of making same, electrical assembly utilizing same and information handling system utilizing same	7,800,916	9/21/2010
Item identification control method	7,801,833	9/21/2010

Title	Patent No. (App. No.)	Issue Date (App. Date)
Method of making circuitized substrate with filled isolation border	7,814,649	10/19/2010
Method of making multilayered circuitized substrate assembly	7,823,274	11/2/2010
Apparatus for making circuitized substrates having photo-imageable dielectric layers in a continuous manner	7,827,682	11/9/2010
Circuitized substrates utilizing smooth-sided conductive layers as part thereof	7,838,776	11/23/2010
LED lighting assembly and lamp utilizing same	7,841,741	11/30/2010
Flexible circuit electronic package with standoffs	7,851,906	12/14/2010
Method of making circuitized substrate with a resistor	7,870,664	1/18/2011
High speed interposer	7,875,811	1/25/2011
Capacitive substrate	7,897,877	3/1/2011
Method of making circuitized substrate with selected conductors having solder thereon	7,910,156	3/22/2011
Dielectric composition for use in circuitized substrates and circuitized substrate including same	7,931,830	4/26/2011

Title	Patent No. (App. No.)	Issue Date (App. Date)
Spring actuated clamping mechanism	8,028,390	10/4/2011
Circuitized substrate with conductive paste, electrical assembly including said circuitized substrate and method of making said substrate	8,063,315	11/22/2011
Circuitized substrate with continuous thermoplastic support film dielectric layers	8,084,863	12/27/2011

Inactive U.S. Patent and Patent Applications:

Title	Patent No. (App. No.)	Issue Date (App. Date)
Electronic card	(10/449,019)	(6/2/2003)
Electronic package with conductive pad capable of withstanding significant loads	(10/868,066)	(6/16/2004)
Method of making a circuitized substrate having a plurality of solder connection sites thereon	(11/253,659)	(10/20/2005)

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