

## TRADEMARK ASSIGNMENT

Electronic Version v1.1  
 Stylesheet Version v1.1

|                           |   |                                 |                         |
|---------------------------|---|---------------------------------|-------------------------|
| SUBMISSION TYPE:          | NEW ASSIGNMENT  |                                 |                         |
| NATURE OF CONVEYANCE:     | SECURITY INTEREST   |                                 |                         |
| CONVEYING PARTY DATA      |   |                                 |                         |
| Name                      | Formerly  | Execution Date                  | Entity Type             |
| AEHR TEST SYSTEMS         |   | 08/21/2013                      | CORPORATION: CALIFORNIA |
| RECEIVING PARTY DATA      |   |                                 |                         |
| Name:                     | SILICON VALLEY BANK   |                                 |                         |
| Street Address:           | 3003 TASMAN DRIVE   |                                 |                         |
| City:                     | SANTA CLARA   |                                 |                         |
| State/Country:            | CALIFORNIA  |                                 |                         |
| Postal Code:              | 95054   |                                 |                         |
| Entity Type:              | CORPORATION: CALIFORNIA   |                                 |                         |
| PROPERTY NUMBERS Total: 1 |   |                                 |                         |
| Property Type             | Number  | Word Mark                       |                         |
| Registration Number:      | 1994800   | DIEPAK KNOWN GOOD DIE SOLUTIONS |                         |
| CORRESPONDENCE DATA       |   |                                 |                         |
| Fax Number:               | 4088524475  |                                 |                         |
|                           | <i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent via US Mail.</i> |                                 |                         |
| Phone:                    | 4088417195  |                                 |                         |
| Email:                    | dsanchezbentz@vlpawgroup.com  |                                 |                         |
| Correspondent Name:       | Diana Sanchez Bentz, Legal Specialist   |                                 |                         |
| Address Line 1:           | VLP Law Group LLP   |                                 |                         |
| Address Line 2:           | 235 Victoria Drive  |                                 |                         |
| Address Line 4:           | Gilroy, CALIFORNIA 95020  |                                 |                         |
| ATTORNEY DOCKET NUMBER:   | SVB-AEHR (TM)   |                                 |                         |
| NAME OF SUBMITTER:        | Diana Sanchez Bentz   |                                 |                         |
| Signature:                | /DSB1068/   |                                 |                         |

Date:

09/05/2013

**Total Attachments: 11**

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## INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement (“Agreement”) is entered into as of August 21, 2013 by and between SILICON VALLEY BANK (“Bank”) and AEHR TEST SYSTEMS (“Grantor”).

### RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodations to Grantor (the “Loans”) in the amounts and manner set forth in that certain Loan and Security Agreement by and between Bank and Grantor dated August 25, 2011 (as the same has been and may be further amended, modified or supplemented from time to time, the “Domestic Loan Agreement”; capitalized terms not otherwise defined in this Agreement shall have the meanings set forth in the Domestic Loan Agreement) and that certain Export-Import Bank Loan and Security Agreement by and between Bank and Grantor dated as of August 25, 2011 (as the same has been and may be further amended, modified or supplemented from time to time, the “Ex-Im Loan Agreement”, and together with the Domestic Loan Agreement, the “Loan Agreements”). As used herein, “Loan Documents” shall mean all “Loan Documents” as defined in the Loan Agreements. Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in certain Copyrights, Trademarks, Patents, and Mask Works (as each term is described below) to secure the obligations of Grantor under the Loan Agreements.

B. Pursuant to the terms of the Loan Agreements, Grantor has granted to Bank a security interest in all of Grantor’s right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreements, Grantor hereby represents, warrants, covenants and agrees as follows:

### AGREEMENT

1. Grant of Security Interest. To secure its obligations under the Loan Agreements, Grantor grants and pledges to Bank a security interest in all of Grantor’s right, title and interest in, to and under its intellectual property (all of which shall collectively be called the “Intellectual Property Collateral”), including, without limitation, the following:

(a) Any and all copyright rights, copyright applications, copyright registrations and like protections in each work of authorship and derivative work thereof, whether published or unpublished and whether or not the same also constitutes a trade secret, now or hereafter existing, created, acquired or held, including without limitation those set forth on Exhibit A attached hereto (collectively, the “Copyrights”);

(b) Any and all trade secrets, and any and all intellectual property rights in computer software and computer software products now or hereafter existing, created, acquired or held;

(c) Any and all design rights that may be available to Grantor now or hereafter existing, created, acquired or held;

(d) All patents, patent applications and like protections including, without limitation, improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the same, including without limitation the patents and patent applications set forth on Exhibit B attached hereto (collectively, the "Patents");

(e) Any trademark and servicemark rights, whether registered or not, applications to register and registrations of the same and like protections, and the entire goodwill of the business of Grantor connected with and symbolized by such trademarks, including without limitation those set forth on Exhibit C attached hereto (collectively, the "Trademarks");

(f) All mask works or similar rights available for the protection of semiconductor chips, now owned or hereafter acquired, including, without limitation those set forth on Exhibit D attached hereto (collectively, the "Mask Works");

(g) Any and all claims for damages by way of past, present and future infringements of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above;

(h) All licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works and all license fees and royalties arising from such use to the extent permitted by such license or rights;

(i) All amendments, extensions, renewals and extensions of any of the Copyrights, Trademarks, Patents, or Mask Works; and

(j) All proceeds and products of the foregoing, including without limitation all payments under insurance or any indemnity or warranty payable in respect of any of the foregoing.

2. Recordation. Grantor authorizes the Commissioner for Patents, the Commissioner for Trademarks and the Register of Copyrights and any other government officials to record and register this Agreement upon request by Bank.

Grantor hereby authorizes Bank to (a) modify this Agreement unilaterally by amending the exhibits to this Agreement to include any Intellectual Property Collateral which Grantor obtains subsequent to the date of this Agreement and (b) file a duplicate original of this Agreement containing amended exhibits reflecting such new Intellectual Property Collateral.

3. Loan Documents. This Agreement has been entered into pursuant to and in conjunction with the Loan Agreements, which is hereby incorporated by reference. The provisions of the Loan Agreements shall supersede and control over any conflicting or inconsistent provision herein. The rights and remedies of Bank with respect to the Intellectual Property Collateral are as provided by the Loan Agreements and related documents, and nothing in this Agreement shall be deemed to limit such rights and remedies.

4. Execution in Counterparts. This Agreement may be executed in counterparts (and by different parties hereto in different counterparts), each of which shall constitute an original, but all of which when taken together shall constitute a single contract. Delivery of an executed counterpart of a signature page to this Agreement by facsimile or in electronic (i.e., “pdf” or “tif” format) shall be effective as delivery of a manually executed counterpart of this Agreement.

5. Successors and Assigns. This Agreement will be binding on and shall inure to the benefit of the parties hereto and their respective successors and assigns.

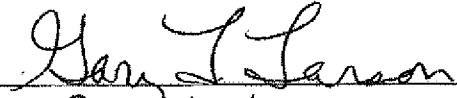
6. Governing Law. This Agreement and any claim, controversy, dispute or cause of action (whether in contract or tort or otherwise) based upon, arising out of or relating to this Agreement and the transactions contemplated hereby and thereby shall be governed by, and construed in accordance with, the laws of the United States and the State of California, without giving effect to any choice or conflict of law provision or rule (whether of the State of California or any other jurisdiction).

[Signature page follows.]

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

AEHR TEST SYSTEMS

  
By: Gary L. Larson  
Title: VP, CEO

BANK:

SILICON VALLEY BANK


  
By: Minal Patel  
Title: Relationship Manager / VP

EXHIBIT A

Copyrights

Description

Registration/  
Application  
Number

Registration/  
Application  
Date

NONE

EXHIBIT B

Patents

| <u>Description</u>   | <u>Application/<br/>Publication/<br/>Patent<br/>Number</u> | <u>Filing/<br/>Publication/<br/>Registration<br/>Date</u> |
|--|--|---|
| PRINTED CIRCUIT BOARD LOADER/UNLOADER  | 07/526069<br>5093984                                       | 5/18/1990<br>3/10/1992                                    |
| REUSABLE DIE CARRIER FOR BURN-IN AND BURN-IN PROCESS   | 08/089752<br>5517125                                       | 7/9/1993<br>5/14/1996                                     |
| METHOD AND SYSTEM FOR TESTING MEMORY PROGRAMMING DEVICES   | 08/407103<br>5682472                                       | 3/17/1995<br>10/28/1997                                   |
| WAFER-LEVEL BURN-IN AND TEST CARTRIDGE   | 09/353214<br>6340895                                       | 7/14/1999<br>1/22/2002                                    |
| KINEMATIC COUPLING   | 09/353123<br>6413113                                       | 7/14/1999<br>7/2/2002                                     |
| WAFER BURN-IN AND TEST EMPLOYING DETACHABLE CARTRIDGE  | 09/884537<br>6556032                                       | 6/18/2001<br>4/29/2003                                    |
| WATER LEVEL BURN-IN AND ELECTRICAL TEST SYSTEM AND METHOD  | 09/353121<br>6562636                                       | 7/14/1999<br>5/13/2003                                    |
| WAFER LEVEL BURN-IN AND TEST METHODS   | 09/353116<br>6580283                                       | 7/14/1999<br>6/17/2003                                    |
| WAFER LEVEL BURN-IN AND ELECTRICAL TEST SYSTEM AND METHOD  | 09/865957<br>6682945                                       | 5/25/2001<br>1/27/2004                                    |
| SYSTEM FOR BURN-IN TESTING OF ELECTRONIC DEVICES   | 10/184525<br>6815966                                       | 6/27/2002<br>11/9/2004                                    |
| CONTACTOR ASSEMBLY FOR TESTING ELECTRICAL CIRCUITS   | 10/197133<br>6853209                                       | 7/16/2002<br>2/8/2005                                     |
| DIE CARRIER  | 10/245934<br>6859057                                       | 9/17/2002<br>2/22/2005                                    |
| ASSEMBLY FOR ELECTRICALLY CONNECTING A TEST COMPONENT TO A TESTING MACHINE FOR TESTING ELECTRICAL CIRCUITS ON THE TEST COMPONENT | 10/197104<br>6867608                                       | 7/16/2002<br>3/15/2005                                    |
| SYSTEM FOR TESTING AND BURNING IN OF INTEGRATED CIRCUITS   | 11/013855<br>7053644                                       | 12/15/2004<br>5/30/2006                                   |



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| WAFER BURN-IN AND TEST EMPLOYING DETACHABLE CARTRIDGE  | 10/396170<br>7088117 | 3/24/2003<br>8/8/2006    |
| RELOADING OF DIE CARRIERS WITHOUT REMOVAL OF DIE CARRIERS FROM SOCKETS ON TEST BOARDS                                    | 10/940288<br>7303929 | 9/13/2004<br>12/4/2007   |
| WAFER LEVEL BURN-IN AND ELECTRICAL TEST SYSTEM AND METHOD  | 10/718825<br>7619428 | 11/21/2003<br>11/17/2009 |
| ELECTRONICS TESTER WITH A SIGNAL DISTRIBUTION BOARD AND A WAFER CHUCK HAVING DIFFERENT COEFFICIENTS OF THERMAL EXPANSION | 12/062988<br>7667475 | 4/4/2008<br>2/23/2010    |
| APPARATUS FOR TESTING ELECTRONIC DEVICES   | 11/413323<br>7762822 | 4/27/2006<br>7/27/2010   |
| SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE   | 11/960453<br>7800382 | 12/19/2007<br>9/21/2010  |
| APPARATUS FOR TESTING ELECTRONIC DEVICES   | 11/522216<br>7826995 | 9/14/2006<br>11/2/2010   |
| SEPARATE TEST ELECTRONICS AND BLOWER MODULES IN AN APPARATUS FOR TESTING AN INTEGRATED CIRCUIT                           | 12/437465<br>7969175 | 5/7/2009<br>6/28/2011    |
| SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE   | 12/411233<br>8030957 | 3/25/2009<br>10/4/2011   |
| INTERFACE ON AN ELECTRONICS CONNECTOR  | 29/327293<br>D629760 | 11/3/2008<br>12/28/2010  |
| CONNECTOR  | 29/327294<br>D630166 | 11/3/2008<br>1/4/2011    |
| HIGH-DENSITY INTERCONNECT TECHNIQUE  | 08/161282<br>5429510 | 12/1/1993<br>7/4/1995    |
| ENHANCEMENTS IN TESTING DEVICES ON BURN-IN BOARDS  | 09/407659<br>6292415 | 9/28/1999<br>9/18/2001   |
| WAFER LEVEL BURN-IN AND TEST THERMAL CHUCK AND METHOD  | 09/161323<br>6140616 | 9/25/1998<br>10/31/2000  |
| APPARATUS FOR TESTING ELECTRONIC DEVICES   | 13/353269<br>8388357 | 1/18/2012<br>3/5/2013    |
| SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE   | 12/885373<br>8228085 | 9/17/2010<br>7/24/2012   |

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| ELECTRONICS TESTER WITH A SIGNAL DISTRIBUTION BOARD AND A WAFER CHUCK HAVING DIFFERENT COEFFICIENTS OF THERMAL EXPANSION           | 13/022803<br>8198909     | 2/8/2011<br>6/12/2012    |
| APPARATUS FOR TESTING ELECTRONIC DEVICES   | 12/772932<br>8118618     | 5/3/2010<br>2/21/2012    |
| WAFER LEVEL BURN-IN AND ELECTRICAL TEST SYSTEM AND METHOD  | 12/574447<br>7928754     | 10/6/2009<br>4/19/2011   |
| ELECTRONICS TESTER WITH A SIGNAL DISTRIBUTION BOARD AND A WAFER CHUCK HAVING DIFFERENT COEFFICIENTS OF THERMAL EXPANSION           | 12/684051<br>7902846     | 1/7/2010<br>3/8/2011     |
| WAFER BURN-IN AND TEST EMPLOYING DETACHABLE CARTRIDGE  | 11/276314<br>7541822     | 2/23/2006<br>6/2/2009    |
| ASSEMBLY FOR ELECTRICALLY CONNECTING A TEST COMPONENT TO A TESTING MACHINE FOR TESTING ELECTRICAL CIRCUITS ON THE TEST COMPONENT   | 12/045480<br>7511521     | 3/10/2008<br>3/31/2009   |
| ASSEMBLY FOR ELECTRICALLY CONNECTING A TEST COMPONENT TO A TESTING MACHINE FOR TESTING ELECTRICAL CIRCUITS ON THE TEST COMPONENT   | 11/433845<br>7385407     | 5/12/2006<br>6/10/2008   |
| CONTACTOR ASSEMBLY FOR TESTING ELECTRICAL CIRCUITS   | 10/971897<br>7301358     | 10/22/2004<br>11/27/2007 |
| DIE CARRIER  | 11/032846<br>7126363     | 1/10/2005<br>10/24/2006  |
| SYSTEM FOR BURN-IN TESTING OF ELECTRONIC DEVICES   | 10/917139<br>7063544     | 8/11/2004<br>6/20/2006   |
| ASSEMBLY FOR ELECTRICALLY CONNECTING A TEST COMPONENT TO A TESTING MACHINE FOR A TESTING ELECTRICAL CIRCUITS ON THE TEST COMPONENT | 10/912785<br>7046022     | 8/6/2004<br>5/16/2006    |
| REUSABLE DIE CARRIER FOR BURN-IN AND BURN-IN PROCESS   | 08/948696<br>6025732     | 5/6/1997<br>2/15/2000    |
| APPARATUS FOR TESTING ELECTRONIC DEVICES   | 13/754765<br>20130141135 | 1/30/2013<br>6/6/2013    |
| SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE   | 13/554722<br>20120280704 | 7/20/2012<br>11/8/2012   |
| ADHESIVELY ATTACHED STAND-OFFS ON A PORTABLE PACK FOR AN ELECTRONICS TESTER  | 13/474581<br>20120223729 | 5/17/2012<br>9/6/2012    |

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| APPARATUS FOR TESTING ELECTRONIC DEVICES   | 13/353269<br>20120113556 | 1/18/2012<br>5/10/2012  |
| SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE   | 13/223319<br>20110316577 | 9/1/2011<br>12/29/2011  |
| SEPARATE TEST ELECTRONICS AND BLOWER MODULES IN AN APPARATUS FOR TESTING AN INTEGRATED CIRCUIT                                   | 13/168910<br>20110256774 | 6/24/2011<br>10/20/2011 |
| ELECTRONICS TESTER WITH A SIGNAL DISTRIBUTION BOARD AND A WAFER CHUCK HAVING DIFFERENT COEFFICIENTS OF THERMAL EXPANSION         | 13/022803<br>20110156745 | 2/8/2011<br>6/30/2011   |
| SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE   | 12/885373<br>20110006800 | 9/17/2010<br>1/13/2011  |
| SEPARATE TEST ELECTRONICS AND BLOWER MODULES IN AN APPARATUS FOR TESTING AN INTEGRATED CIRCUIT                                   | 12/437465<br>20100283475 | 5/7/2009<br>11/11/2010  |
| SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE   | 12/411233<br>20100244866 | 3/25/2009<br>9/30/2010  |
| APPARATUS FOR TESTING ELECTRONIC DEVICES   | 12/772932<br>20100213957 | 5/3/2010<br>8/26/2010   |
| ELECTRONICS TESTER WITH A SIGNAL DISTRIBUTION BOARD AND A WAFER CHUCK HAVING DIFFERENT COEFFICIENTS OF THERMAL EXPANSION         | 12/684051<br>20100109696 | 1/7/2010<br>5/6/2010    |
| SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE   | 11/960453<br>20090160468 | 12/19/2007<br>6/25/2009 |
| ELECTRONICS TESTER WITH A SIGNAL DISTRIBUTION BOARD A WAFER CHUCK HAVING DIFFERENT COEFFICIENTS OF THERMAL EXPANSION             | 12/062988<br>20090015282 | 4/4/2008<br>1/15/2009   |
| ASSEMBLY FOR ELECTRICALLY CONNECTING A TEST COMPONENT TO A TESTING MACHINE FOR TESTING ELECTRICAL CIRCUITS ON THE TEST COMPONENT | 12/045480<br>20080150560 | 3/10/2008<br>6/26/2008  |
| WAFER LEVEL BURN-IN AND ELECTRICAL TEST SYSTEM AND METHOD  | 10/718825<br>20040113645 | 11/21/2003<br>6/17/2004 |

EXHIBIT C

Trademarks

| <u>Description</u>              | Registration/<br>Application<br><u>Number</u> | Registration/<br>Application<br><u>Date</u> |
|---------------------------------|---|---|
| DIEPAK KNOWN GOOD DIE SOLUTIONS | 1994800                                       | 08-20-1996                                  |

EXHIBIT D

Mask Works

Description

Registration/  
Application  
Number

Registration/  
Application  
Date

NONE