TRADEMARK ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
Adesto Technologies Corporation		10/04/2013	CORPORATION: CALIFORNIA
Artemis Acquisition LLC		10/04/2013	LIMITED LIABILITY COMPANY: CALIFORNIA

RECEIVING PARTY DATA

Name:	BRIDGE BANK, NATIONAL ASSOCIATION
Street Address:	55 Almaden Boulevard, Suite 100
Internal Address:	Attn: Mike Field
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95113
Entity Type:	National Banking Association: UNITED STATES

PROPERTY NUMBERS Total: 3

Property Type	Number	Word Mark
Serial Number:	85470629	ADESTO TECHNOLOGIES
Serial Number:	85470550	CBRAM
Serial Number:	85470695	ADESTO

CH $90.00 85470629

CORRESPONDENCE DATA

Fax Number: 8586385130
Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent via US Mail.
Phone: 858-677-1400
Email: susan.reynholds@dlapiper.com
Correspondent Name: DLA Piper LLP (US)
Address Line 1: 4365 Executive Drive, Suite 1100
Address Line 4: San Diego, CALIFORNIA 92121

ATTORNEY DOCKET NUMBER:	355157-162

NAME OF SUBMITTER:	Troy Zander
Signature:	/s/ Troy Zander
Date:	10/07/2013

Total Attachments: 10
source=IPSA#page1.tif
source=IPSA#page2.tif
source=IPSA#page3.tif
source=IPSA#page4.tif
source=IPSA#page5.tif
source=IPSA#page6.tif
source=IPSA#page7.tif
source=IPSA#page8.tif
source=IPSA#page9.tif
source=IPSA#page10.tif

INTELLECTUAL PROPERTY SECURITY AGREEMENT

This INTELLECTUAL PROPERTY SECURITY AGREEMENT, dated as of October 4, 2013, (the "Agreement") between BRIDGE BANK, NATIONAL ASSOCIATION ("Lender"), ADESTO TECHNOLOGIES CORPORATION and ARTEMIS ACQUISITION LLC (each a "Grantor" and collectively, "Grantors") is made with reference to (A) that certain Business Financing Agreement, dated as of October 4, 2013 (as amended from time to time, the "Loan Agreement"), between Lender and ADESTO TECHNOLOGIES CORPORATION and (B) that certain Guaranty, dated as of October 4, 2013 (as amended from time to time, the "Guaranty"), between Lender and ARTEMIS ACQUISITION LLC. Terms defined in the Loan Agreement or Guaranty have the same meanings when used in this Agreement.

For good and valuable consideration, receipt of which is hereby acknowledged, each Grantor hereby covenants and agrees as follows:

To secure the obligations under the Loan Agreement and the Guaranty, ADESTO TECHNOLOGIES CORPORATION and ARTEMIS ACQUISITION LLC respectively, grant to Lender a security interest in all right, title, and interest of Grantors in any of the following, whether now existing or hereafter acquired or created in any and all of the following property (collectively, the "Intellectual Property Collateral"):

(a) copyright rights, copyright applications, copyright registrations and like protections in each work or authorship and derivative work thereof, whether published or unpublished and whether or not the same also constitutes a trade secret, now or hereafter existing, created, acquired or held (collectively, the "Copyrights"), including the Copyrights described in Exhibit A;

(b) trademark and servicemark rights, whether registered or not, applications to register and registrations of the same and like protections, and the entire goodwill of the business of Grantor connected with and symbolized by such trademarks (collectively, the "Trademarks"), including the Trademarks described in Exhibit B;

(c) patents, patent applications and like protections including without limitation improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the same (collectively, the "Patents"), including the Patents described in Exhibit C;

(d) mask work or similar rights available for the protection of semiconductor chips or other products (collectively, the "Mask Works");

(e) trade secrets, and any and all intellectual property rights in computer software and computer software products;

(f) design rights;

(g) claims for damages by way of past, present and future infringement of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above;

(h) licenses or other rights to use, where Grantor is the licensor or transferor of any of the Copyrights, Patents, Trademarks, or Mask Works, and all license fees and royalties arising from such use to the extent permitted by such license or rights;

(i) amendments, renewals and extensions of any of the Copyrights, Trademarks, Patents, or Mask Works; and

(j) proceeds and products of the foregoing, including without limitation all payments under insurance or any indemnity or warranty payable in respect of any of the foregoing.

Notwithstanding anything to the contrary contained in this Agreement, Intellectual Property Collateral does not include rights held under a license that are not assignable by their terms without the consent of the licensor thereof (but only to the extent such restriction on assignment is enforceable under applicable law).

The rights and remedies of Lender with respect to the security interests granted hereunder are in addition to those set forth in the Loan Agreement and the Guaranty, and those which are now or hereafter available to Lender as a matter of law or equity. Each right, power and remedy of Lender provided for herein or in the Loan Agreement or the Guaranty, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right, power or remedy provided for herein, and the exercise by Lender of any one or more of such rights, powers or remedies does not preclude the simultaneous or later exercise by Lender of any other rights, powers or remedies.

[*Balance of Page Intentionally Left Blank*]

IN WITNESS WHEREOF, the parties have executed this Agreement as of the date first written above.

GRANTOR:

ADESTO TECHNOLOGIES CORPORATION

By: _____

Name: Ron Shelton

Title: CFO

Address for Notices:
Attn: Ron Shelton, CFO
1250 Borregas Avenue
Sunnyvale, CA 94089
Tel: (408) 419-4841
Fax: (408) 419-4841

GRANTOR:

ARTEMIS ACQUISITION LLC

By: Adesto Technologies Corporation,
as sole member and manager of
Artemis Acquisition LLC

By: _____
Name: Narbeh Derhacobian
Title: President and Chief Executive Officer

Address for Notices:

c/o ADESTO TECHNOLOGIES CORPORATION
1250 Borregas Ave.
Sunnyvale, CA 94089
Tel: (408) 400-0578

LENDER:

BRIDGE BANK, NATIONAL ASSOCIATION

By: _____

Name: _____

Title: SVP

Address for Notices:
Attn: Mike Field
55 Almaden Boulevard, Suite 100
San Jose, California 95113
Tel: (408) 556-6501
Fax:(408) 282-1681

[Signature Page to Intellectual Property Security Agreement]

EXHIBIT A

COPYRIGHTS

Please Check if No Copyrights Exist ☑

Type of Work:	Title:	International Standard Serial Number (ISSN):	Registration Number:	Filing Date:	Pre - registered?

EXHIBIT B

TRADEMARKS

Please Check if No Trademarks Exist ☐

Mark / Title:	U.S. Serial Number:	U.S. Registration Number:	USPTO Reference Number:	Filing Date:
adesto TECHNOLOGIES	85470629	4303684		11/11/11
CBRAM	85470550	4235215		11/11/11
Adesto	85470695	4193574		11/11/11

EXHIBIT C

PATENTS

Please Check if No Patents Exist ☐

Title:	Patent Number:	Application/ Serial Number:	Issued or Published?	Issued/Published Date:
Programmable impedance element circuits and methods	8294488		Issued	10/23/12
Variable impedance memory device biasing circuits and methods	8498164		Issued	7/30/13
Resistive switching devices and methods of formation thereof		13767800	Published	2/14/13
Low power voltage regulator circuit for use in an integrated circuit device*	6320454		Issued	11/20/01
Reference cell for high speed sensing in non-volatile memories*	6411549		Issued	6/25/02
Method of establishing reference levels for sensing multilevel memory cell states*	6618297		Issued	9/9/03
Row decoder circuit for use in programming a memory device*	6621745		Issued	9/16/03
Method of programming a multi-level memory device*	6714448		Issued	3/30/04
Method of recovering overerased bits in a memory device*	6724662		Issued	4/20/04
Approach for zero dummy byte flash memory read operation*	6879535		Issued	4/12/05
Current sense amplifier*	6946882		Issued	9/20/05
Method for identification of spi compatible serial memory devices*	7032039		Issued	4/18/06
Dual stage voltage regulation circuit*	7064529		Issued	6/20/06
Functional register decoding system for multiple plane operation*	7099226		Issued	8/29/06
Method and apparatus of a smart decoding scheme for fast synchronous read in a memory system*	7143257		Issued	11/28/06
Column/sector redundancy cam fast programming scheme using regular memory core array in multi-plane flash memory device*	7196952		Issued	3/27/07
Method for fabricating a semiconductor memory cell*	7214587		Issued	5/8/07

Title:	Patent Number:	Application/ Serial Number:	Issued or Published?	Issued/Published Date:
Semiconductor memory component in cross-point architecture*	7215564		Issued	5/8/07
Resistive memory arrangement*	7215568		Issued	5/8/07
Pmc memory circuit and method for storing a datum in a pmc memory circuit*	7257014,		Issued	8/14/07
Integrated semiconductor memory with an arrangement of nonvolatile memory cells, and method*	7277312		Issued	10/2/07
Redundant column read in a memory array*	7296196		Issued	11/13/07
A memory device including electrical circuit configured to provide reversible bias across the pmc memory cell to perform erase and write functions*	7327603		Issued	2/5/08
Memory system and process for controlling a memory component to achieve different kinds of memory characteristics on one and the same memory component*	7337282		Issued	2/26/08
Read, write and erase circuit for programmable memory devices*	7359236		Issued	4/15/08
Method for fabricating a resistive memory*	7368314		Issued	5/6/08
Memory having cbram memory cells and method*	7372716		Issued	5/13/08
Channel discharging after erasing flash memory devices*	7397699		Issued	7/8/08
Programmable memory device circuit*	7426131		Issued	9/16/08
Resistively switching memory*	7442605		Issued	10/28/08
Method for preventing over-erasing of unused column redundant memory cells in a flash memory having single-transistor memory cells*	7457167		Issued	11/25/08
Method for improving the thermal characteristics of semiconductor memory cells*	7483293		Issued	1/27/09
Read, write and erase circuit for programmable memory devices*	7483294		Issued	1/27/09
Resistive memory element with shortened erase time*	7511294		Issued	3/31/09
Voltage reference circuit using programmable metallization cells*	7514706		Issued	4/7/09

Title:	Patent Number:	Application/ Serial Number:	Issued or Published?	Issued/Published Date:
Cbram cell and cbram array, and method of operating thereof*	7515454		Issued	4/7/09
Method and system for reducing soft-writing in a multi-level flash memory*	7522455		Issued	4/21/09
Integrated circuit including resistivity changing memory cells*	7538411		Issued	5/26/09
Implementation of column redundancy for a flash memory with a high write parallelism*	7551498		Issued	6/23/09
Resistive memory arrangement*	7561460		Issued	7/14/09
Memory cell, memory device and method for the production thereof*	7655939		Issued	2/2/10
Method for fabricating a solid electrolyte memory device and solid electrolyte memory device*	7658773		Issued	2/9/10
Method for fabricating an integrated device comprising a structure with a solid electrolyte*	7700398		Issued	4/20/10
A memory device including electrical circuit configured to provide reversible bias across the pmc memory cell to perform erase and write functions*	7715226		Issued	5/11/10
Method for manufacturing a cbram semiconductor memory*	7718537		Issued	5/18/10
Integrated circuit, method for manufacturing an integrated circuit memory cell array, memory module, and device*	7732888		Issued	6/8/10
Memory component with memory cells having changeable resistance and fabrication method therefor*	7737428		Issued	6/15/10
Nor and nad memory arrangement of resistive memory elements*	7746683		Issued	6/29/10
Method for manufacturing an integrated circuit including an electrolyte material layer*	7749805		Issued	7/6/10
Device and method for access time reduction by speculatively decoding non-memory read commands on a serial interface*	7769909		Issued	8/3/10
Solid electrolyte memory element and method for fabricating such a memory element*	7772614		Issued	8/10/10

Title:	Patent Number:	Application/ Serial Number:	Issued or Published?	Issued/Published Date:
Method for producing memory having a solid electrolyte material region*	7829134		Issued	11/9/10
Method of manufacturing an integrated circuit, an integrated circuit and a memory module*	7888228		Issued	2/15/11
Method and system to access memory*	7929356		Issued	4/19/11
Method for producing memory having a solid electrolyte material region*	8062694		Issued	11/22/11
Integrated circuits having programmable metallization cells (pmcs) and operating methods therefor*	8107273		Issued	1/31/12
Memory cells with an anode comprising intercalating material and metal species dispersed therein*	8115282		Issued	2/14/12
Method and system to access memory*	8208315		Issued	6/26/12
Methods of manufacturing a semiconductor device; method of manufacturing a memory cell, semiconductor device; semiconductor processing device, integrated circuit having a memory cell*	8268664		Issued	9/18/12
Variable impedance memory device having simultaneous program and erase, and corresponding methods and circuits*	8274842		Issued	9/25/12
Pmc-based non-volatile cam*	8320148		Issued	11/27/12
Humanized antibodies against the beta-amyloid peptide**	8323647		Issued	12/4/12
Reconfigurable memory arrays having programmable impedance elements and corresponding methods*	8331128		Issued	12/11/12
Methods of programming and erasing programmable metallization cells (pmcs)*	8369132		Issued	2/5/13
Memory cell device and method of manufacture*	8420481		Issued	4/16/13
Conducting bridge random access memory (cbram) device structures*	8426839		Issued	4/23/13
Methods and circuits for temperature varying write operations of programmable impedance elements*	8437171		Issued	5/7/13
Method for operating an integrated circuit having a resistivity changing memory cell*	8531863		Issued	9/10/13

Title:	Patent Number:	Application/ Serial Number:	Issued or Published?	Issued/Published Date:
Conductive filament based memory elements and methods with improved data retention and/or endurance*	8531867		Issued	9/10/13
Resistive switching element*		11746393	Published	5/9/07
Contact structure and method for variable impedance memory element*		13470286	Published	5/12/12
Resistive switching devices having alloyed electrodes and methods of formation thereof*		13558296	Published	7/25/12

*Shared ownership with Artemis Acquisition LLC
**Shared ownership with Artemis Acquisition LLC and University of Zurich, Prorektorat Forschung