TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

ETAS ID: TM322338

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
US Bank National Association, as collateral agent		11/03/2014	CORPORATION:

RECEIVING PARTY DATA

Name:	Vitesse Semiconductor Corporation
Street Address:	4721 Calle Carga
City:	Camarillo
State/Country:	CALIFORNIA
Postal Code:	93012
Entity Type:	CORPORATION: DELAWARE

PROPERTY NUMBERS Total: 22

Property Type	Number	Word Mark
Registration Number:	3004768	ACTIPHY
Registration Number:	2526300	FIBRETIMER
Registration Number:	3007582	FOCUS CONNECT
Registration Number:	2744204	IQ10G
Registration Number:	2661839	IQ2000
Registration Number:	2692482	IQ2200
Registration Number:	2706045	MONITOR 4.8
Registration Number:	2890481	PACKET EXCHANGE MATRIX
Registration Number:	2695611	SIMPLIPHY
Registration Number:	2761196	SIMPLIPIN I/0
Registration Number:	2850240	SUPER FEC
Registration Number:	2735775	TERASTREAM
Registration Number:	2487476	V
Registration Number:	2766449	VERIPHY
Registration Number:	1959483	VITESSE
Registration Number:	2682324	VITESSE
Serial Number:	77385769	VSCOPE
Registration Number:	2695613	MAGNIPHY
Registration Number:	2694410	MULTILINK

OP $565.00 3004768

Property Type	Number	Word Mark
Registration Number:	2697316	
Registration Number:	2697054	PACEMAKER
Registration Number:	2695612	UNIPHY

CORRESPONDENCE DATA

Fax Number: 8184446327

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 818-444-4527
Email: kchoi@stubbsalderton.com
Correspondent Name: Kirstin Choi
Address Line 1: 15260 Ventura Blvd. 20th Fl.
Address Line 2: Stubbs Alderton & Markiles
Address Line 4: Sherman Oaks, CALIFORNIA 91403

ATTORNEY DOCKET NUMBER:	VITESSE.06
NAME OF SUBMITTER:	Kirstin Choi
SIGNATURE:	/s/ Kirstin Choi
DATE SIGNED:	11/05/2014

Total Attachments: 10
source=Vitesse - Patent and Trademark Security Interest Termination (executed)#page1.tif
source=Vitesse - Patent and Trademark Security Interest Termination (executed)#page2.tif
source=Vitesse - Patent and Trademark Security Interest Termination (executed)#page3.tif
source=Vitesse - Patent and Trademark Security Interest Termination (executed)#page4.tif
source=Vitesse - Patent and Trademark Security Interest Termination (executed)#page5.tif
source=Vitesse - Patent and Trademark Security Interest Termination (executed)#page6.tif
source=Vitesse - Patent and Trademark Security Interest Termination (executed)#page7.tif
source=Vitesse - Patent and Trademark Security Interest Termination (executed)#page8.tif
source=Vitesse - Patent and Trademark Security Interest Termination (executed)#page9.tif
source=Vitesse - Patent and Trademark Security Interest Termination (executed)#page10.tif

TERMINATION OF
SECURITY INTEREST IN PATENTS AND TRADEMARKS

WHEREAS, Vitesse Semiconductor Corporation, a Delaware corporation (the "***Grantor***"), is the owner of record of (i) the patents and patent applications listed on the attached Schedule 1, now issued or pending in the United States Patent and Trademark Office (the "***Patents***") and (ii) the trademarks and trademark applications listed on the attached Schedule 2, now issued or pending in the United States Patent and Trademark Office (the "***Trademarks***");

WHEREAS, the Grantor entered into that certain Collateral Assignment (Intellectual Property), dated as of October 30, 2009 (the "***Collateral Assignment***"), in favor of US Bank National Association (the "***Collateral Agent***") as collateral agent for the trustee under the Indenture (defined below), a true and correct copy of which was recorded by the United States Patent and Trademark Office on November 5, 2009, at REEL/FRAME: 004091/0557, granting security interests in the Patents and the Trademarks to secure the Grantor's obligations under the Indenture;

WHEREAS, the Grantor's obligations under that certain Indenture, dated as of October 30, 2009 (the "Indenture"), between the Grantor and the Collateral Agent, as trustee, have been satisfied and discharged in all respects; and

WHEREAS, the Collateral Agent, on behalf of the Holders (as such term is defined in the Indenture), desires to (i) release its security interest in the Patents and the Trademarks and (ii) terminate the Collateral Assignment;

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, the Collateral Agent, on behalf of the Secured Parties, hereby:

1. Releases and reassigns to the Grantor any and all liens, security interests, right, title and interest of the Collateral Agent pursuant to the Collateral Assignment in (i) the patents and applications more fully described on Schedule 1 and (ii) the trademarks more fully described on Schedule 2 hereto, in each case without recourse or representation or warranty, express or implied; and

2. Authorizes and requests the Commissioner of Patents and Trademarks of the United States of America to note and record the existence of the release hereby given.

IN WITNESS WHEREOF, the Collateral Agent, on behalf of the Secured Parties, has caused this Termination of Security Interest in Patents and Trademarks to be signed as of this 3rd day of November, 2014.

U.S. BANK NATIONAL ASSOCIATION,
as Collateral Agent

By: Donald T. Hurrelbrink
Name: Donald T. Hurrelbrink
Title: Vice President

Schedule 1
Patents and Patent Applications

	Patent No.	Title	Issue Date
1	5,153,852	Static Ram Cell With High Speed And Improved Cell Stability	October 6, 1992
2	5,180,998	High Speed Logic Circuit	January 19, 1993
3	5,204,559	Method And Apparatus For Controlling Clock Skew	April 20, 1993
4	5,600,269	Digital Logic Protocol Interface For Different Semiconductor Technologies	February 4, 1997
5	5,694,070	Distributed Ramp Delay Generator	December 2, 1997
6	5,849,630	Process For Forming Ohmic Contact For III-V Semiconductor Devices	December 15, 1998
7	6,034,570	Gallium Arsenide Voltage-Controlled Oscillator And Oscillator Delay Cell	March 7, 2000
8	6,076,115	Media Access Control Receiver And Network Management System	June 13, 2000
9	6,076,194	Logic Gates For Reducing Power Consumption Of Gallium	June 20, 2000
10	6,084,478	Transimpedance Amplifier With Automatic Gain Control	July 4, 2000
11	6,085,248	Media Access Control Transmitter And Parallel Network Management System	July 4, 2000
12	6,108,713	Media Access Control Architectures And Network Management Systems	August 22, 2000
13	6,115,416	Pulse Code Sequence Analyzer	September 5, 2000
14	6,167,029	System And Method For Integrated Data Flow Control	December 26, 2000
15	6,172,990	Media Access Control Micro-Risc Stream Processor And Method For Implementing The Same	January 9, 2001
16	6,178,213	Adaptive Data Recovery System And Methods	January 23, 2001
17	6,204,733	Multiple-Phase-Interpolation LC Voltage-Controlled Oscillator	March 20, 2001

Schedule 1
Patents and Patent Applications

(cont'd)

	Patent No.	Title	Issue Date
18	6,218,905	Common-Gate Transimpedance Amplifier With Dynamically Controlled Input Impedance	April 17, 2001
19	6,223,242	Linearly Expandable Self-Routing Crossbar Switch	April 24, 2001
20	6,229,344	Phase Selection Circuit	May 8, 2001
21	6,229,367	Method And Apparatus For Generating A Time Delayed Signal With A Minimum Data Dependency Error Using An Oscillator	May 8, 2001
22	6,232,844	Oscillator Using A Phase Detector And Phase Shifter	May 15, 2001
23	6,263,034	Circuit And Technique For Digital Reduction Of Jitter	July 17, 2001
24	6,366,140	Method And Circuitry For High Speed Buffering Of Clocks Signals	April 2, 2002
25	6,377,575	High Speed Cross Point Switch Routing Circuit With Word-Synchronous Serial Back Plane	April 23, 2002
26	6,393,489	Media Access Control Architectures And Network Management Systems	May 21, 2002
27	6,462,590	High Bandwidth Clock Buffer	October 8, 2002
28	6,463,109	Multiple Channel Adaptive Data Recovery System	October 8, 2002
29	6,473,813	Module Based Address Translation Arrangement And Transaction Offloading In A Digital System	October 29, 2002
30	6,545,567	Programmable Analog Tapped Delay Line Filter Having Cascaded Differential Delay Cells	April 8, 2003
31	6,559,682	Dual-Mixer Loss Of Signal Detection Circuit	May 6, 2003
32	6,566,904	Pad Calibration Circuit With On-Chip Resistor	May 20, 2003
33	6,580,846	Actively-Controllable Optical Switches Based On Optical Position Sensing And Applications In Optical Switching Arrays	June 17, 2003
34	6,604,206	Reduced GMII With Internal Timing Compensation	August 5, 2003
35	6,605,958	Precision On-Chip Transmission Line Termination	August 12, 2003
36	6,633,191	Clock Buffer With DC Offset Suppression	October 14, 2003

Schedule 1
Patents and Patent Applications

(cont'd)

Patent No.		Title	Issue Date
37	6,633,605	Pulse Code Sequence Analyzer	October 14, 2003
38	6,665,347	Output Driver For High Speed Ethernet Transceiver	December 16, 2003
39	6,683,896	Method Of Controlling The Turn Off Characteristics Of A VCSEL Diode	January 27, 2004
40	6,694,476	Reed-Solomon Encoder And Decoder	February 17, 2004
41	6,700,886	High Speed Cross Point Switch Routing Circuit With Word-Synchronous Serial Back Plane	March 2, 2004
42	6,713,749	Monolithic Loss-Of-Signal Detect Circuitry	March 30, 2004
43	6,727,777	Apparatus And Method For Angles Coaxial To Planar Structure Broadband Transition	April 27, 2004
44	6,737,995	Clock and Data Recovery With A Feedback Loop To Adjust The Slice Level Of An Input Sampling Circuit	May 18, 2004
45	6,738,173	Limiting Amplifier Modulator Driver	May 18, 2004
46	6,738,922	Clock Recovery Unit Including A Frequency Detection	May 18, 2004
47	6,738,942	Product Code Based Forward Error Correction System	May 18, 2004
48	6,768,347	Precise Phase Detector	July 27, 2004
49	6,801,518	High Speed Cross Point Switch Routing Circuit With Word-Synchronous Serial Back Plane	October 5, 2004
50	6,810,499	Product Code Based Forward Error Correction System	October 26, 2004
51	6,833,743	Adjustment Of A Clock Duty Cycle	December 21, 2004
52	6,844,962	Actuator-Controlled Mirror With Z-Stop Mechanism	January 18, 2005
53	6,850,661	Multiple Element Controlled Optical Coupling	February 1, 2005
54	6,873,029	Self-Aligned Bipolar Transistor	March 29, 2005
55	6,904,061	Transparent Transport Overhead Mapping	June 7, 2005
56	6,925,216	Control-Techniques And Devices For An Optical Switch Array	August 2, 2005
57	6,933,793	Method Of Overtone Selection And Level Control In An Integrated Circuit CMOS Negative Resistance Oscillator To Achieve Low Jitter	August 23, 2005

Schedule 1
Patents and Patent Applications

(cont'd)

Patent No.		Title	Issue Date
58	6,946,948	Crosspoint Switch With Switch Matrix Module	September 20, 2005
59	6,948,109	Low-Density Parity Check Forward Error Correction	September 20, 2005
60	6,967,471	Switching Mode Regular For SFP Ethernet Adaptor	November 22, 2005
61	6,990,162	Scalable Clock Distribution For Multiple CRU On The Same Chip	January 24, 2006
62	6,996,202	Multiple Channel Adaptive Data Recovery System	February 7, 2006
63	6,998,292	Apparatus And Method For Interchip Or Chip-To-Substrate Connection With A Sub-Carrier	February 14, 2006
64	7,003,226	Method And Apparatus For Improved High-Speed Adaptive Equalization	February 21, 2006
65	7,119,611	On-Chip Calibrated Source Termination For Voltage Mode Driver and Method Of Calibration Thereof	October 10, 2006
66	7,123,678	RZ Recovery	October 17, 2006
67	7,132,849	Method And Apparatus For Configuring The Operation Of An Integrated Circuit	November 7, 2006
68	7,142,596	Integrated Circuit Implementation For Power And Area Efficient Adaptive Equalization	November 28, 2006
69	7,158,567	Method And Apparatus For Improved High-Speed FEC Adaptive Equalization	January 2, 2007
70	7,161,901	Automatic Load Balancing In Switch Fabrics	January 9, 2007
71	7,164,677	Data Switching System	January 16, 2007
72	7,200,176	Transformerless Ethernet Controller	April 3, 2007
73	7,227,678	Differential Opto-Electronics Transmitter	June 5, 2007
74	7,230,923	Time Based Packet Scheduling And Sorting System	June 12, 2007
75	7,231,008	Fast Locking Clock And Data Recovery Unit	June 12, 2007
76	7,236,084	Crosspoint Switch With Switch Matrix Module	June 26, 2007

Schedule 1
Patents and Patent Applications

(cont'd)

	Patent No.	Title	Issue Date
77	7,301,997	Method And Apparatus For Improved High-Speed Adaptive Equalization	November 27, 2007
78	7,305,190	Optical Dispersion Correction In Transimpedance Amplifiers	December 4, 2007
79	7,331,816	High-Speed Data Interface For Connecting Network Devices	February 19, 2008
80	7,340,662	GBIT/S Transceiver With Built-In Self Test Features	March 4, 2008
81	7,342,889	Means and a Method for Switching Data Packets or Frames	March 11, 2008
82	7,406,616	Data De-Skew Method and System	July 29, 2008
83	7,428,599	Method for Detecting Link Partner State During Auto Negotiation and Switching Local State to Establish Link	September 23, 2008
84	7,471,751	Power and Area Efficient Adaptive Equalization	December 30, 2008
85	7,486,686	Method and Apparatus for Scheduling Data on a Medium	February 3, 2009
86	7,516,897	Digital Automatic Power Control Loop For Continuous And Burst Mode Applications	April 14, 2009
87	7,545,817	Data Loop Port Acceleration Circuit	June 9, 2009

Schedule 1
Patents and Patent Applications

(cont'd)

Patent Title	Serial Number	Application Date
System And A Method For Processing Data Packets Or Frames	10/139338	05/07/02
Packet Forwarding Method And System	10/429267	05/02/03
Output Clock Adjustment For A Digital I/O Between Physical Layer Device And Media Access Controller	10/754204	01/09/04
Adaptive Equalization With Group Delay	11/029297	01/04/05
Variable Bandwidth Transimpedance Amplifier With One-Wire Interface	11/060061	02/16/05
Maintaining Filtering Database Consistency	11/508361	08/22/06

Patent Title	Serial Number	Application Date
Method And Apparatus For Improved High-Speed Adaptive Equalization	11/943569	11/20/07
Squelching A Recovered Clock In An Ethernet Network	12/029230	02/11/08
System And Method For Detecting Early Link Failure In An Ethernet Network	12/029195	02/11/08
Fuses For Memory Repair	12/207321	09/09/08
Digital Impedance Calibration Of Differential Voltage Mode	12/239418	09/26/08
Continuously Interleaved Error Correction	12/270774	11/13/08
Adaptive Data Recovery System With Input Signal Equalization	12/366544	2/5/2009

Schedule 2
Trademarks

Mark Name	Country	Class	Reg. # (or App. #)	Reg. Date (or Filing Date)
ACTIPHY	U.S.	009	3,004,768	10/4/2005
FIBRETIMER	U.S.	009	2,526,300	1/1/2002
FOCUS CONNECT	U.S.	009	3,007,382	10/18/2005
IQ10G	U.S.	009	2,744,204	7/29/2003
IQ2000	U.S.	009	2,681,839	12/17/2002
IQ2200	U.S.	009	2,692,462	3/4/2003
MONITOR 4.8	U.S.	009	2,706,045	4/15/2003
PACKET EXCHANGE MATRIX	U.S.	009	2,880,491	8/28/2004
SIMPLIPHY	U.S.	042	2,685,611	3/11/2003
SIMPLIPINIO	U.S.	042	2,781,198	9/9/2003
SUPER PEC	U.S.	009	2,850,240	6/8/2004
TERASTREAM	U.S.	009	2,735,775	7/15/2003
V (Stylized) 	U.S.	009	2,487,478	8/11/2001
VERIPHY	U.S.	042	2,786,449	9/23/2003
VITESSE	U.S.	009	1,959,483	3/5/1996

Mark Name	Country	Class	Reg. # (or App. #)	Reg. Date (or Filing Date)
VITESSE	U.S.	009 035 040 042	2,682,324	2/4/2003
VSCOPE	U.S.	009	77/385,760 (App. #)	1/31/2008 Filing Date

Schedule 2
Trademarks

(cont'd)

Mark Name	Country	Class	Reg. # (or App. #)	Reg. Date (or Filing Date)
MAGNIPHY	U.S.	042	2,895,613	3/11/2003
MULTILINK	U.S.	009	2,894,410	3/11/2003
MULTILINK Logo 	U.S.	009	2,897,316	3/18/2003

Mark Name	Country	Class	Reg. # (or App. #)	Reg. Date (or Filing Date)
PACEMAKER	U.S.	009	2,897,054	3/18/2003
UNIPHY	U.S.	042	2,895,612	3/11/2003