TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

ETAS ID: TM342305

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
Artemis Acquisition LLC		04/30/2015	LIMITED LIABILITY COMPANY: CALIFORNIA
Adesto Technologies Corporation		04/30/2015	CORPORATION: CALIFORNIA

RECEIVING PARTY DATA

Name:	Opus Bank
Street Address:	19900 MacArthur Boulevard, 12th Floor
City:	Irvine
State/Country:	CALIFORNIA
Postal Code:	92612
Entity Type:	Commercial bank: CALIFORNIA

PROPERTY NUMBERS Total: 7

Property Type	Number	Word Mark
Serial Number:	85532108	FLEXIRAM
Registration Number:	4303684	ADESTO TECHNOLOGIES
Registration Number:	4235215	CBRAM
Registration Number:	4193574	ADESTO
Registration Number:	3133677	RAPID8
Registration Number:	3114814	RAPIDS
Registration Number:	2164517	DATAFLASH

CH $190.00 85532108

CORRESPONDENCE DATA

Fax Number: 3122585600

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 312-258-5724
Email: cbollinger@schiffhardin.com
Correspondent Name: Chris L. Bollinger
Address Line 1: P.O. Box 06079
Address Line 2: Schiff Hardin LLp
Address Line 4: Chicago, ILLINOIS 60606-0079

ATTORNEY DOCKET NUMBER:	41907-0000
NAME OF SUBMITTER:	Chris L. Bollinger
SIGNATURE:	/Chris L. Bollinger/
DATE SIGNED:	05/22/2015

Total Attachments: 31

source=5-22 - Adesto IP Security Agreement#page1.tif
source=5-22 - Adesto IP Security Agreement#page2.tif
source=5-22 - Adesto IP Security Agreement#page3.tif
source=5-22 - Adesto IP Security Agreement#page4.tif
source=5-22 - Adesto IP Security Agreement#page5.tif
source=5-22 - Adesto IP Security Agreement#page6.tif
source=5-22 - Adesto IP Security Agreement#page7.tif
source=5-22 - Adesto IP Security Agreement#page8.tif
source=5-22 - Adesto IP Security Agreement#page9.tif
source=5-22 - Adesto IP Security Agreement#page10.tif
source=5-22 - Adesto IP Security Agreement#page11.tif
source=5-22 - Adesto IP Security Agreement#page12.tif
source=5-22 - Adesto IP Security Agreement#page13.tif
source=5-22 - Adesto IP Security Agreement#page14.tif
source=5-22 - Adesto IP Security Agreement#page15.tif
source=5-22 - Adesto IP Security Agreement#page16.tif
source=5-22 - Adesto IP Security Agreement#page17.tif
source=5-22 - Adesto IP Security Agreement#page18.tif
source=5-22 - Adesto IP Security Agreement#page19.tif
source=5-22 - Adesto IP Security Agreement#page20.tif
source=5-22 - Adesto IP Security Agreement#page21.tif
source=5-22 - Adesto IP Security Agreement#page22.tif
source=5-22 - Adesto IP Security Agreement#page23.tif
source=5-22 - Adesto IP Security Agreement#page24.tif
source=5-22 - Adesto IP Security Agreement#page25.tif
source=5-22 - Adesto IP Security Agreement#page26.tif
source=5-22 - Adesto IP Security Agreement#page27.tif
source=5-22 - Adesto IP Security Agreement#page28.tif
source=5-22 - Adesto IP Security Agreement#page29.tif
source=5-22 - Adesto IP Security Agreement#page30.tif
source=5-22 - Adesto IP Security Agreement#page31.tif

INTELLECTUAL PROPERTY SECURITY AGREEMENT

Dated as of April 30, 2015

From

ADESTO TECHNOLOGIES CORPORATION

and

ARTEMIS ACQUISITION LLC,
as Debtors,

to

OPUS BANK,
as Lender and Secured Party

INTELLECTUAL PROPERTY SECURITY AGREEMENT

THIS INTELLECTUAL PROPERTY SECURITY AGREEMENT ("IP Security Agreement") is made as of April 30, 2015 by and between **ADESTO TECHNOLOGIES CORPORATION**, a California corporation (*"Adesto"*), **ARTEMIS ACQUISITION LLC**, a California limited liability company (*"Artemis"*, and, together with Adesto, collectively, the "Debtor"), and **OPUS BANK**, a California commercial bank ("Opus" or "Lender") as Lender under that certain Credit Agreement of even date herewith among Debtors and Lender (the "Credit Agreement").

RECITALS

A. Concurrently herewith Debtor is entering into the Credit Agreement pursuant to which Lender shall provide Debtor with a senior term loan facility (the *"Facility"*).

B. It is a prerequisite to the Lender entering into the Credit Agreement that Debtor enters into this IP Security Agreement and grants to the Lender, the security interest hereafter provided to secure the Obligations.

C. Debtor as owner of the assets encumbered hereby, desires to enter into this IP Security Agreement to secure payment and performance of the Obligations.

AGREEMENT

NOW, THEREFORE, for good and valuable consideration, the receipt and adequacy of which is hereby acknowledged, the parties hereto agree as follows:

1. DEFINITIONS.

For purposes of this IP Security Agreement, the following terms shall have the meanings specified below. In addition terms not defined below that are defined in Division 8 or Division 9 of the UCC or in the Credit Agreement shall have the meaning specified therein.

1.1 Bankruptcy Code. The term "Bankruptcy Code" shall mean the Bankruptcy Reform Act of 1978 (11 U.S.C. § 101-1330) as amended and as hereafter modified.

1.2 Collateral. The term "Collateral" shall mean:

(a) The Intellectual Property Collateral;

(b) All Proceeds thereof; and

(c) All of the Debtor's Books relating thereto.

Notwithstanding the foregoing, the terms "Collateral" and "Intellectual Property Collateral" shall not include any General Intangibles of the Debtor (whether owned or held as licensee or lessee or otherwise) to the extent that the granting of a security interest therein would be contrary to applicable law or create a default under any agreement governing such property, right or license (but solely to the extent that such restrictions are enforceable as a matter of law).

1.3 Copyrights. The term "Copyrights" shall mean any and all copyright rights, copyright applications, copyright registrations and like protections in each work or authorship and derivative work thereof, whether published or unpublished and whether or not the same also constitutes a trade secret, now or hereafter existing, created, acquired or held, including without limitation those set forth on Exhibit A attached hereto, and all renewals of the foregoing.

1.4 Debtor's Books. The term "Debtor's Books" shall mean all of Debtor's books and records including, but not limited to: minute books; ledgers, records indicating, summarizing or evidencing Debtor's assets, liabilities, the Collateral, the Obligations, and all information relating thereto; records indicating, summarizing or evidencing Debtor's business operations or financial condition; and all computer programs, disc or tape files, printouts, runs, and other computer prepared information and the equipment containing such information.

1.5 Intentionally Omitted.

1.6 Event of Default. The term "Event of Default" shall have the meaning given to such term in Section 9 of this IP Security Agreement.

1.7 Intellectual Property Collateral. The term "Intellectual Property Collateral" shall mean all of the following assets now owned or hereafter acquired:

(a) Copyrights, Trademarks, Patents, and Mask Works;

(b) Licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works, and all license fees and royalties arising from such use to the extent permitted by such license or rights;

(c) Any and all trade secrets, and any and all intellectual property rights in computer software and computer software products now or hereafter existing, created, acquired or held;

(d) Any and all design rights which may be available to Debtor now or hereafter existing, created, acquired or held;

(e) Any and all claims for damages by way of past, present and future infringement of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above;

(f) All domain names of Debtor, including without limitation those listed on Exhibit D;

(g) All amendments, renewals and extensions of any of the Copyrights, Trademarks, Patents, or Mask Works;

(h) All contracts and contract rights relating to any of the foregoing; and

(i) All Proceeds of the foregoing.

1.8 IP Priority Liens. The term "IP Priority Liens" shall mean and refer to (i) Liens on any imbedded software in any equipment, the purchase price and related acquisition costs of such equipment which are financed by third-party lenders or lessors as permitted by the Credit Agreement; (ii) Liens in existence on the date any asset becomes Collateral, to the extent such Lien is Permitted by the Credit Agreement, subject to such Lien; (iii) Liens (including tax Liens) in favor of any Governmental Authority, which pursuant to the statute or law and other applicable law creating such Lien, have priority over Liens granted under this IP Security Agreement; (iv) the Liens set forth on Exhibit E hereto and (v) Liens permitted under Section 7.02(i) of the Credit Agreement and clauses (c), (d), (e), (i) and (k) of the definition of "Ordinary Course Liens" in the Credit Agreement.

1.9 IP Security Agreement. The term "IP Security Agreement" shall mean this IP Security Agreement (any concurrent or subsequent rider to this IP Security Agreement) and any extensions, supplements, amendments or modifications to this IP Security Agreement and/or to any such rider.

1.10 Lender Expenses. The term "Lender Expenses" means all costs and expenses incurred by Lender which are subject to payment or reimbursement by Debtor pursuant to Section 10.03 of the Credit Agreement.

1.11 Lender. The term "Lender" shall have the meaning given to such term in the preamble to this IP Security Agreement.

1.12 Licenses. The term "Licenses" shall mean all licenses or other rights to use any intellectual property rights, including any of the Copyrights, Patents, Trademarks, or Mask Works, and all license fees and royalties arising from such use to the extent permitted by such license or right.

1.13 License Disposition. The term "License Disposition" shall mean in respect of any Intellectual Property Collateral which is material to Debtor (the "Material IP") (i) the granting of an exclusive license across all or substantially all fields, uses or regions to any person or entity other than a majority-owned subsidiary of Debtor, (ii) the granting of any license that conveys directly or indirectly to any person or entity other than a majority-owned subsidiary of Debtor, all or substantially all of the economic value of such Material IP, or (iii) the abandonment by the Debtor of such Material IP.

1.14 Intentionally Omitted.

1.15 Intentionally Omitted.

1.16 Mask Works. The term "Mask Works" shall have the meaning provided in the Semiconductor Chip Protection Act of 1984 (17 U.S.C. §§ 901-914) and shall include, without limitation, all mask works or similar rights available for the protection of semiconductor chips, now owned or hereafter acquired, including, without limitation those set forth on Exhibit D attached hereto.

1.17 Obligations. The term "Obligations" shall have the meaning set forth in the Credit Agreement.

1.18 Patents. The term "Patents" shall mean all patents, industrial design registrations, utility models, and like protections and grants and applications for the foregoing, including, without limitation, improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the same, including without limitation the patents and patent applications set forth on Exhibit B attached hereto.

1.19 Proceeds. The term "Proceeds" shall have the meaning provided in the UCC including without limitation whatever is received upon the sale, lease, exchange, collection or other disposition of Collateral or proceeds, including, without limitation, proceeds of insurance covering the foregoing collateral, tax refunds, and any and all accounts, notes, instruments, chattel paper, equipment, money, deposit accounts, goods, or other tangible and intangible property of Debtor resulting from the sale or other disposition of the Collateral, and the proceeds thereof.

1.20 Trademarks. The term "Trademarks" shall mean any trademarks and servicemark rights, whether registered or not, applications to register and registrations of the same and like protections, and the entire goodwill of the business of Debtor connected with and symbolized by such trademarks, including without limitation those set forth on Exhibit C attached hereto.

1.21 UCC. The term "UCC" shall mean the California Uniform Commercial Code, as presently in force and effect and any replacements therefore as and when such replacements become effective.

2. GRANT OF SECURITY INTEREST.

As security for the prompt and complete payment and performance of all the Obligations, Debtor hereby grants to the Lender, a first priority security interest in all of Debtor's right, title and interest in, to and under the Collateral, subject to IP Priority Liens. Notwithstanding the foregoing, the security interest granted herein shall not extend to, and the term "Collateral" shall not include, any General Intangibles of the Debtor (whether owned or held as licensee or lessee or otherwise) to the extent that the granting of a security interest therein would be contrary to applicable law or create a default under any agreement governing such property, right or license (but only if such restrictions are enforceable as a matter of law).

3. AUTHORIZATION AND REQUEST.

Debtor authorizes and requests that the Register of Copyrights and the Commissioner of Patents and Trademarks record this IP Security Agreement or a version thereof.

4. REPRESENTATIONS AND WARRANTIES.

In addition to the representations and warranties of Debtor set forth in the Credit Agreement, which are incorporated herein by reference, Debtor represents and warrants, and represents to Lender that:

4.1 Incorporation: Place of Business. Adesto is a corporation validly existing and in good standing under the laws of the State of California; Artemis is limited liability company validly existing and in good standing under the laws of the State of California; and Debtor's chief executive office and principal place of business is located at 1250 Borregas Avenue, Sunnyvale, California 94089.

4.2 Title to Collateral. Except as specified on Schedule 4.2 hereto, Debtor has and at all times will have good, marketable and indefeasible title to the Collateral; except for any Intellectual Property Collateral which is being licensed by the Debtor or Collateral which is being leased by the Debtor, and as to such assets, Debtor has the appropriate rights to use such Collateral; the Collateral is and at all times shall remain free and clear of all Liens except for licenses granted by Debtor and except for IP Priority Liens.

4.3 Intellectual Property. All of Debtor's U.S. patents and patent applications, registered copyrights, applications for copyright registration, trademarks, service marks and trade names (whether registered or unregistered), and applications for registration of such trademarks, service marks and trade names, are set forth in Exhibits A, B and C. Debtor represents that none

of the Copyrights owned by it constitute a material asset of Debtor's business. All of Debtor's registered Mask Works are set forth in Exhibit D.

4.4 Domain Names. All of Debtor's domain names are set forth in Exhibit D.

4.5 No Conflict. Performance of this IP Security Agreement does not conflict with or result in a breach of any agreement relating to the intellectual property of Debtor, except to the extent that certain intellectual property agreements prohibit the assignment of the rights thereunder to a third party without the licensor's or other party's consent and this IP Security Agreement constitutes a security interest.

4.6 IP Enforceability. To Debtor's knowledge, each of the Patents is valid and enforceable, and no part of the Intellectual Property Collateral has been judged invalid or unenforceable, in whole or in part, and no claim has been made that any part of the Intellectual Property Collateral violates the rights of any third party.

4.7 Validity of Lien. This IP Security Agreement creates, and in the case of after acquired Intellectual Property Collateral, this IP Security Agreement will create at the time Debtor first has rights in such after acquired Intellectual Property Collateral, in favor of Lender a valid and perfected first priority security interest in the Intellectual Property Collateral in the United States securing the payment and performance of the Obligations which is senior to all other interests except for IP Priority Liens.

4.8 IP Registration. To its knowledge, except for, and upon, the filing with the United States Patent and Trademark office with respect to the Patents and Trademarks and the filing with the Register of Copyrights with respect to the Copyrights and Mask Works necessary to perfect the security interests created hereunder and except as been already made or obtained, no authorization, approval or other action by, and no notice to or filing with, any U.S. governmental authority of U.S. regulatory body is required either (i) for the grant by Debtor of the security interest granted hereby or for the execution, delivery or performance of this IP Security Agreement by Debtor in the U.S. or (ii) for the perfection in the United States or the exercise by Lender of its rights and remedies thereunder.

4.9 Complete. All information heretofore, herein or hereafter supplied to Lender by or on behalf of Debtor with respect to the Intellectual Property Collateral is accurate and complete in all material respects.

4.10 Continuing Warranties. Debtor's warranties and representations set forth in this Section 4 and in any exhibit hereto shall be true and correct at the time of execution of this IP Security Agreement by Debtor and at the time of any request for advance and at the time of any advance under the Credit Agreement.

4.11 Warranties and Representations Cumulative. The warranties, representations and agreements set forth herein shall be cumulative and in addition to any and all other warranties, representations and agreements which Debtor shall give, or cause to be given, to Lender, either now or hereafter.

5. COVENANTS.

So long as the Obligations, or any portion thereof, remains unsatisfied.

5.1 Change in Identity. Without prior notice to Lender, Debtor will not change Debtor's name, or state of incorporation; or relocate Debtor's principal place of business or chief executive office.

5.2 Intentionally Omitted.

5.3 Protection of IP. Debtor shall (i) protect, defend and maintain the validity and enforceability of the Intellectual Property Collateral that is material to the business of the Debtor, (ii) use commercially reasonable best efforts to detect infringements of the Intellectual Property Collateral that is material to the business of the Debtor and promptly advise Lender in writing of material infringements detected, and (iii) not allow any Intellectual Property Collateral to be abandoned, forfeited or dedicated to the public without the written consent of Lender, which shall not be unreasonably withheld, unless Debtor determines that reasonable business practices suggest that abandonment is appropriate.

5.4 Copyright Registration. Debtor shall promptly register the most recent version of any of Debtor's Copyrights, which are material to the business of Debtor, if not already so registered.

5.5 New IP Filings. If and when Debtor shall obtain rights to any new patents, trademarks, service marks, trade names or material copyrights, or otherwise acquire or become entitled to the benefit of, or apply for registration of, any of the foregoing that is material to the business of the Debtor, Debtor (i) shall promptly notify Lender thereof and (ii) hereby authorizes Lender to modify, amend, or supplement the schedules attached hereto to reflect such fact and from time to time to include any of the foregoing and make all necessary or appropriate filings with respect thereto and to perfect Lender 's Lien thereon.

5.6 Notice to Lender. Debtor shall promptly advise Lender of any material adverse change in the composition of the Collateral, including but not limited to any subsequent ownership right of the Debtor in or to any Trademark, Patent, Copyright, or Mask Work specified in this IP Security Agreement that is material to the business of the Debtor. Upon any executive officer of Debtor obtaining actual knowledge thereof, Debtor will promptly notify Lender in writing of any event that materially adversely affects the value of any material

Intellectual Property Collateral, the ability of Debtor to dispose of any material Intellectual Property Collateral or of the rights and remedies of Lender in relation thereto, including the levy of any legal process against any of the Intellectual Property Collateral.

5.7 Intentionally Omitted.

5.8 Intentionally Omitted.

5.9 Further Assurances. Debtor shall, from time to time, execute and file such other instruments, and take such further actions as Lender may reasonably request from time to time to perfect or continue the perfection of Lender's interest in the Intellectual Property Collateral.

6. LENDER'S RIGHTS TO COMPEL ACTION.

Lender shall have the right, but not the obligation, to take, at Debtor's sole expense, any actions that Debtor is required under this IP Security Agreement to take but which Debtor fails to take, after ten (10) days' written notice to Debtor. Debtor shall reimburse and indemnify Lender for all reasonable costs and reasonable expenses incurred in the reasonable exercise of its rights under this Section 6.

7. INSPECTION RIGHTS.

Not more often thane once per quarter unless an Event of Default exists, at any time during regular business hours and as often as reasonably requested upon reasonable notice, permit Lender, or any employee or representative thereof, to examine, audit and make copies and abstracts from Debtor's records and books of account, including quality control records, relating to the Collateral and to visit and inspect its properties related thereto, and, upon request, furnish promptly to Lender true copies of all financial information and internal management reports made available to their senior management related to the Collateral. Notwithstanding any provision of this Agreement to the contrary, so long as no Event of Default shall have occurred and be continuing, Debtor shall not be required to disclose, permit the inspection, examination, photocopying or making extracts of, or discuss, any document, information or other matter that (i) constitutes non-financial trade secrets or non-financial proprietary information, or (ii) the disclosure of which to Lender, or their designated representative, is then prohibited by law or any agreement binding on Debtor that was not entered into by Debtor for the purpose of concealing information from the Lender. Debtor shall, however, furnish to Lender such information concerning Debtor's Collateral as is reasonably necessary to permit Lender to perfect a security interest in such intellectual property; provided, however, nothing herein shall entitle Lender access to Debtor's trade secrets and other proprietary information.

8. FURTHER ASSURANCES: ATTORNEY IN FACT.

8.1 On a continuing basis, Debtor will, subject to any prior licenses, encumbrances and restrictions and prospective licenses, make, execute, acknowledge and deliver, and file and

record in the proper filing and recording places in the United States, all such instruments, including appropriate financing and continuation statements and collateral agreements and filings with the United States Patent and Trademark Office and the Register of Copyrights, and take all such action as reasonably requested by Lender, to perfect Lender's security interest in all Intellectual Property Collateral and otherwise to carry out the intent and purposes of this IP Security Agreement, or for assuring and confirming to Lender the grant or perfection of a security interest in all Intellectual Property Collateral.

8.2 Debtor hereby irrevocably (until the Obligations are paid in full) appoints Lender as Debtor's attorney-in-fact, with full authority in the place and stead of Debtor and in the name of Debtor, Lender or otherwise, from time to time in Lender's discretion, upon Debtor's failure or inability to do so, to take any action and to execute any instrument which Lender may deem necessary or advisable to accomplish the purposes of this IP Security Agreement, including:

(a) To modify, in its sole discretion, this IP Security Agreement without first obtaining Debtor's approval of or signature to such modification by amending Exhibit A, Exhibit B, Exhibit C, and Exhibit D hereof, as appropriate, to include reference to any right, title or interest in any Copyrights, Patents, Trademarks or Mask Works acquired by Debtor after the execution hereof or to delete any reference to any right, title or interest in any Copyrights, Patents, Trademarks, or Mask Works in which Debtor no longer has or claims any right, title or interest; and

(b) To file, in its sole discretion, one or more financing or continuation statements and amendments thereto, relative to any of the Intellectual Property Collateral without the signature of Debtor where permitted by law.

9. EVENTS OF DEFAULT.

The occurrence of any of the following shall constitute an Event of Default under this IP Security Agreement:

9.1 Breach of IP Security Agreement. (i) Any representation or warranty hereunder proves to have been incorrect in any material respect when made or deemed made, (ii) Debtor breaches any provision of this IP Security Agreement which cannot be cured, or (iii) the breach by Debtor of any other provision of this IP Security Agreement that remains uncured for a period of thirty (30) days.

9.2 Breach of Other Agreements. The occurrence and continuance of an Event of Default under the Credit Agreement as defined therein.

9.3 Lien Priority. Lender shall cease to have a valid and perfected first priority security interest upon any material item of the Collateral subject only to the IP Priority Liens.

9.4 Material Impairment. If there is a material impairment of the value of the Collateral.

9.5 Seizure of Assets. If all or any material item of Collateral is attached, seized, subjected to a writ or distress warrant, or are levied upon.

10. REMEDIES.

The exercise of remedies hereunder shall be made by Lender upon the terms and conditions contained herein. If an Event of Default shall have occurred and be continuing and not been cured or waived in accordance with the terms hereof or the Credit Agreement, Lender shall have the following rights and powers and may, at Lender's option, without notice of its election and without demand, to the extent permitted by Section 8.03 of the Credit Agreement, do any one or more of the following (in addition to the rights and remedies permitted under the Credit Agreement), all of which are authorized by Debtor:

10.1 UCC Rights. Lender shall have all of the rights and remedies of a secured party under the UCC and under all other applicable laws.

10.2 Intentionally Omitted.

10.3 Intentionally Omitted.

10.4 Protection of Collateral. Without notice to or demand upon Debtor or any guarantor, make such payments and do such acts as Lender considers necessary or reasonable to protect its security interest in the Collateral to pay, purchase, contest or compromise any encumbrance, charge or lien which in the opinion of Lender appears to be prior or superior to Lender's security interest and to pay all expenses incurred in connection therewith.

10.5 Assembly of Collateral. Lender may require Debtor to assemble the Collateral and make it available to Lender at a place designated by Lender.

10.6 Possession of Collateral. If an Event of Default exists, Lender, without a breach of the peace, may enter any of the premises of Debtor and search for, take possession of, remove, keep or store any or all of the Collateral. If Lender seeks to take possession of any or all of the Collateral by court process, Debtor irrevocably and unconditionally agrees that a receiver may be appointed by a court for such purpose without regard to the adequacy of the security for the Obligations. Lender shall have the right to remain on Debtor's premises or cause a custodian to remain thereon in exclusive control of such premises without charge for as long as Lender deems necessary in order to complete the enforcement of its rights under this IP Security Agreement. If Lender seeks possession of any or all of the Collateral by court process, Debtor irrevocably

waives (a) any bond and any surety or security relating thereto required by any statute, court rule or otherwise as an incident or condition to such possession; (b) any demand for possession prior to the commencement of any suit or action to recover possession; and (c) any requirement that Lender retain possession of and not dispose of such Collateral until after trial or final judgment.

10.7 License. Lender shall have a nonexclusive, royalty free license to use the Intellectual Property Collateral to the extent reasonably necessary to permit Lender to exercise its rights and remedies upon the occurrence of an Event of Default. All of Lender's rights and remedies with respect to the Intellectual Property Collateral shall be cumulative.

11. INDEMNITY.

Debtor agrees to defend, indemnify and hold harmless Lender and its officers, employees, and agents against: (a) all obligations, demands, claims, and liabilities claimed or asserted by any other party related to or in connection with the transactions contemplated by this IP Security Agreement or the Collateral, and (b) all losses or expenses in any way suffered, incurred, or paid by Lender as a result of or in any way arising out of, following or consequential to the transactions between Lender and Debtor under this IP Security Agreement or the Collateral (including without limitation, reasonable attorneys fees and reasonable expenses), except for losses arising from or out of Lender's gross negligence or willful misconduct.

12. GENERAL.

12.1 Taxes and Other Expenses Regarding the Collateral. If Debtor fails to pay promptly when due to any person or entity, monies which Debtor is required to pay by this IP Security Agreement, Lender may, but need not, pay the same and charge Debtor's account therefor, and Debtor shall promptly reimburse Lender therefor. Any payments made by Lender shall not constitute; (a) an agreement by Lender to make similar payments in the future, or (b) a waiver by Lender of any default under this IP Security Agreement. Lender need not inquire as to, or contest the validity of, any such expense, tax, security interest, encumbrance or lien and the receipt of the usual official notice for the payment thereof shall be conclusive evidence that the same was validly due and owing.

12.2 Notices. All notices, demands, or requests from one party to another shall, unless otherwise specified herein, be made in the manner set forth in the Credit Agreement.

12.3 Intentionally Omitted.

12.4 Release of Collateral. Lender shall promptly file UCC termination statements and any other documents or instruments as necessary upon any Disposition by Debtor of any items or item of Collateral, to the extent such Disposition is permitted under the Credit Agreement.

12.5 Termination. At such time as the Obligations are paid in full, this Agreement shall terminate and Lender shall execute and deliver to Debtor all instruments as may be necessary or proper to reinvest in Debtor full title to the property assigned hereunder, subject to any disposition thereof which may have been made by Lender pursuant hereto.

12.6 Course of Dealing. No course of dealing, nor any failure to exercise, nor any delay in exercising any right, power or privilege hereunder shall operate as a waiver thereof.

12.7 Intentionally Omitted.

12.8 Amendments. This IP Security Agreement may be amended only by a written instrument signed by both parties hereto.

12.9 Agreement Binding, Assignment. This IP Security Agreement shall be binding and deemed effective when executed by Debtor and Lender. This IP Security Agreement shall bind and inure to the benefit of the respective successors and assigns of each of the parties; provided, however, that Debtor may not assign this Security Agreement or any rights hereunder without Lender's prior written consent and any prohibited assignment shall be absolutely void. No consent to an assignment by Lender shall release Debtor from its obligations to Lender. Lender reserves the right to sell, assign, transfer, negotiate or grant participations in all or any part of, or any interest in, Lender's rights and benefits hereunder to the extent and in the manner provided for in Section 9.04 of the Credit Agreement. In connection therewith, Lender may disclose all documents and information that Lender now has or hereafter may have relating to Debtor or Debtor's business, subject to Debtor's reasonable confidentiality requirements.

12.10 Article and Section Headings. Article and section headings and article and section numbers have been set forth herein for convenience only. Unless the contrary is compelled by the context, everything contained in each article and section applies equally to this entire IP Security Agreement.

12.11 Construction. Neither this IP Security Agreement nor any uncertainty or ambiguity herein shall be construed or resolved against Lender or Debtor, whether under any rule of construction or otherwise. On the contrary, this IP Security Agreement has been reviewed by all parties and shall be construed and interpreted according to the ordinary meaning of the words used so as to fairly accomplish the purposes and intentions of all parties hereto.

12.12 Performance of Covenants. Debtor shall perform all of its covenants under this IP Security Agreement at its sole cost and expense.

12.13 Term. This IP Security Agreement shall continue in full force and effect as long as any of the Obligations are outstanding.

12.14 Conflict or Credit Agreement Modifications. To the extent that there is an explicit conflict between the terms of the Credit Agreement and this IP Security Agreement, the terms of the Credit Agreement shall control. Any future changes or modifications to the Credit Agreement, shall apply to and modify this IP Security Agreement, to the extent that such change or modification would reasonably be construed to apply to this IP Security Agreement.

12.15 Severability. Each provision of this IP Security Agreement shall be severable from every other provision of this IP Security Agreement for the purpose of determining the legal enforceability of any specific provision.

12.16 Successors. This IP Security Agreement shall be binding upon and inure to the benefit of Debtor and the Lender and their respective permitted successors and assigns.

12.17 Counterparts. This IP Security Agreement may be executed in two or more counterparts, each of which shall be deemed an original but all of which together shall constitute the same instrument.

13. CHOICE OF LAW AND VENUE.

The validity of this IP Security Agreement, its construction, interpretation and enforcement, and the rights of the parties hereunder and concerning the Collateral, shall be determined under, governed by and construed in accordance with the laws of the State of California. The parties agree that all actions or proceedings arising in connection with this Security Agreement shall be tried and litigated only in the state courts or federal courts located in the city and county of San Francisco, California.

[SIGNATURE PAGES FOLLOW]

IN WITNESS WHEREOF, the parties hereto have executed this IP Security Agreement on the day and year first above written.

ADESTO TECHNOLOGIES CORPORATION, a California corporation, as a Debtor

By: _____
Name:
Its: Narbeh Derhacobian
President & CEO

ARTEMIS ACQUISITION LLC, a California limited liability company, as a Borrower

By: Adesto Technologies Corporation, as sole member and manager of Artemis Acquisition LLC

By: _____
Name:
Its: Narbeh Derhacobian
President & CEO

OPUS BANK, as Lender

By: _____
Name:
Its:

IN WITNESS WHEREOF, the parties hereto have executed this IP Security Agreement on the day and year first above written.

ADESTO TECHNOLOGIES CORPORATION, a California corporation, as a Debtor

By: _____
Name:
Its:

ARTEMIS ACQUISITION LLC, a California limited liability company, as a Borrower

By: Adesto Technologies Corporation, as sole member and manager of Artemis Acquisition LLC

By: _____
Name:
Its:

OPUS BANK, as Lender

By: _____
Name: Kevin McBride
Its: Senior Managing Director

Exhibit "A" attached to that certain IP Security Agreement dated April 30, 2015.

EXHIBIT A
COPYRIGHTS

None.

Exhibit "B" attached to that certain IP Security Agreement dated April 30, 2015.

EXHIBIT B
PATENTS

Adesto Owned and Issued Patents

Adesto Ref	Document	Title	Published
Adesto-1001	US7442605	Resistively switching memory	10/28/2008
Adesto-1002	US7829134	Method for producing memory having a solid electrolyte material region	11/9/2010
Adesto-1002	US8062694	Method for producing memory having a solid electrolyte material region	11/22/2011
Adesto-1003	US7737428	Memory component with memory cells having changeable resistance and fabrication method therefor	6/15/2010
Adesto-1004	US7718537	Method for manufacturing a CBRAM semiconductor memory	5/18/2010
Adesto-1005	US7483293	Method for improving the thermal characteristics of semiconductor memory cells	1/27/2009
Adesto-1006	US7511294	Resistive memory element with shortened erase time	3/31/2009
Adesto-1007	US7749805	Method for manufacturing an integrated circuit including an electrolyte material layer	7/6/2010
Adesto-1008	US7772614	Solid electrolyte memory element and method for fabricating such a memory element	8/10/2010 Abandoned
Adesto-1010	US7700398	Method for fabricating an integrated device comprising a structure with a solid electrolyte	4/20/2010
Adesto-1011	US7215568	Resistive memory arrangement	5/8/2007
Adesto-1011	US7561460	Resistive memory arrangement	7/14/2009
Adesto-1012	US7746683	NOR and NAND memory arrangement of resistive memory elements	6/29/2010
Adesto-1013	US7538411	Integrated circuit including resistivity changing memory cells	5/26/2009
Adesto-1014	US7655939	Memory cell, memory device and method for the production thereof	2/2/2010
Adesto-1015	US8115282	MEMORY CELL DEVICE AND METHOD OF MANUFACTURE	2/14/2012
Adesto-1016	US7515454	CBRAM cell and CBRAM array, and method of operating thereof	4/7/2009

Adesto-1017	US7658773	Method for fabricating a solid electrolyte memory device and solid electrolyte memory device	2/9/2010
Adesto-1019	US7888228	Method of manufacturing an integrated circuit, an integrated circuit, and a memory module	2/15/2011
Adesto-1020	US7732888	Integrated circuit, method for manufacturing an integrated circuit, memory cell array, memory module, and device	6/8/2010
Adesto-1021	US6946882	Current sense amplifier	9/20/2005
Adesto-1022	US7214587	Method for fabricating a semiconductor memory cell	5/8/2007 Abandoned
Adesto-1023	US7215564	Semiconductor memory component in cross-point architecture	5/8/2007 Abandoned
Adesto-1024	US7257014	PMC memory circuit and method for storing a datum in a PMC memory circuit	8/14/2007
Adesto-1025	US7277312	Integrated semiconductor memory with an arrangement of nonvolatile memory cells, and method	10/2/2007
Adesto-1026	US7327603	Memory device including electrical circuit configured to provide reversible bias across the PMC memory cell to perform erase and write functions	2/5/2008
Adesto-1026	US7715226	Memory device including electrical circuit configured to provide reversible bias across the PMC memory cell to perform erase and write functions	5/11/2010
Adesto-1027	US7337282	Memory system and process for controlling a memory component to achieve different kinds of memory characteristics on one and the same memory component	2/26/2008
Adesto-1028	US7368314	Method for fabricating a resistive memory	5/6/2008
Adesto-1029	US7372716	Memory having CBRAM memory cells and method	5/13/2008
ADTO-00101	US8107273	Integrated circuits having programmable metallization cells (PMCs) and operating methods therefor	1/31/2012
ADTO-01200	US7359236	Read, write and erase circuit for programmable memory devices	4/15/2008
ADTO-01201	US7483294	Read, write, and erase circuit for programmable memory devices	1/27/2009
ADTO-01300	US7514706	Voltage reference circuit using programmable metallization cells	4/7/2009
ADTO-01400	US7426131	Programmable memory device circuit	9/16/2008
Adesto-1009	US8531863	Method for operating an integrated circuit having a resistivity changing memory cell	9/10/2013

Adesto-1015US_CON	US8952493	MEMORY CELL DEVICE AND METHOD OF MANUFACTURE	2/10/2015
Adesto-1015US_DIV	US8420481	Memory cell device and method of manufacture	4/16/2013
Adesto-1018	US8268664	Methods of manufacturing a semiconductor device; Method of manufacturing a memory cell; Semiconductor device; Semiconductor processing device; Integrated circuit having a memory cell	9/18/2012

Adesto-0001CON	METHODS OF PROGRAMMING AND ERASING PROGRAMMABLE METALLIZATION CELLS (PMCs)	8625331	7-Jan-14
Adesto-0001DIV	METHODS OF PROGRAMMING AND ERASING PROGRAMMABLE METALLIZATION CELLS (PMCs)	8369132	5-Feb-13
Adesto-0004	Variable impedance memory device having simultaneous program and erase, and corresponding methods and circuits	8274842	25-Sep-12
Adesto-0004DIV	VARIABLE IMPEDANCE MEMORY DEVICE BIASING CIRCUITS AND METHODS	8498164	30-Jul-13
Adesto-0008	Reconfigurable memory arrays having programmable impedance elements and corresponding methods	8331128	11-Dec-12
Adesto-0008/13CON	INTEGRATED CIRCUIT DEVICES AND SYSTEMS HAVING PROGRAMMABLE IMPEDANCE ELEMENTS WITH DIFFERENT RESPONSE TYPES	8675396	18-Mar-14
Adesto-0008/13CON2	APPLICATION OF RELAXATION VOLTAGE PULSES TO PROGRAMMABLE IMPEDANCE ELEMENTS DURING READ OPERATIONS	9007814	14-Apr-15
Adesto-0014	CONDUCTING BRIDGE RANDOM ACCESS MEMORY (CBRAM) DEVICE STRUCTURES	8426839	23-Apr-13
Adesto-0017B	VARIABLE IMPEDANCE MEMORY DEVICE STRUCTURE AND METHOD OF MANUFACTURE INCLUDING PROGRAMMABLE IMPEDANCE MEMORY CELLS AND METHODS OF FORMING THE SAME	8829482	9-Sep-14
Adesto-0026,0029,0030	METHODS AND CIRCUITS FOR TEMPERATURE VARYING WRITE OPERATIONS OF PROGRAMAMBLE IMPEDANCE ELEMENTS	8437171	7-May-13
Adesto-0026,0029,0030CON	CURRENT SOURCE CIRCUITS AND METHODS FOR MASS WRITE AND TESTING OF PROGRAMMABLE IMPEDANCE ELEMENTS	8947907	3-Feb-15

Adesto-0027	PROGRAMMABLE IMPEDANCE ELEMENT CIRCUITS AND METHODS	8294488	23-Oct-12
Adesto-0032	CIRCUITS HAVING PROGRAMMABLE IMPEDANCE ELEMENTS	8687403	1-Apr-14
Adesto-0034,0036,0037	CIRCUITS AND METHODS HAVING PROGRAMMABLE IMPEDANCE ELEMENTS	8947913	3-Feb-15
Adesto-0039, 40	READ METHODS, CIRCUITS AND SYSTEMS FOR MEMORY DEVICES	8654561	18-Feb-14
Adesto-0043	MEMORY DEVICES AND METHODS WITH IMPROVED READ OPERATIONS	8913444	16-Dec-14
Adesto-0044	MEMORY DEVICES, ARCHITECTURES AND METHODS FOR MEMORY ELEMENTS HAVING DYNAMIC CHANGE IN PROPERTY	8854873	7-Oct-14
Adesto-0047	PROGRAMMABLE MEMORY ELEMENTS, DEVICES AND METHODS HAVING PHYSICALLY LOCALIZED STRUCTURE	8895953	25-Nov-14
Adesto-0048	CONDUCTIVE FILAMENT BASED MEMORY ELEMENTS AND METHODS WITH IMPROVED DATA RETENTION AND/OR ENDURANCE	8531867	10-Sep-13
Adesto-0052	CONTACT STRUCTURE AND METHOD FOR VARIABLE IMPEDANCE MEMORY ELEMENT	8816314	26-Aug-14
Adesto-0054	ERASE AND SOFT PROGRAM WITHIN THE ERASE OPERATION FOR A HIGH SPEED RESISTIVE SWITCHING MEMORY OPERATION WITH CONTROLLED ERASED STATES	8659931	25-Feb-14
Adesto-0055	RESISTIVE SWITCHING DEVICES HAVING ALLOYED ELECTRODES AND METHODS OF FORMATION THEREOF	8847192	30-Sep-14
Adesto-0058	CBRAM/ReRAM WITH IMPROVED PROGRAM AND ERASE ALGORITHMS	8659954	25-Feb-14
Adesto-0063	MEMORY CELLS, DEVICES AND METHOD WITH DYNAMIC STORAGE ELEMENTS AND PROGRAMMABLE IMPEDANCE SHADOW ELEMENTS	8995173	31-Mar-15
Adesto-0064	PMC-BASED NON-VOLATILE CAM	8320148	27-Nov-12
Adesto-0064CON	PMC-BASED NON-VOLATILE CAM	8659926	25-Feb-14
Adesto-0068	CIRCUITS AND METHODS FOR PROGRAMMING VARIABLE IMPEDANCE ELEMENTS	8976568	10-Mar-15
Adesto-0073	VARIABLE IMPEDANCE MEMORY ELEMENT STRUCTURES, METHODS OF MANUFACTURE, AND MEMORY DEVICES CONTAINING THE SAME	8624219	7-Jan-14

Adesto-0075	PROGRAMMABLE IMPEDANCE MEMORY ELEMENTS, METHODS OF MANUFACTURE, AND MEMORY DEVICES CONTAINING THE SAME	8847191	30-Sep-14
Adesto-0075CON	PROGRAMMABLE IMPEDANCE MEMORY ELEMENTS WITH LATERALLY EXTENDING CELL STRUCTURE	8952351	10-Feb-15
Adesto-0076	CIRCUITS AND METHODS FOR PLACING PROGRAMMABLE IMPEDANCE MEMORY ELEMENTS IN HIGH IMPEDANCE STATES	8730752	20-May-14
Adesto-0077	Resistive switching devices and methods of formation thereof	8941089	27-Jan-15
Adesto-0085	MEMORY DEVICES, CIRCUITS AND, METHODS THAT APPLY DIFFERENT ELECTRICAL CONDITIONS IN ACCESS OPERATIONS	8982602	17-Mar-15
Adesto-0087	MEMORY DEVICES, CIRCUITS AND, METHODS THAT APPLY DIFFERENT ELECTRICAL CONDITIONS IN ACCESS OPERATIONS	8902631	2-Dec-14
Adesto-0090	Resistive Switching Memory	8912517	16-Dec-14
Adesto-0091	Resistive Switching Devices Having A Buffer Layer and Methods of Formation Thereof	8866122	21-Oct-14
Adesto-0095	SAFEGUARDING DATA THROUGH AN SMT PROCESS	9007808	14-Apr-15
Adesto-0097	Resistive Devices and Methods of Operation Thereof	8953362	10-Feb-15
Adesto-0098	Resistive Devices and Methods of Operation Thereof	9001553	7-Apr-15
Adesto-0108	Reverse program and erase cycling algorithms	8995167	31-Mar-15
Adesto-0109	Verify pulse delay to improve resistance window	9019745	28-Apr-15

Adesto Pending Patent Applications

Adesto Ref	Title	App No	App Date	Status
Adesto-0042	MEMORY DEVICES AND METHODS FOR READ AND WRITE OPERATIONS TO MEMORY ELEMENTS HAVING DYNAMIC CHANGE IN PROPERTY	13/408,367	29-Feb-2012	Allowed
Adesto-0048DIV	MEMORY ELEMENTS AND METHODS WITH IMPROVED DATA RETENTION AND/OR ENDURANCE	13/972,718	21-Aug-2013	Allowed
Adesto-0057	PROGRAMMABLE WINDOW OF OPERATION FOR CBRAM	13/548,429	13-Jul-2012	Allowed
Adesto-0065	Pre-conditioning circuits and methods for programmable impedance elements in memory devices	13/763,461	8-Feb-2013	Allowed
Adesto-0071	SOLID ELECTROLYTE MEMORY ELEMENTS WITH ELECTRODE INTERFACE FOR IMPROVED PERFORMANCE	13/850,267	25-Mar-2013	Allowed
Adesto-0078	Resistive Switching Memories	13/462,659	2-May-2012	Allowed
Adesto-0084	Triggered cell annihilation for resistive switching memory devices	13/859,853	10-Apr-2013	Allowed
Adesto-0102	Coding Techniques for Reducing Write Cycles for Memory	13/687,147	28-Nov-2012	Allowed
Adesto-0138	Resistive switching memory with diode select	14/256,123	18-Apr-2014	Allowed

Adesto-0008/13CON3	PROTOTYPING INTEGRATED CIRCUIT DEVICES WITH PROGRAMMABLE IMPEDANCE ELEMENTS	14/686,403	14-Apr-2015	Pending
Adesto-0014/16DIV	CONDUCTING BRIDGE RANDOM ACCESS MEMORY (CBRAM) DEVICE STRUCTURES AND FABRICATION METHODS	13/845,922	18-Mar-2013	Pending
Adesto-0019	PROGRAMMABLE IMPEDANCE ELEMENTS, METHODS OF FORMING ALL OR PORTIONS OF SUCH ELEMENTS, AND METHODS AND DEVICES THAT INCLUDE SUCH ELEMENTS	13/242,391	23-Sep-2011	Pending
Adesto-0020	PROGRAMMABLE IMPEDANCE DEVICES AND CELLS, AND METHODS THEREFOR	13/243,659	23-Sep-2011	Pending
Adesto-0027DIV	PROGRAMMABLE IMPEDANCE ELEMENT CIRCUITS AND METHODS	13/657,568	22-Oct-2012	Pending
Adesto-0032DIV	CIRCUITS HAVING PROGRAMMABLE IMPEDANCE ELEMENTS AND VERTICAL ACCESS DEVICES	14/231,729	31-Mar-2014	Pending
Adesto-0034DIV	CIRCUITS AND METHODS HAVING PROGRAMMABLE IMPEDANCE ELEMENTS	14/578,368	20-Dec-2014	Pending
Adesto-0041	MEMORY DEVICES AND METHODS HAVING DATA VALUES BASED ON DYNAMIC CHANGE IN MATERIAL PROPERTY	13/315,652	9-Dec-2011	Pending
Adesto-0043DIV	MEMORY DEVICES AND METHODS WITH IMPROVED READ OPERATIONS	14/572,646	16-Dec-2014	Pending
Adesto-0046	MEMORY DEVICES, ARCHITECTURES AND METHODS WITH DATA VALUES STORED IN MULTIPLE PROGRAMMABLE IMPEDANCE ELEMENTS	13/545,919	10-Jul-2012	Pending
Adesto-0067	RESISTIVE MEMORY DEVICES, CIRCUITS AND METHODS HAVING READ CURRENT LIMITING	13/336,642	23-Dec-2011	Pending
Adesto-0070	MEMORY DEVICES AND METHODS HAVING ADAPTABLE READ THRESHOLD LEVELS	13/851,011	26-Mar-2013	Pending
Adesto-0076CON	CIRCUITS AND METHODS FOR PLACING PROGRAMMABLE IMPEDANCE MEMORY ELEMENTS IN HIGH IMPEDANCE STATES	14/281,830	19-May-2014	Pending
Adesto-0079	Resistive Devices and Methods of Operation Thereof	13/470,030	11-May-2012	Pending
Adesto-0086	MULTI-PORT MEMORY DEVICES AND METHODS HAVING PROGRAMMABLE IMPEDANCE ELEMENTS	13/615,493	13-Sep-2012	Pending
Adesto-0088	MEMORY DEVICES AND METHODS HAVING WRITE DATA PERMUTATION FOR CELL WEAR REDUCTION	13/626,721	25-Sep-2012	Pending
Adesto-0089	SYSTEM ARCHITECTURE WITH MULTIPLE MEMORY TYPES, INCLUDING PROGRAMMABLE IMPEDANCE MEMORY ELEMENTS	13/846,539	18-Mar-2013	Pending
Adesto-0090DIV	Resistive Switching Memory	14/552,250	24-Nov-2014	Pending
Adesto-0096	Solid electrolyte materials and structures for memory device elements	13/691,425	30-Nov-2012	Pending
Adesto-0097CON	Resistive Devices and Methods of Operation Thereof	14/599,654	19-Jan-2015	Pending
Adesto-0106	NETWORK INTERFACE WITH LOGGING	13/716,357	17-Dec-2012	Pending
Adesto-0107	Two Terminal Resistive Access Devices and Methods of Formation Thereof	13/748,470	23-Jan-2013	Pending
Adesto-0109CON	Verify pulse delay to improve resistance window	14/663,719	20-Mar-2015	Pending
Adesto-0112	Storage elements, structures and methods having edgeless features for programmable layer(s)	13/830,315	14-Mar-2013	Pending
Adesto-0113	Latch circuits and methods with programmable impedance elements	14/176,123	9-Feb-2014	Pending
Adesto-0116	Resistive Switching Devices Having a Switching Layer And An Intermediate Electrode Layer and Methods of Formation Thereof	13/829,941	14-Mar-2013	Pending
Adesto-0117	NONVOLATILE MEMORY ELEMENTS HAVING CONDUCTIVE STRUCTURES WITH SEMIMETALS AND/OR SEMICONDUCTORS	14/217,256	17-Mar-2014	Pending
Adesto-0118	Sensing data in resistive switching memory devices	13/793,685	11-Mar-2013	Pending
Adesto-0120	Common plate switching reduction in resistive switching memory devices	13/909,983	4-Jun-2013	Pending
Adesto-0123	Programmable impedance memory elements and corresponding methods	14/195,787	3-Mar-2014	Pending
Adesto-0131	MEMORY DEVICE MAIN NONVOLATILE STORAGE AND BUFFER WITH NONVOLATILE OR QUASI-NONVOLATILE BACKUP	61/993,509	15-May-2014	Pending

Adesto-0133	Serial memory device alert of an external host to completion of an internally self-timed operation	14/516,261	16-Oct-2014	Pending
Adesto-0136,0144	Capacitor arrangements using a resistive switching memory cell structure	14/325,119	7-Jul-2014	Pending
Adesto-0139	Resistive switching memory device architecture for reduced cell damage during processing	14/265,548	30-Apr-2014	Pending
Adesto-0140	Cached memory structure and operation	14/665,831	23-Mar-2015	Pending
Adesto-0142	INTEGRATED CIRCUIT DEVICE WITH PROGRAMMABLE IMPEDANCE MEMORY CELL ARRAY AND RELATED METHODS	14/680,059	6-Apr-2015	Pending
Adesto-0145,0146	MEMORY CELLS WITH VERTICALLY INTEGRATED TUNNEL ACCESS DEVICE AND PROGRAMMABLE IMPEDANCE ELEMENT	14/530,460	31-Oct-2014	Pending
Adesto-0148	Resistive switching memory cell endurance improvement with redundant memory cell mapping	14/326,380	8-Jul-2014	Pending
Adesto-0149	Concurrent read and write operations in a serial flash device	62/021,840	8-Jul-2014	Pending
Adesto-0150	Support for improved SPI throughput in a serial Flash device	62/050,264	15-Sep-2014	Pending
Adesto-0153	CBRAM/RRAM cells utilizing cap layer to prevent oxygen contamination	62/061,124	7-Oct-2014	Pending
Adesto-0154	CBRAM/RRAM Device Anode Materials	62/095,026	21-Dec-2014	Pending
Adesto-0157	Re-erase Operation for Memory Devices with Programmable Impedance Devices	62/095,025	21-Dec-2014	Pending
Adesto-0158	Resistive switching memory with cell access by analog signal controlled transmission gate	14/628,280	22-Feb-2015	Pending

Patents and Patent Applications Acquired from Atmel Corporation

Application Title	Country	Application Number	Filing Date	Patent Number	Issue Date	Inventors
Method and System to Access Memory	US	12/205,518	05-Sep-2008	7,929,356	19-Apr-2011	DeCaro, Richard; Manea, Danut
Method and System to Access Memory	TW	98129756	03-Sep-2009			DeCaro, Richard; Manea, Danut
METHOD AND SYSTEM TO ACCESS MEMORY	CN	2009-100087964	04-Sep-2009			DeCaro, Richard; Manea, Danut
Method and System to Access Memory	US	13/052,810	21-Mar-2011	8,208,315	26-Jun-2012	DeCaro, Richard; Manea, Danut
Method and System for Reducing Soft-Writing in a Multi-Level Flash Memory	US	11/144,174	02-Jun-2005	7,522,455	21-Apr-2009	Oddone, Giorgio; Bartoli, Simone; Caser, Fabio T.; Bedarida, Lorenzo
Reference Cell for High Speed Sensing in Non-Volatile Memories	US	09/602,108	21-Jun-2000	6,411,549	25-Jun-2002 Abandoned	Pathak, Jagdish; Payne, James E; Pathak (S), Saroj
Reference Cell for High Speed Sensing in Non-Volatile Memories	CN	01801049.0	14-May-2001	ZL 01801049.0	04-May-2005 Abandoned	Pathak, Jagdish; Payne, James E; Pathak (S), Saroj
Reference Cell for High Speed Sensing in Non-Volatile Memories	TW	90114695	18-Jun-2001	NI-167346	03-Apr-2003	Pathak, Jagdish; Payne, James E; Pathak (S), Saroj

Low Power Voltage Regulator Circuit for Use in an Integrated Circuit Device	US	09/586,664	01-Jun-2000	6,320,454	20-Nov-2001	Kuo, Harry H; Payne, James E; Pathak (S), Saroj
Low Power Voltage Regulator Circuit for Use in an Integrated Circuit Device	TW	90112073	21-May-2001	NI-166239	18-Mar-2003	Kuo, Harry H; Payne, James E; Pathak (S), Saroj
Low Power Voltage Regulator Circuit for Use in an Integrated Circuit Device	CN	01810120.8	20-Apr-2001	ZL 01810120.8	08-Jun-2005	Kuo, Harry H; Payne, James E; Pathak (S), Saroj
Low Power Voltage Regulator Circuit for Use in an Integrated Circuit Device	DE	01 928 713.5	20-Apr-2001	1 301 982	02-Aug-2006	Kuo, Harry H; Payne, James E; Pathak (S), Saroj
Row Decoder Circuit for Use in Programming a Memory Device	US	10/174,632	18-Jun-2002	6,621,745	16-Sep-2003	Manea, Danut
Row Decoder Circuit for Use in Programming a Memory Device	TW	92112834	12-May-2003	NI-238417	21-Aug-2005	Manea, Danut
Row Decoder Circuit for Use in Programming a Memory Device	CN	03819561.5	14-Apr-2003	ZL 03819561.5	08-Oct-2008	Manea, Danut
Method of Programming a Multi-Level Memory Device	US	10/190,374	02-Jul-2002	6,714,448	30-Mar-2004	Manea, Danut
Method of Programming a Multi-Level Memory Device	TW	92113850	22-May-2003	NI-238532	21-Aug-2005	Manea, Danut
Method of Programming a Multi-Level Memory Device	CN	03820720.6	30-Apr-2003	ZL 03820720.6	20-Apr-2011	Manea, Danut
Method of Establishing Reference Levels for Sensing Multilevel Memory Cell States	US	10/211,437	02-Aug-2002	6,618,297	09-Sep-2003 Abandoned	Manea, Danut
Method of Recovering Overerased Bits in a Memory Device	US	10/235,265	04-Sep-2002	6,724,662	20-Apr-2004	Manea, Danut
Dual Stage Voltage Regulation Circuit	US	10/666,324	17-Sep-2003	7,064,529	20-Jun-2006 Abandoned	Telecco, Nicola
Method for Identification of SPI Compatible Serial Memory	US	10/284,597	30-Oct-2002	7,032,039	18-Apr-2006	DeCaro, Richard
Method for Identification of SPI Compatible Serial Memory	TW	92128993	20-Oct-2003	NI-289748	11-Nov-2007	DeCaro, Richard
Method for Identification of SPI Compatible Serial Memory	CN	03825730.0	25-Sep-2003	ZL 03825730.0	04-Apr-2007	DeCaro, Richard

Method and Apparatus of a Smart Decoding Scheme for Fast Synchronous Read in a Memory System	US	10/686,243	14-Oct-2003	7,143,257	28-Nov-2006 Abandoned	Schumann, Steven; Ching, Fai; Kowshik, Vikram
Functional Register Decoding System for Multiple Plane Operation	US	10/686,401	14-Oct-2003	7,099,226	29-Aug-2006 Abandoned	Yuan, Yolanda; Guo, Jason; Tsang, Sai; Kowshik, Vikram; Schumann, Steven
Approach for Zero Dummy Byte Flash Memory Read Operation	US	10/929,899	30-Aug-2004	6,879,535	12-Apr-2005	Perisetty, Srinivas
Redundant Column Read in a Memory Array	US	11/131,017	17-May-2005	7,296,196	13-Nov-2007 Abandoned	Perisetty, Srinivas
Channel Discharging After Erasing Flash Memory Devices	US	11/190,722	27-Jul-2005	7,397,699	08-Jul-2008	Trinh, Stephen P
Column/Sector Redundancy CAM Fast Programming Scheme Using Regular Memory Core Array in Mulit-Plane Flash Memory Device	US	11/295,878	07-Dec-2005	7,196,952	27-Mar-2007 Abandoned	Trinh, Stephen P
A Method For Preventing Over-Erasing of Unused Redundt Memory Cells in a Flash Memory Having Single-Transistor Memory Cells	US	11/553,393	26-Oct-2006	7,457,167	25-Nov-2008	Patrascu, Dinu; Ho, On-Pong R.; Kuo (W), Wei-Yen
Device and Method for Access Time Reduction by Speculatively Decoding Non-Memory Read Commands on a Serial Interface	US	11/566,555	04-Dec-2006	7,769,909	03-Aug-2010	Ho, On-Pong R.; Nguyen, Dixie; Patrascu, Dinu
A New Implementation of Column Redundancy for a Flash Memory With a High Write Parallelism	US	11/611,452	15-Dec-2006	7,551,498	23-Jun-2009	Bartoli, Simone; Surico, Stefano; Sacco, Andrea; Mostola, Maria
A New Implementation of Column Redundancy for a Flash Memory With a High Write Parallelism	TW	096143993	20-Nov-2007	NI-457933	21-Oct-2014	Bartoli, Simone; Surico, Stefano; Sacco, Andrea; Mostola, Maria
A New Implementation of Column Redundancy for a Flash Memory With a High Write Parallelism	CN	2007-80046296.9	3-Nov-2007	ZL 200780046296.9	4-Apr-2013	Bartoli, Simone; Surico, Stefano; Sacco, Andrea; Mostola, Maria

Ultra-Deep Power-Down Mode for Memory Devices	US	13/559,320	26-Jul-2012			DeCaro, Richard, Manea, Danut, Wang, Yongliang, Trinh, Stephen; Hill, Paul

Exhibit "C" attached to that certain IP Security Agreement dated April 30, 2015.

EXHIBIT C
TRADEMARKS

Trademark	Ctry	App. Num.	Reg. Num.	Status
FLEXIRAM	USA	85532108		(Abandoned Jan 2013)– Not in use in commerce.
ADESTO TECHNOLOGIES adesto TECHNOLOGIES	USA	85470629	[redacted]	REGISTERED
CBRAM®	USA	85470550	[redacted]	REGISTERED
ADESTO	USA	85470695	4193574	REGISTERED
RAPID8	USA	78210348	3133677	REGISTERED (Not in use)
RAPIDS	USA	78210343	3114814	REGISTERED
DATAFLASH	USA	75121234	2164517	REGISTERED

Exhibit "D" attached to that certain IP Security Agreement dated April 30, 2015.

EXHIBIT D
DOMAIN NAMES; MASK WORKS[1]

Adesto has purchased the domain name registration for the following domain name:

adestotech.com
adestotech.net
adestotech.org
adestotech.info
resistiveram.com
resistive-ram.com
reram-forum.com
.

[1] Borrowers: Please update this as necessary.

Exhibit "E" attached to that certain IP Security Agreement dated April 30, 2015.

EXHIBIT E

The following is a list of liens on the Collateral as permitted under Section 1.8 of the IP Security Agreement:

Equipment lien pursuant to Master Lease Agreement No. ADESX by and between Adesto and ATEL Ventures, Inc. dated as of January 23, 2008, as amended.

Equipment lien pursuant to Equipment Lease Agreement by and between Adesto and De Lage Landen Financial Services, Inc. dated as of July 8, 2011, as amended.

Equipment lien pursuant to Equipment Lease Agreement by and between Adesto and Cisco Systems Capital Corporation dated June 28, 2011, as amended.

SCHEDULE 4.2

Reference is made to the liens set forth on Exhibit E.

41907-0000
CH2\16531098.3