# TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

ETAS ID: TM354585

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| **SUBMISSION TYPE:** | NEW ASSIGNMENT |
| **NATURE OF CONVEYANCE:** | RELEASE OF SECURITY INTEREST |

**CONVEYING PARTY DATA**

| Name | Formerly | Execution Date | Entity Type |
|---|---|---|---|
| Silicon Valley Bank | | 08/25/2015 | CORPORATION: |

**RECEIVING PARTY DATA**

| | |
|---|---|
| **Name:** | Atrenta Inc. |
| **Street Address:** | 2077 GATEWAY PL |
| **City:** | San Jose |
| **State/Country:** | CALIFORNIA |
| **Postal Code:** | 95110 |
| **Entity Type:** | CORPORATION: DELAWARE |

**PROPERTY NUMBERS Total: 21**

| Property Type | Number | Word Mark |
|---|---|---|
| **Registration Number:** | 2603761 | SPYGLASS |
| **Registration Number:** | 2762455 | ATRENTA |
| **Registration Number:** | 2778737 | SPYGLASS PREDICTIVE ANALYZER |
| **Registration Number:** | 3230954 | 1TEAM |
| **Registration Number:** | 3256970 | 1TEAM:EMBEDDED |
| **Registration Number:** | 3304662 | EARLY DESIGN CLOSURE |
| **Registration Number:** | 4105992 | GENSYS |
| **Registration Number:** | 4636973 | BUGSCOPE |
| **Registration Number:** | 4682935 | MARS |
| **Serial Number:** | 78726061 | 1TEAM:SPYGLASS |
| **Serial Number:** | 78726104 | 1TEAM:ANALYZE SPYGLASS |
| **Serial Number:** | 78579382 | FUTURE PERFECT |
| **Registration Number:** | 3230964 | ATRENTA |
| **Serial Number:** | 78572528 | 1TEAM:ANALYZE |
| **Serial Number:** | 78572545 | 1TEAM:VERIFY |
| **Registration Number:** | 3160627 | 1TEAM:IMPLEMENT |
| **Registration Number:** | 3046985 | PERISCOPE |
| **Serial Number:** | 78394711 | BLUEPRINT |
| **Serial Number:** | 78168426 | ACTIVESPEC |

CH $540.00 2603761

| Property Type | Number | Word Mark |
|---|---|---|
| **Registration Number:** | 2799296 | ATRENTA THE PREDICTIVE ANALYSIS COMPANY |
| **Registration Number:** | 2451460 | SURVEYOR |

**CORRESPONDENCE DATA**

**Fax Number:** 6508023007

***Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.***

**Phone:** 6508023000
**Email:** brian.lee@weil.com
**Correspondent Name:** Ryne Saxe
**Address Line 1:** Weil, Gotshal & Manges LLP
**Address Line 4:** Redwood Shores, CALIFORNIA 94065

| | |
|---|---|
| **ATTORNEY DOCKET NUMBER:** | 76789.0016/R. SAXE |
| **NAME OF SUBMITTER:** | Ryne Saxe |
| **SIGNATURE:** | /Ryne Saxe/ |
| **DATE SIGNED:** | 09/10/2015 |

**Total Attachments: 12**
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# RELEASE OF INTELLECTUAL PROPERTY SECURITY INTEREST

This **RELEASE OF INTELLECTUAL PROPERTY SECURITY INTEREST**, dated as of the date of the signature page hereto (this "**Release**"), is made by **SILICON VALLEY BANK,** a California corporation (the "**Lender**"), in favor of **ATRENTA INC.,** a Delaware corporation (the "**Grantor**").

All capitalized terms used but not otherwise defined herein have the meanings given to them in the Loan and Security Agreement or the Intellectual Property Security Agreement (each as defined below).

## W I T N E S S E T H

**WHEREAS**, Lender and Grantor are parties to that certain Amended and Restated Loan and Security Agreement, dated as of June 26, 2014 (as amended, restated, supplemented or otherwise modified, the "**Loan and Security Agreement**") and Intellectual Property Security Agreement, dated as of April 14, 2009 (as amended, restated, supplemented or otherwise modified (including Addendum to Intellectual Property Security Agreement, dated October 12, 2010, Addendum to Intellectual Property Security Agreement, dated June 12, 2012, and Addendum to Intellectual Property Security Agreement, dated May 5, 2014), the "**Intellectual Property Security Agreement**").

**WHEREAS**, pursuant to the Loan and Security Agreement, Grantor granted Lender a security interest in certain collateral.

**WHEREAS**, pursuant to the Intellectual Property Security Agreement, Grantor granted Lender a security interest in the Intellectual Property Collateral (as defined in the Intellectual Property Security Agreement) in conjunction with the security interest granted pursuant to the Loan and Security Agreement.

**WHEREAS**, Lender and Grantor desire that Lender terminate and release Lender's security interest in all right, title and interest of Grantor in, to and under any and all intellectual property, intellectual property rights and proprietary rights throughout the world (whether registered or unregistered) and corresponding goodwill and other rights of Grantor, including all Intellectual Property Collateral (as defined in the Intellectual Property Security Agreement), General Intangibles, Intellectual Property (each as defined in the Loan and Security Agreement), Copyrights, Patents (including the patents, provisionals and patent applications set forth on Schedule A hereto), Trademarks (including the trademarks and trademark applications set forth on Schedule B hereto), Mask Works (each as defined in the Intellectual Property Security Agreement), websites, and domain names (collectively, the "**Released Intellectual Property Collateral**").

**NOW, THEREFORE**, in consideration of the premises and for other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged:

Lender hereby terminates, releases and discharges fully, without representation, warranty or recourse, Lender's security interest in all right, title and interest of the Grantor in, to

and under all of the Released Intellectual Property Collateral, and reassigns and transfers any right, title and interest that Lender may have in, to and under all of the foregoing to the Grantor.

Lender hereby authorizes the Grantor, or the Grantor's authorized representative, to record this Release with the United States Patent and Trademark Office, the United States Copyright Office, any similar office or agency of the United States, any state thereof, any other country or any political subdivision thereof, or any applicable office or agency thereof.

Lender agrees to execute all documents and take all actions reasonably requested by the Grantor (at the sole cost and expense of the Grantor) to (a) terminate, release and discharge fully, without representation, warranty or recourse, Lender's security interest in all right, title and interest of the Grantor in, to and under all of the Released Intellectual Property Collateral, (b) reassign and transfer any right, title and interest that Lender may have in the Released Intellectual Property Collateral to the Grantor and (c) perfect, register or record the rights of the Grantor to the Released Intellectual Property Collateral.

This Release may be executed in counterparts, each of which when executed will be deemed to be an original but all of which taken together will constitute one and the same agreement. The words "include", "including" and variations thereof will be deemed to be followed by the words "without limitation". The use of "or" will not be deemed to be exclusive.

THIS RELEASE AND THE RIGHTS AND OBLIGATIONS OF THE PARTIES HEREUNDER SHALL BE GOVERNED BY, AND SHALL BE CONSTRUED AND ENFORCED IN ACCORDANCE WITH, THE INTERNAL LAWS OF THE STATE OF CALIFORNIA, WITHOUT REGARD TO CONFLICTS OF LAWS PRINCIPLES.

[*Signature page follows*]

**IN WITNESS WHEREOF**, the parties have executed this Release as of the date written below.

Made this 25 day of August 2015.

**SILICON VALLEY BANK**

By: _____

Name: Reisa Bubic

Title: VP

**ATRENTA INC.**

By: _____

Name: ERIKA VARGA MCENROE

Title: DIRECTOR

[SIGNATURE PAGE TO RELEASE OF INTELLECTUAL PROPERTY SECURITY INTEREST]

## SCHEDULE A

## Patents, Provisionals and Patent Applications

| | Patent Title | Jurisdiction | Application (Provisional) Number | Application (Provisional) Date | Patent Number | Patent Date |
|---|---|---|---|---|---|---|
| 1. | An Apparatus and Method for Handling of Multi-Level Circuit Design Data | United States | 10/118,242 | 9-Apr-2002 | 6993733 | 31-Jan-2006 |
| 2. | A Method for Determining Fault Coverage from RTL Description | United States | 10/217,535 | 14-Aug-2002 | 6876934 | 5-Apr-2005 |
| 3. | Identification And Implementation Of Clock Gating In The Design Of Integrated Circuits | United States | 10/631,755 | 1-Aug-2003 | 7076748 | 11-Jul-2006 |
| 4. | Method For Clock Synchronization Validation In Integrated Circuit Design | United States | 10/695,803 | 30-Oct-2003 | 7073146 | 4-Jul-2006 |
| 5. | A Method, System, and Computer Program Product for Automatic Insertion and Correctness Verification of Level Shifters in Integrated Circuits with Multiple Voltage Domains | United States | 10/711,971 | 15-Oct-2004 | 7152216 | 19-Dec-2006 |
| 6. | Pattern Recognition in an Integrated Circuit Design | United States | 10/783,091 (60/452,970) | 23-Feb-2004 (10-Mar-2003) | 7216321 | 8-May-2007 |
| 7. | A Method for Detecting Bus Contention from RTL Description | United States | 10/172,996 | 18-Jun-2002 | 7277840 | 2-Oct-2007 |
| 8. | Method, System And Computer Program Product For Generating And Verifying Isolation Logic Modules In Design Of Integrated Circuits | United States | 10/711493 | 21-Sep-2004 | 7349835 | 25-Mar-2008 |
| 9. | A Chip Development System Enabled for the Handling of Multi-Level Circuit Design Data | United States | 11/260225 | 28-Oct-2005 | 7421670 | 2-Sep-2008 |
| 10. | Bus Representation For Efficient Physical Synthesis Of Integrated Circuit Designs | United States | 11/423,919 (60/689,545) | 13-Jun-2006 (13-Jun-2005) | 7451427 | 11-Nov-2008 |

| | Patent Title | Jurisdiction | Application (Provisional) Number | Application (Provisional) Date | Patent Number | Patent Date |
|---|---|---|---|---|---|---|
| 11. | Method For Clock Synchronization Validation In Integrated Circuit Designs | United States | 11/276,819 | 15-Mar-2006 | 7506292 | 17-Mar-2009 |
| 12. | Method For Recognizing And Verifying FIFO Structures In Integrated Circuit Designs | United States | 11/426936 | 27-Jun-2006 | 7536662 | 19-May-2009 |
| 13. | A Method for Optimization of Clock Gating in Integrated Circuit Designs | United States | 11/419,624 | 22-May-2006 | 7546559 | 9-Jun-2009 |
| 14. | A Method For Modeling And Verifying Timing Exceptions | United States | 11/749,090 | 15-May-2007 | 7650581 | 19-Jan-2010 |
| 15. | A Method, System, and Computer Program Product for Generating and Verifying Isolation Logic Modules in Design of Integrated Circuits | United States | 11/959,427 | 28-Nov-2007 | 7712061 | 4-May-2010 |
| 16. | A Method For Checking Constraints Equivalence Of An Integrated Circuit Design | United States | 11/755,764 | 31-May-2007 | 7882483 | 1-Feb-2011 |
| 17. | Method For Computing Power Savings And Determining The Preferred Clock Gating Circuit Of An Integrated Circuit Design | United States | 11/837,174 | 10-Aug-2007 | 7941679 | 10-May-2011 |
| 18. | A Method For Compaction Of Timing Exception Paths | United States | 12/206,473 | 8-Sep-2008 | 8042085 | 18-Oct-2011 |
| 19. | Methods for Automatically Generating Assertions | United States | 11/672,919 | 8-Feb-2007 | 7926020 | 12-Apr-2011 |
| 20. | Method and System For Circuit Equivalence Checking | United States | 12/785,986 | 24-May-2010 | 8285527 | 9-Oct-2012 |
| 21. | Systems and Methods for Generating Predicates and Assertions | United States | 12/649,144 | 29-Dec-2009 | 8326778 | 4-Dec-2012 |
| 22. | A Method and System Thereof for Optimization of Power Consumption of Scan Chains of an Integrated Circuit for Test | United States | 12/910,510 (61/279,603) | 21-Oct-2010 (23-Oct-2009) | 8423843 | 16-Apr-2013 |

| | Patent Title | Jurisdiction | Application (Provisional) Number | Application (Provisional) Date | Patent Number | Patent Date |
|---|---|---|---|---|---|---|
| 23. | System And Method For Metastability Verification Of Circuits Of An Integrated Circuit | United States | 12/986,644 | 7-Jan-2011 | 8448111 | 21-May-2013 |
| 24. | A Method For Generating An Integrated And Unified View Of Ip-Cores For Hierarchical Analysis Of A System On Chip (SOC) Design | United States | 13/645,897 | 5-Oct-2012 | 8533647 | 10-Sep-2013 |
| 25. | An Apparatus And Method Thereof For Hybrid Timing Exception Verification Of An Integrated Circuit Design | United States | 13/209,702 (61,373,511) | 15-Aug-2011 (13-Aug-2010) | 8560988 | 15-Oct-2013 |
| 26. | A System and Method for Inferring Higher Level Descriptions from RTL Topology Based on Naming Similarities, and Dependency. | United States | 13/433,395 (61/587,367) | 29-Mar-2012 (17-Jan-2012) | 8589835 | 19-Nov-2013 |
| 27. | Hierarchical Bottom-Up Clock Domain Crossing Verification | United States | 13/416,856 | 9-Mar-2012 | 8607173 | 10-Dec-2013 |
| 28. | System And Method For Strengthening Of A Circuit Element To Reduce An Integrated Circuit's Power Consumption | United States | 13/828709 | 14-Mar-2013 | 8635578 | 21-Jan-2014 |
| 29. | A System and Methods for Inferring Higher Level Descriptions from RTL Topology Based on Connectivity Propagation | United States | 13/532,175 (61/639,099) | 25-Jun-2012 (27-Apr-2012) | 8656335 | 18-Feb-2014 |
| 30. | Sequential clock gating using net activity and XOR technique on semiconductor designs including already gated pipeline design | United States | 13/766017 | 13-Feb-2013 | 8656326 | 18-Feb-2014 |
| 31. | System and Method for Abstraction of a Circuit Portion of an Integrated Circuit | United States | 13/791,492 | 8-Mar-2013 | 8656328 | 18-Feb-2014 |

| | Patent Title | Jurisdiction | Application (Provisional) Number | Application (Provisional) Date | Patent Number | Patent Date |
|---|---|---|---|---|---|---|
| 32. | Sequential Clock Gating using Net Activity and XOR Technique on Semiconductor Designs including Already Gated Pipeline Design | United States | 14/083,109 | 18-Nov-2013 | 8677295 | 18-Mar-2014 |
| 33. | A Method and System Thereof for Optimization of Power Consumption of Scan Chains of an Integrated Circuit for Test | United States | 13/847,938 | 20-Mar-2013 | 8756466 | 17-Jun-2014 |
| 34. | System and Method for Large Multiplexer Identification and Creation in a Design of an Integrated Circuit | United States | 13/756,083 | 31-Jan-2013 | 8739087 | 27-May-2014 |
| 35. | Computer aided Design System and Methods for Merging Design Constraint Files across Operational Modes | United States | 13/178,607 | 8-Jul-2011 | 8775989 | 8-Jul-2014 |
| 36. | Method For Creating Physical Connections In 3d Integrated Circuits | United States | 14/012,734 (61/780,526) | 28-Aug-2013 (13-Mar-2013) | 8732647 | 20-May-2014 |
| 37. | Systems and Methods for Generating a Higher Level Description of a Circuit Design Based on Connectivity Strengths | United States | 13/683,287 (61/677,334) | 21-Nov-2012 (30-Jul-2012) | 8782587 | 15-Jul-2014 |
| 38. | An Efficient Apparatus and Method for Analysis of RTL Structures that Cause Physical Congestion | United States | 13/952,024 (61/780,986) | 26-Jul-2013 (14-Mar-2013) | 8745567 | 3-Jun-2014 |
| 39. | An efficient method to analyze RTL structures that cause physical implementation issues based on rule checking and overlap analysis | United States | 13/954,097 (61/780,488) | 30-Jul-2013 (13-Mar-2013) | 8782582 | 15-Jul-2014 |
| 40. | Computer System For Generating An Integrated And Unified View Of Ip-Cores For Hierarchical Analysis Of A System On Chip (SOC) Design | United States | 13/961,758 | 7-Aug-2013 | 8788993 | 22-Jul-2014 |

| | Patent Title | Jurisdiction | Application (Provisional) Number | Application (Provisional) Date | Patent Number | Patent Date |
|---|---|---|---|---|---|---|
| 41. | A System and Methods for Reasonable Functional Verification of an Integrated Circuit Design | United States | 13/851,763 (61/786,668) | 27-Mar-2013 (15-Mar-2013) | 8806401 | 12-Aug-2014 |
| 42. | A System and Method for Inferring Higher Level Descriptions from RTL Topology based on Naming Similarities and Dependency | United States | 14/056,094 | 17-Oct-2013 | 8813003 | 19-Aug-2014 |
| 43. | Method Of Global Design Closure At Top Level And Driving Of Downstream Implementation Flow | United States | 14/055,653 (61/806,906) | 16-Oct-2013 (31-Mar-2013) | 8839171 | 16-Sep-2014 |
| 44. | System And Method For Metastability Verification Of Circuits Of An Integrated Circuit | United States | 13/887,596 | 6-May-2013 | 8856706 | 7-Oct-2014 |
| 45. | Characterization based Buffering and Sizing for System performance Optimization | United States | 13/625,377 | 24-Sep-2012 | 8863058 | 14-Oct-2014 |
| 46. | Method for measuring assertion density in a system of verifying integrated circuit design | United States | 13/783,635 | 4-Mar-2013 | 8881075 | 4-Nov-2014 |
| 47. | System And Method For Altering Circuit Design Hierarchy To Optimize Routing And Power Distribution Using Initial RTL-Level Circuit Description Netlist | United States | 13/829211 | 14-Mar-2013 | 8930863 | 6-Jan-2015 |
| 48. | System and Method for a Hybrid Clock Domain Crossing Verification | United States | 13/864,082 (61/786,661) | 16-Apr-2013 (15-Mar-2013) | 8984457 | 17-Mar-2015 |
| 49. | System and Method for Strengthening of a Circuit Element to Reduce an Integrated Circuit's Power Consumption | United States | 14/106,374 | 13-Dec-2013 | 8984469 | 17-Mar-2015 |

| | Patent Title | Jurisdiction | Application (Provisional) Number | Application (Provisional) Date | Patent Number | Patent Date |
|---|---|---|---|---|---|---|
| 50. | Quasi-static identification - An approach to identify potentially static signals in a design such as configuration and status registers. | United States | 13/872,303 (61/786,671) | 29-Apr-2013 (15-Mar-2013) | | |
| 51. | An Apparatus And Method Thereof For Hybrid Timing Exception Verification Of An Integrated Circuit Design | United States | 14/047,396 | 7-Oct-2013 | | |
| 52. | System and Methods for Reducing Power of a Circuit Using Critical Signal Analysis | United States | 14/600,234 (62/009,275) | 20-Jan-2015 (8-Jun-2014) | | |
| 53. | Method and System for selecting simulation signals for Power estimation | United States | 14/603,188 | 22-Jan-2015 | | |
| 54. | System and Method for Abstraction of a Circuit portion of An Integrated Circuit | United States | 14/181,476 | 14-Feb-2014 | | |
| 55. | Sequential Clock Gating Using Net Activity And Xor Technique On Semiconductor Designs Including Already Gated Pipeline Design | United States | 14/196,089 | 4-Mar-2014 | | |
| 56. | Method and Apparatus Using Formal Methods for Checking Generated-Clock Timing Definitions | United States | 14/184,021 | 19-Feb-2014 | | |
| 57. | A System And Method For Grading And Selecting Simulation Tests Using Property Coverage | United States | 14/745,700 (62/019,333) | 22-Jun-2015 (30-Jun-2014) | | |
| 58. | A System And Method Using Pass/Fail Test Results To Prioritize Electronic Design Verification Review Issues | United States | 14/812,109 (62/041,661) | 29-Jul-2015 (26-Aug-2014) | | |
| 59. | A System And Method For Viewing And Modifying Configurable RTL Modules | United States | 14/745,675 (62/019,360) | 22-Jun-2015 (30-Jun-2014) | | |

| | Patent Title | Jurisdiction | Application (Provisional) Number | Application (Provisional) Date | Patent Number | Patent Date |
|---|---|---|---|---|---|---|
| 60. | A System And Method For Generating Properties To Assist Emulation Debug (MARS Flow - Enhance And Enable Emulation Debug) | United States | (62/072,986) | (30-Oct-2014) | | |
| 61. | A System And Method For Netlist Clock Domain Crossing Verification | United States | 14/790,318<br><br>(62,129,645) | 2-Jul-2015<br><br>(6-Mar-2015) | | |
| 62. | A System And Method For Power Verification Using Efficient Merging Of Power State Tables | United States | 14/815,202<br><br>(62/140,386) | 31-Jul-2015<br><br>(30-Mar-2015) | | |
| 63. | A System And Method For Reactive Initialization Based Verification | United States | 14/794,549<br><br>(62/146,927) | 8-Jul-2015<br><br>(13-Apr-2015) | | |
| 64. | Systems, Methods, and Media for Assertion-Based Verification of Devices | United States | 13/672,477 | 8-Nov-2012 | | |
| 65. | Systems and Methods for Generating Predicates and Assertions | United States | 13/672,537 | 8-Nov-2012 | | |
| 66. | Method and System for Checking and Correcting Shoot-Through in RTL Simulation | United States | 14/716,422 | 19-May-2015 | | |
| 67. | A System And Method For Multi-Mode Clock Domain Crossing Verification | United States | (62,169,555) | (2-Jun-2015) | | |
| 68. | A System and Method for Transient Pulse Power Estimation | United States | (62,182,019) | (19-Jun-2015) | | |
| 69. | System and Method for Hierarchical Power Verification | United States | 14,815,302<br><br>(62,189,453) | 31-Jul-2015<br><br>(7-Jul-2015) | | |
| 70. | A System and Method for Managing and Composing Verification Engines | United States | 14,807,676 | 23-Jul-2015 | | |

## SCHEDULE B

## Trademarks and Trademark Applications

| | Trademark | Application Number | Application Date | Registration Number | Registration Date |
|---|---|---|---|---|---|
| 1. | **SPYGLASS** | 76/128979 | 15-Sep-2000 | 2,603,761 | 6-Aug-2002 |
| 2. | **ATRENTA** | 76/299344 | 13-Aug-2001 | 2,762,455 | 9-Sep-2003 |
| 3. | **SPYGLASS PREDICTIVE ANALYZER** | 78/137403 | 20-Jun-2002 | 2,778,737 | 28-Oct-2003 |
| 4. | **1TEAM** | 78/572506 | 22-Feb-2005 | 3,230,954 | 17-Apr-2007 |
| 5. | **1TEAM:EMBEDDED** | 78/572582 | 22-Feb-2005 | 3,256,970 | 26-Jun-2007 |
| 6. | **EARLY DESIGN CLOSURE** | 78/909287 | 15-Jun-2006 | 3,304,662 | 2-Oct-2007 |
| 7. | **GENSYS** | 77/842929 | 6-Oct-2009 | 4,105,992 | 28-Feb-2012 |
| 8. | **BUGSCOPE** | 86/245,590 | 8-Apr-2014 | 4,636,973 | 11-Nov-2014 |
| 9. | **MARS** | 86/261,440 | 24-Apr-2014 | 4,682,935 | 3-Feb-2015 |
| 10. | **1TEAM: SPYGLASS** | 78726061 | 04-Oct-2005 | | |
| 11. | **1TEAM: ANALYZE SPYGLASS** | 78726104 | 04-Oct-2005 | | |
| 12. | **FUTURE PERFECT** | 78579382 | 03-Mar-2005 | | |
| 13. | **ATRENTA** | 78575618 | 25-Feb-2005 | 3230964 | 17-Apr-2007 |
| 14. | **1TEAM: ANALYZE** | 78572528 | 22-Feb-2005 | | |
| 15. | **1TEAM: VERIFY** | 78572545 | 22-Feb-2005 | | |
| 16. | **1TEAM: IMPLEMENT** | 78572568 | 22-Feb-2005 | 3160627 | 17-Oct-2006 |
| 17. | **PERISCOPE** | 78416834 | 11-May-2004 | 3046985 | 17-Jan-2006 |
| 18. | **BLUEPRINT** | 78394711 | 01-Apr-2004 | | |
| 19. | **ACTIVESPEC** | 78168426 | 26-Sep-2002 | | |
| 20. | **ATRENTA THE PREDICTIVE ANALYSIS COMPANY** | 78137397 | 20-Jun-2002 | 2799296 | 23-Dec-2003 |

| | Trademark | Application Number | Application Date | Registration Number | Registration Date |
|---|---|---|---|---|---|
| 21. | **SURVEYOR** | 75552929 | 14-Sep-1998 | 2451460 | 15-May-2001 |