

TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

ETAS ID: TM379671

SUBMISSION TYPE:	NEW ASSIGNMENT		
NATURE OF CONVEYANCE:	Security Agreement		
CONVEYING PARTY DATA			
Name	Formerly	Execution Date	Entity Type
MAGNUM SEMICONDUCTOR, INC.		04/05/2016	Corporation: DELAWARE
RECEIVING PARTY DATA			
Name:	Silicon Valley Bank		
Street Address:	2400 Hanover Street		
City:	Palo Alto		
State/Country:	CALIFORNIA		
Postal Code:	95134		
Entity Type:	Corporation: CALIFORNIA		
PROPERTY NUMBERS Total: 2			
Property Type	Number	Word Mark	
Registration Number:	3808970	MAGNUM SEMICONDUCTOR	
Registration Number:	3805344	MAGNUM SEMICONDUCTOR	
CORRESPONDENCE DATA			
Fax Number:	8004947512		
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>			
Phone:	202-370-4750		
Email:	ipteam@nationalcorp.com		
Correspondent Name:	Darlena Bari Stark		
Address Line 1:	1025 Vermont Ave NW, Suite 1130		
Address Line 2:	National Corporate Research, Ltd.		
Address Line 4:	Washington, D.C. 20005		
ATTORNEY DOCKET NUMBER:	F162326		
NAME OF SUBMITTER:	James Won		
SIGNATURE:	/James Won/		
DATE SIGNED:	04/06/2016		
Total Attachments: 11			
source=1. Closing Copy - Intellectual Property Security Agreement - Magnum Semiconductor, Inc. (Borrower) (4-5-16)#page1.tif			

OP \$65.00 3808970

source=1. Closing Copy - Intellectual Property Security Agreement - Magnum Semiconductor, Inc. (Borrower) (4-5-16)#page2.tif
source=1. Closing Copy - Intellectual Property Security Agreement - Magnum Semiconductor, Inc. (Borrower) (4-5-16)#page3.tif
source=1. Closing Copy - Intellectual Property Security Agreement - Magnum Semiconductor, Inc. (Borrower) (4-5-16)#page4.tif
source=1. Closing Copy - Intellectual Property Security Agreement - Magnum Semiconductor, Inc. (Borrower) (4-5-16)#page5.tif
source=1. Closing Copy - Intellectual Property Security Agreement - Magnum Semiconductor, Inc. (Borrower) (4-5-16)#page6.tif
source=1. Closing Copy - Intellectual Property Security Agreement - Magnum Semiconductor, Inc. (Borrower) (4-5-16)#page7.tif
source=1. Closing Copy - Intellectual Property Security Agreement - Magnum Semiconductor, Inc. (Borrower) (4-5-16)#page8.tif
source=1. Closing Copy - Intellectual Property Security Agreement - Magnum Semiconductor, Inc. (Borrower) (4-5-16)#page9.tif
source=1. Closing Copy - Intellectual Property Security Agreement - Magnum Semiconductor, Inc. (Borrower) (4-5-16)#page10.tif
source=1. Closing Copy - Intellectual Property Security Agreement - Magnum Semiconductor, Inc. (Borrower) (4-5-16)#page11.tif

INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement (this "Agreement") is entered into as of April 5, 2016 by and between **SILICON VALLEY BANK**, a California corporation, with a loan production office located at 2400 Hanover Street, Palo Alto, California 95134 ("Bank") and **MAGNUM SEMICONDUCTOR, INC.**, a Delaware corporation, with its principal place of business located at 591 Yosemite Drive, Milpitas, California 95035 ("Grantor").

RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodations to Grantor, **GIGOPTIX, INC.**, a Delaware corporation, **CHIPX, INCORPORATED**, a Delaware corporation, and **ENDWAVE CORPORATION.**, a Delaware corporation (jointly and severally, individually and collectively "Borrower") (the "Loans") in the amounts and manner set forth in that certain Third Amended and Restated Loan and Security Agreement by and between Bank and Grantor dated as of the date hereof (as the same may be amended, modified or supplemented from time to time, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Borrower, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in its Copyrights, Trademarks, Patents, and Mask Works (as each term is described below) to secure the obligations of Borrower to Bank.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of Borrower's obligations to Bank, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

1. Grant of Security Interest. To secure Borrower's obligations to Bank, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its intellectual property (all of which shall collectively be called the "Intellectual Property Collateral"), including, without limitation, the following:

(a) Any and all copyright rights, copyright applications, copyright registrations and like protections in each work of authorship and derivative work thereof, whether published or unpublished and whether or not the same also constitutes a trade secret, now or hereafter existing, created, acquired or held, including without limitation those set forth on Exhibit A attached hereto (collectively, the "Copyrights");

(b) Any and all trade secrets, and any and all intellectual property rights in computer software and computer software products now or hereafter existing, created, acquired or held;

(c) Any and all design rights that may be available to Grantor now or hereafter existing, created, acquired or held;

(d) All patents, patent applications and like protections including, without limitation, improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the same, including without limitation the patents and patent applications set forth on Exhibit B attached hereto (collectively, the "Patents");

(e) Any trademark and servicemark rights, whether registered or not, applications to register and registrations of the same and like protections, and the entire goodwill of the business of Grantor connected with and symbolized by such trademarks, including without limitation those set forth on Exhibit C attached hereto (collectively, the "Trademarks");

(f) All mask works or similar rights available for the protection of semiconductor chips, now owned or hereafter acquired, including, without limitation those set forth on Exhibit D attached hereto (collectively, the "Mask Works");

(g) Any and all claims for damages by way of past, present and future infringements of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above;

(h) All licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works and all license fees and royalties arising from such use to the extent permitted by such license or rights;

(i) All amendments, extensions, renewals and extensions of any of the Copyrights, Trademarks, Patents, or Mask Works; and

(j) All proceeds and products of the foregoing, including without limitation all payments under insurance or any indemnity or warranty payable in respect of any of the foregoing.

2. Recordation. Grantor authorizes the Commissioner for Patents, the Commissioner for Trademarks and the Register of Copyrights and any other government officials to record and register this Agreement upon request by Bank.

3. Loan Documents. This Agreement has been entered into pursuant to and in conjunction with the Loan Agreement, which is hereby incorporated by reference. The provisions of the Loan Agreement shall supersede and control over any conflicting or inconsistent provision herein. The rights and remedies of Bank with respect to the Intellectual Property Collateral are as provided by the Loan Agreement and related documents, and nothing in this Agreement shall be deemed to limit such rights and remedies.

4. Execution in Counterparts. This Agreement may be executed in counterparts (and by different parties hereto in different counterparts), each of which shall constitute an original, but all of which when taken together shall constitute a single contract. Delivery of an executed counterpart of a signature page to this Agreement by facsimile or in electronic (i.e., "pdf" or "tif" format) shall be effective as delivery of a manually executed counterpart of this Agreement.

5. Successors and Assigns. This Agreement will be binding on and shall inure to the benefit of the parties hereto and their respective successors and assigns.

6. Governing Law. This Agreement and any claim, controversy, dispute or cause of action (whether in contract or tort or otherwise) based upon, arising out of or relating to this Agreement and the transactions contemplated hereby and thereby shall be governed by, and construed in accordance with, the

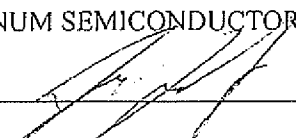
laws of the United States and the State of California, without giving effect to any choice or conflict of law provision or rule (whether of the State of California or any other jurisdiction).

[Signature page follows.]

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

MAGNUM SEMICONDUCTOR, INC.

By:  _____

Title: President

BANK:

SILICON VALLEY BANK

By: _____

Title: _____

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

MAGNUM SEMICONDUCTOR, INC.

By: _____

Title: _____

BANK:

SILICON VALLEY BANK

By:  _____

Title: Vice president _____

SCHEDULE A

Magnum Semiconductor, Inc. - Copyrights

None.

SCHEDULE B

Magnum Semiconductor, Inc. - U.S. Patents

PATENT NO.	ISSUE DATE	TITLE
7,134,039	2006-11-07	Recovery of real-time video data after power loss
7,974,523	2011-07-05	Optimal buffering and scheduling strategy for smooth reverse in a DVD player or the like
7,391,468	2008-06-24	Telecine conversion detection for progressive scan playback
7,469,067	2008-12-23	Sequential decoding of progressive coded JPEGs
7,574,580	2009-08-11	Intelligent caching scheme for streaming file systems
7,813,621	2010-10-12	Synchronized streaming layer with presentation layer
7,864,858	2011-01-04	Techniques for minimizing memory bandwidth used for motion compensation
7,613,615	2009-11-03	Circuits, systems, and methods for real-time de-shuffling of shuffled audio data
7,587,131	2009-09-08	Audio clocking in video applications
7,538,824	2009-05-26	Systems and methods for reducing noise during video deinterlacing
7,414,671	2008-08-19	Systems and methods for display object edge detection and pixel data interpolation in video processing systems
6,950,605	2005-09-27	Method and apparatus for recording real-time audio/video information onto recordable compact disc drives
7,246,220	2007-07-17	Architecture for hardware-assisted context switching between register groups dedicated to time-critical or non-time critical tasks without saving state
7,646,968	2010-01-12	End-user configurable digital versatile disk menus and methods for generating the same
7,894,681	2011-02-22	Sequential decoding of progressive coded JPEGs
9,118,425	2015-08-25	Transport stream multiplexers and methods for providing packets on a transport stream
9,154,782	2015-10-06	Apparatuses and methods for adjusting coefficients using dead zones
7,450,184	2008-11-11	Circuits and methods for detecting 2:2 encoded video and systems utilizing the same
7,522,214	2009-04-21	Circuits and methods for deinterlacing video display data and systems using the same
7,420,626	2008-09-02	Systems and methods for detecting a change in a sequence of interlaced data fields generated from a progressive scan source
6,011,870	2000-01-04	Multiple stage and low-complexity motion estimation for interframe video coding
6,108,047	2000-08-22	Variable-size spatial and temporal video scaler
6,192,075	2001-02-20	Single-pass variable bit-rate control for digital video coding
6,320,905	2001-11-20	Postprocessing system for removing blocking artifacts in block-based codecs
6,584,156	2003-06-24	LSI Architecture and implementation of MPEG video codec
6,754,618	2004-06-22	Fast implementation of MPEG audio coding
6,400,852	2002-06-04	Arbitrary zoom "on -the -fly"
8,487,797	2013-07-16	Audio clocking in video applications
8,378,867	2013-02-19	Audio clocking in video applications
9,258,517	2016-02-09	Methods and apparatuses for adaptively filtering video signals
9,277,254	2016-03-01	Transport stream multiplexers and methods for providing packets on a transport stream

Magnum Semiconductor, Inc. - U.S. Patent Applications

APPLICATION NO.	FILING DATE	TITLE
13/743,091	2013-01-16	Methods and apparatuses for providing an adaptive reduced resolution update mode
13/434,736	2012-03-29	Apparatuses and methods for providing quantized coefficients for video encoding
13/454,669	2012-04-24	Apparatuses and methods for bitstream bitstuffing
13/467,624	2012-05-09	Apparatuses and methods for estimating bitstream bit counts
13/660,803	2012-10-25	Rate-distortion optimizers and optimization techniques including joint optimization of multiple color components
13/627,776	2012-09-26 https://patents.google.com/?before=20120926	Apparatuses and methods for optimizing rate-distortion of syntax elements
13/800,980	2013-03-13	Video synchronization techniques using projection
13/760,871	2013-02-06	Apparatuses and methods for performing joint rate-distortion optimization of prediction mode
13/800,804	2013-03-13	Method and apparatus for perceptual macroblock quantization parameter decision to improve subjective visual quality of a video signal
13/836,746	2013-03-15	Apparatuses and methods for providing quantized coefficients for video encoding
14/011,503	2013-08-27	Apparatuses and methods for cabac initialization
13/889,778	2013-05-08	Systems, apparatuses, and methods for transcoding a bitstream
13/851,737	2013-03-27	Apparatuses and methods for staggered-field intra-refresh
13/856,995	2013-04-04	Apparatuses and methods for pooling multiple channels into a multi-program transport stream
13/886,047	2013-05-02	Methods and apparatuses including a statistical multiplexer with global rate control
14/071,341	2013-11-04	Methods and apparatuses for multi-pass adaptive quantization
14/011,535	2013-08-27	Methods and apparatuses for adjusting macroblock quantization parameters to improve visual quality for lossy video encoding
14/161,930	2014-01-23	Methods and apparatuses for content-adaptive quantization parameter modulation to improve video quality in lossy video coding
13/889,028	2013-05-07	Methods and apparatuses including a statistical multiplexer with bitrate smoothing
14/037,148	2013-09-25	Apparatuses and methods for reducing rate and distortion costs during encoding by modulating a lagrangian parameter
14/109,539	2013-12-17	Apparatuses and methods for providing optimized quantization weight matrices
14/326,211	2014-07-08	Methods and apparatuses for stripe-based temporal and spatial video processing
14/721,967	2015-05-26	
13/937,733	2013-07-09	Apparatuses and methods for adjusting a quantization parameter to improve subjective quality
14/025,522	2013-09-12	Methods and apparatuses including an encoding system with temporally adaptive quantization
14/854,359	2015-09-15	Apparatuses and methods for adjusting coefficients using dead zones
14/201,492	2014-03-07	Apparatuses and methods for performing video quantization rate distortion

		calculations
14/133,261	2013-12-18	Apparatuses and methods for optimizing rate-distortion costs in video encoding
14/309,034	2014-06-19	Apparatuses and methods for parameter selection during rate-distortion optimization
14/592,539	2015-01-08	
14/263,535	2014-04-28	Methods and apparatuses including a statistical multiplexer with multiple channel rate control
14/705,658	2015-05-06	
14/495,583	2014-09-24	Apparatuses and Methods for Filtering Noise from a Video Signal
14/316,329	2014-06-26	Methods and apparatuses for edge preserving and/or edge enhancing spatial filter
14/746,146	2015-06-22	
14/747,879	2015-06-23	
14/717,931	2015-05-20	

SCHEDULE C

Magnum Semiconductor, Inc. – U.S. Trademarks

REGISTRATION NO.	DATE	TRADEMARK
3808970	2010-06-29	MAGNUM SEMICONDUCTOR
3805344	2010-06-22	MAGNUM SEMICONDUCTOR & DESIGN

EXHIBIT D

Mask Works

Description

Registration/
Application
Number

Registration/
Application
Date

1959608.1