TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

ETAS ID: TM422460

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
Silicon Valley Bank		04/04/2017	Corporation: CALIFORNIA

RECEIVING PARTY DATA

Name:	ChipX, Incorporated
Street Address:	130 Baytech Drive
City:	San Jose
State/Country:	CALIFORNIA
Postal Code:	95134
Entity Type:	Corporation: DELAWARE

PROPERTY NUMBERS Total: 1

Property Type	Number	Word Mark
Registration Number:	3261924	CHIP·X

CORRESPONDENCE DATA

Fax Number: 80091442

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 614-280-3568
Email: John.Salvage@wolterskluwer.com
Correspondent Name: CT Corporation System
Address Line 1: 4400 Easton Commons Way
Address Line 2: Suite 125
Address Line 4: Columbus, OHIO 43219

OP $40.00 3261924

NAME OF SUBMITTER:	Elaine Carrera
SIGNATURE:	/Elaine Carrera/
DATE SIGNED:	04/04/2017

Total Attachments: 5
source=TM2#page1.tif
source=TM2#page2.tif
source=TM2#page3.tif
source=TM2#page4.tif
source=TM2#page5.tif

Form **PTO-1594** (Rev. 6-12)
OMB Collection 0651-0027 (exp. 04/30/2018)

U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

RECORDATION FORM COVER SHEET
TRADEMARKS ONLY

To the Director of the U. S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies):

Silicon Valley Bank

☐ Individual(s) ☐ Association
☐ Partnership ☐ Limited Partnership
☒ Corporation- State: CA
☐ Other

Citizenship (see guidelines) USA

Additional names of conveying parties attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies)

Additional names, addresses, or citizenship attached? ☐ Yes ☒ No

Name: ChipX, Incorporated

Street Address: 130 Baytech Drive

City: San Jose

State: CA

Country: USA Zip: 95134

☐ Individual(s) Citizenship
☐ Association Citizenship
☐ Partnership Citizenship
☐ Limited Partnership Citizenship
☒ Corporation Citizenship USA-DE
☐ Other Citizenship

If assignee is not domiciled in the United States, a domestic representative designation is attached: ☐ Yes ☐ No
(Designations must be a separate document from assignment)

3. Nature of conveyance/Execution Date(s) :

Execution Date(s) April 4, 2017

☐ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☒ Other Release of Security Interes

4. Application number(s) or registration number(s) and identification or description of the Trademark.

A. Trademark Application No.(s) Text

B. Trademark Registration No.(s)
3261924

Additional sheet(s) attached? ☐ Yes ☒ No

C. Identification or Description of Trademark(s) (and Filing Date if Application or Registration Number is unknown):

5. Name & address of party to whom correspondence concerning document should be mailed:

Name: Elaine Carrera, Legal Assistant

Internal Address:

Street Address: c/o Cahill Gordon & Reindel LLP
80 Pine Street

City: New York

State: NY Zip: 10005

Phone Number: (212) 701-3365

Docket Number:

Email Address: ecarrera@cahill.com

6. Total number of applications and registrations involved: 1

7. Total fee (37 CFR 2.6(b)(6) & 3.41) $

☐ Authorized to be charged to deposit account
☐ Enclosed

8. Payment Information:

Deposit Account Number

Authorized User Name

9. Signature: Elaine Carrera
Signature

April 4, 2017
Date

Elaine Carrera
Name of Person Signing

Total number of pages including cover sheet, attachments, and document: 5

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Branch, Director of the USPTO, P.O. Box 1450, Alexandria, VA 22313-1450

RELEASE OF SECURITY INTEREST IN INTELLECTUAL PROPERTY

This RELEASE, dated as of April 4, 2017, is made by Silicon Valley Bank (the "Secured Party"), pursuant to that certain Amended and Restated Security Agreement dated as of April 5, 2016 (the "Security Agreement") and that certain Third Amended and Restated Loan and Security Agreement dated as of April 5, 2016 (the "Amended Security Agreement").

W I T N E S S E T H

WHEREAS, ChipX Incorporated, a Delaware corporation, (the "Grantor") is party to the Security Agreement;

WHEREAS, pursuant to the Security Agreement, the Grantor executed that certain Intellectual Property Security Agreement dated as of April 23, 2010 and recorded with the U.S. Patent and Trademark Office on April 15, 2011 at Reel/Frame No. 026179/0023, and that certain Amended and Restated Intellectual Property Security Agreement dated as of April 5, 2016 and recorded with the U.S. Patent and Trademark Office on April 6, 2016 at Reel/Frame No. 038369/0452 with respect to the patents and patent applications assigned, and at Reel/Frame No. 5766/0666 with respect to the trademarks and trademark applications assigned (collectively, the "Intellectual Property Security Agreements"), pursuant to which the Grantor granted to the Secured Party a security interest in all of its right, title and interest in and to, among other intellectual property, the intellectual property set forth in Schedule I attached hereto (the "Patent and Trademark Collateral");

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the Secured Party agrees as follows:

The Secured Party hereby TERMINATES, without recourse, representation or warranty the Intellectual Property Security Agreement and the Amended and Restated Intellectual Property Security Agreement, and RELEASES, without recourse, representation or warranty its security interest in the Patent and Trademark Collateral, including the patents, trademark and patent applications set forth in Schedule I.

[SIGNATURE PAGE FOLLOWS]

IN WITNESS WHEREOF, the Secured Party has caused this Release to be duly executed and delivered as of the date first written above.

Silicon Valley Bank, as Secured Party

By: _____

Name: Janice Ahn

Title: Vice President

SCHEDULE I
to
RELEASE OF SECURITY INTEREST IN PATENT AND TRADEMARK COLLATERAL

Reel/Frame No. 026179/0023

Title	Patent No.	Issue Date
Methods and computer readable media implementing a modified routing grid to increase routing densities of customizable logic array devices	7735041	06/08/10
Method and apparatus for dqs postamble detection and drift compensation in a double data rate (ddr) physical interface	7675811	03/09/10
Cells of a customizable logic array device having independently accessible circuit elements	7511536	03/31/09
Method of developing application-specific integrated circuit devices	7500215	03/03/09
In-circuit device, system and method to parallelize design and verification of application-specific integrated circuits ("asics") having embedded specialized function circuits	7340705	03/04/08
Configurable cell for customizable logic array device	6924662	08/02/05
Single metal programmability in a customizable integrated circuit device	6903390	06/07/05
Configurable cell for customizable logic array device	6294927	09/25/01
Low voltage device operable with a high voltage supply	6150878	11/21/00
Customizable integrated circuit device	5903490	05/11/99
Cell forming part of a customizable logic array	5684412	11/04/97
Personalizable gate array devices	5619062	04/08/97
Mapping of gate arrays	5565758	10/15/96
Personalizable gate array devices	5545904	08/13/96
Personalizable multi-chip carrier including removable fuses	5541814	07/30/96
Routing structures for a customizable integrated circuit	5260597	11/09/93

Reel/Frame No. 038369/0452

ChipX, Incorporated - U.S. Patents

PATENT NO.	ISSUE DATE	TITLE
7,340,705	2008-03-04	In-circuit device, system and method to parallelize design and verification of application-specific integrated circuits ("ASICs") having embedded specialized function circuits
7,500,215	2009-03-03	Method of developing application-specific integrated circuit devices
7,511,536	2009-03-31	Cells of a customizable logic array device having independently accessible circuit elements
7,675,811	2010-03-09	Method and apparatus for DQS postamble detection and drift compensation in a double data rate (DDR) physical interface
7,735,041	2010-06-08	Methods and computer readable media implementing a modified routing grid to increase routing densities of customizable logic array devices

ChipX, Incorporated - U.S. Patent Applications

APPLICATION NO.	FILING DATE	TITLE
12/082,100	2008-04-07	Method and apparatus for DQS postamble detection and drift compensation in a double data rate (DDR) physical interface

Reel/Frame No. 5766/0666

ChipX, Incorporated - U.S. Trademarks

REGISTRATION NO.	REGISTRATION DATE	TRADEMARK
3261924	2007-07-10	CHIP·X