

TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

ETAS ID: TM424039

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| SUBMISSION TYPE: | NEW ASSIGNMENT | | |
| NATURE OF CONVEYANCE: | SECURITY INTEREST | | |
| CONVEYING PARTY DATA | | | |
| Name | Formerly | Execution Date | Entity Type |
| Avalanche Technology, Inc. | | 04/13/2017 | Corporation: DELAWARE |
| RECEIVING PARTY DATA | | | |
| Name: | Structured Alpha LP | | |
| Street Address: | 65 Queen Street West | | |
| Internal Address: | Suite 2400 | | |
| City: | Toronto, Ontario | | |
| State/Country: | CANADA | | |
| Postal Code: | M5H 2M8 | | |
| Entity Type: | Corporation: CAYMAN ISLANDS | | |
| PROPERTY NUMBERS Total: 3 | | | |
| Property Type | Number | Word Mark | |
| Registration Number: | 4198751 | AVALANCHE TECHNOLOGY | |
| Registration Number: | 4237990 | AVALANCHE | |
| Registration Number: | 4946647 | AVA | |
| CORRESPONDENCE DATA | | | |
| Fax Number: | 6175231231 | | |
| <i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i> | | | |
| Phone: | (617) 570-1000 | | |
| Email: | AFeeney@Goodwinlaw.com | | |
| Correspondent Name: | Goodwin Procter LLP c/o Alan F. Feeney | | |
| Address Line 1: | 100 Northern Avenue | | |
| Address Line 4: | Boston, MASSACHUSETTS 02210 | | |
| NAME OF SUBMITTER: | ALAN F FEENEY, ESQ | | |
| SIGNATURE: | /alan f feeney/ | | |
| DATE SIGNED: | 04/18/2017 | | |
| Total Attachments: 24 | | | |
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INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement ("Agreement") is entered into as of the April 13, 2017 by and between STRUCTURED ALPHA LP ("Secured Party") and AVALANCHE TECHNOLOGY, INC. ("Grantor").

RECITALS

A. Secured Party has agreed to purchase a certain promissory note (the "Note") from and to extend certain financial accommodation to Grantor in the amounts and manner set forth in that certain Note and Warrant Purchase Agreement by and between Secured Party and Grantor dated as of the date hereof (as the same may be amended, modified or supplemented from time to time, the "Purchase Agreement"; capitalized terms used herein are used as defined in the Purchase Agreement or the Security Agreement (as defined in the Purchase Agreement), as applicable). Secured Party is willing to purchase the Note from Grantor, but only upon the condition, among others, that Grantor shall grant to Secured Party a security interest in certain Copyrights, Trademarks, Patents, and Mask Works (as each term is described below) to secure the obligations of Grantor under the Purchase Agreement, Note and other Transaction Documents.

B. Pursuant to the terms of the Security Agreement, Grantor has granted to Secured Party a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Purchase Agreement, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

1. Grant of Security Interest. To secure its obligations under the Purchase Agreement, including, without limitation, the Obligations, Grantor grants and pledges to Secured Party a security interest in all of Grantor's right, title and interest in, to and under its intellectual property (all of which shall collectively be called the "Intellectual Property Collateral"), including, without limitation, the following:

(a) Any and all copyright rights, copyright applications, copyright registrations and like protections in each work or authorship and derivative work thereof, whether published or unpublished and whether or not the same also constitutes a trade secret, now or hereafter existing, created, acquired or held, including without limitation those set forth on Exhibit A attached hereto (collectively, the "Copyrights");

(b) Any and all trade secrets, and any and all intellectual property rights in computer software and computer software products now or hereafter existing, created, acquired or held;

(c) Any and all design rights that may be available to Grantor now or hereafter existing, created, acquired or held;

(d) All patents, patent applications and like protections including, without limitation, improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the same, including without limitation the patents and patent applications set forth on Exhibit B attached hereto (collectively, the "Patents");

(e) Any trademark and servicemark rights, whether registered or not, applications to register and registrations of the same and like protections, and the entire goodwill of the business of Grantor connected with and symbolized by such trademarks, including without limitation those set forth on Exhibit C attached hereto, but excluding any intent-to-use trademarks at all times prior to the first use thereof, whether by the actual use thereof in commerce, the recording of a statement of use with the United States Patent and Trademark Office or otherwise (collectively, the "Trademarks");

(f) All mask works or similar rights available for the protection of semiconductor chips, now owned or hereafter acquired, including, without limitation those set forth on Exhibit D attached hereto (collectively, the "Mask Works");

(g) Any and all claims for damages by way of past, present and future infringements of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above;

(h) All licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works (other than licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works granted in the ordinary course of Grantor's business);

(i) All license fees and royalties arising from the use of any of the Copyrights, Patents, Trademarks, or Mask Works to the extent permitted by such license or rights;

(j) All amendments, extensions, renewals and extensions of any of the Copyrights, Trademarks, Patents, or Mask Works; and

(k) All proceeds and products of the foregoing, including without limitation all payments under insurance or any indemnity or warranty payable in respect of any of the foregoing.

2. Recordation. Grantor authorizes the Commissioner for Patents, the Commissioner for Trademarks and the Register of Copyrights and any other government officials to record and register this Agreement with the United States Patent and Trademark Office, the United States Copyright Office or any other governmental agency or office providing for the registering or perfection of security interests in any Intellectual Property Collateral, as applicable, upon request by Secured Party.

3. Authorization. Grantor hereby authorizes Secured Party to (a) modify this Agreement unilaterally by amending the exhibits to this Agreement to include any Intellectual Property Collateral which Grantor obtains subsequent to the date of this Agreement, and (b) file a duplicate original of this Agreement containing amended exhibits reflecting such new Intellectual Property Collateral.

4. Transaction Documents. This Agreement has been entered into pursuant to and in conjunction with the Purchase Agreement and the Security Agreement, which are hereby incorporated by reference. The provisions of the Purchase Agreement and the Security Agreement shall supersede and control over any conflicting or inconsistent provision herein. The rights and remedies of Security Party with respect to the Intellectual Property Collateral are as provided by the Purchase Agreement, the Security Agreement and related documents, and nothing in this Agreement shall be deemed to limit such rights and remedies.

5. Execution in Counterparts. This Agreement may be executed in counterparts (and by different parties hereto in different counterparts), each of which shall constitute an original, but all of which when taken together shall constitute a single contract. Delivery of an executed counterpart of a

signature page to this Agreement by facsimile or in electronic (i.e., "pdf" or "tif" format) shall be effective as delivery of a manually executed counterpart of this Agreement. The words "execution," "signed," "signature" and words of like import herein shall be deemed to include electronic signatures or the keeping of records in electronic form, each of which shall be of the same legal effect, validity and enforceability as a manually executed signature or the use of a paper-based recordkeeping systems, as the case may be, to the extent and as provided for in any applicable law, including, without limitation, any state law based on the Uniform Electronic Transactions Act.


6. Successors and Assigns. This Agreement will be binding on and shall inure to the benefit of the parties hereto and their respective successors and assigns.

7. Governing Law. This Agreement and any claim, controversy, dispute or cause of action (whether in contract or tort or otherwise) based upon, arising out of or relating to this Agreement and the transactions contemplated hereby and thereby shall be governed by, and construed in accordance with, the laws of the United States and the State of California, without giving effect to any choice or conflict of law provision or rule (whether of the State of California or any other jurisdiction).

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

AVALANCHE TECHNOLOGY, INC.


By: ROBERT NETTER
Title: CFO

SECURED PARTY:

STRUCTURED ALPHA LP

By: Thomvest Asset Management Inc.,
its General Partner

By: Stefan V. Clulow
Title: Managing Director and Chief Investment
Officer

SIGNATURE PAGE TO
INTELLECTUAL PROPERTY SECURITY AGREEMENT

TRADEMARK
REEL: 006036 FRAME: 0025

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:


AVALANCHE TECHNOLOGY, INC.

By: _____
Title: _____

SECURED PARTY:

STRUCTURED ALPHA LP

By: Thomvest Asset Management Inc.,
its General Partner


By: Stefan V. Glulow
Title: Managing Director and Chief Investment
Officer

SIGNATURE PAGE TO
INTELLECTUAL PROPERTY SECURITY AGREEMENT

TRADEMARK
REEL: 006036 FRAME: 0026

EXHIBIT A

Copyrights

Description

Registration/
Application
Number

Registration/
Application
Date

None.

EXHIBIT B

Patents

Patent Applications

| | Title | Application # |
|----|--|---------------|
| 1 | Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) With Enhanced Write Current | 14524848 |
| 2 | PERPENDICULAR MAGNETIC TUNNEL JUNCTION (pMTJ) WITH IN-PLANE MAGNETO-STATIC SWITCHING-ENHANCING LAYER | 14930523 |
| 3 | MAGNETIC RANDOM ACCESS MEMORY WITH DYNAMIC RANDOM ACCESS MEMORY (DRAM)-LIKE INTERFACE | 15132278 |
| 4 | Fast Programming of Magnetic Random Access Memory (MRAM) | 15417135 |
| 5 | METHOD OF IMPLEMENTING MAGNETIC RANDOM ACCESS MEMORY (MRAM) FOR SYSTEM BOOT | 14091 318 |
| 6 | MANAGEMENT OF MEMORY ARRAY WITH MAGNETIC RANDOM ACCESS MEMORY (MRAM) | 15094 844 |
| 7 | MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER AND THIN REFERENCE LAYER | 15080 208 |
| 8 | MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR ENHANCEMENT LAYER | 14256192 |
| 9 | MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR ENHANCEMENT LAYER | 14797458 |
| 10 | SPIN-ORBITRONICS DEVICE AND APPLICATIONS THEREOF | 14831546 |
| 11 | Three Dimensional Memory Arrays and stitching there of | 15141726 |
| 12 | MEMORY SYSTEM HAVING THERMALLY STABLE PERPENDICULAR MAGNETO TUNNEL JUNCTION (MTJ) AND A METHOD OF MANUFACTURING SAME | 13737897 |
| 13 | MAGNETIC RANDOM ACCESS MEMORY WITH BURST ACCESS | 13235294 |
| 14 | STORAGE SYSTEM EMPLOYING MRAM AND ARRAY OF SOLID STATE DISKS WITH INTEGRATED SWITCH | 13831921 |
| 15 | STORAGE SYSTEM EMPLOYING MRAM AND ARRAY OF SOLID STATE DISKS WITH INTEGRATED SWITCH | 14688996 |

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| 16 | A SHARED PERIPHERAL COMPONENT INTERCONNECT EXPRESS (PCIe) END POINT SYSTEM WITH A PCIe SWITCH AND METHOD FOR INITIALIZING THE SAME | 14948187 |
| 17 | LANDING PAD IN PERIPHERAL CIRCUIT FOR MAGNETIC RANDOM ACCESS MEMORY (MRAM) | 15158 872 |
| 18 | STORAGE PROCESSOR MANAGING SOLID STATE DISK ARRAY | 14595 170 |
| 19 | STORAGE SYSTEM REDUNDANT ARRAY OF SOLID STATE DISK ARRAY | 14678 777 |
| 20 | A METHOD AND APPARATUS FOR DE-DUPLICATION FOR SOLID STATE DISKS (SSDs) | 14722038 |
| 21 | STORAGE PROCESSOR MANAGING NVME LOGICALLY ADDRESSED SOLID STATE DISK ARRAY | 14629404 |
| 22 | PERPENDICULAR STTMRAM DEVICE WITH BALANCED REFERENCE LAYER | 14661253 |
| 23 | MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR ENHANCEMENT LAYER | 15 440 948 |
| 24 | MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR ENHANCEMENT LAYER | 15 365 371 |
| 25 | A METHOD OF LUN MANAGEMENT IN A SOLID STATE DISK ARRAY | 14617868 |
| 26 | SOFTWARE-DEFINED SSD AND SYSTEM USING THE SAME | 14679 956 |
| 27 | A STORAGE SYSTEM CONTROLLING ADDRESSING OF SOLID STORAGE DISKS (SSD) | 14679823 |
| 28 | A METHOD AND APPARATUS TO REDUCE POWER CONSUMPTION OF MOBILE AND PORTABLE DEVICES WITH NON-VOLATILE MEMORIES | 14269049 |
| 29 | A multi-level scalable switch architecture for Storage Appliance | 14842804 |
| 30 | MAGNETIC RANDOM ACCESS MEMORY WITH ULTRATHIN REFERENCE LAYER | 14730073 |
| 31 | MAGNETIC RANDOM ACCESS MEMORY WITH ULTRATHIN REFERENCE LAYER | 14263046 |
| 32 | Reduction of Area and Power for sense amplifier in memory | 15276318 |
| 33 | MAGNETIC RANDOM ACCESS MEMORY WITH MULTILAYERED SEED STRUCTURE | 15295002 |
| 34 | Memory Device Incorporating selector element with multiple thresholds | 15221505 |
| 35 | Memory Device for Emulating Dynamic Random Access | 15011344 |

Memory (DRAM)

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| 36 | Serial Link Storage Interface (SLSI) Hybrid Block Storage | 62274626 |
| 37 | Serial Link Storage Interface (SLSI) Hybrid Block Storage | 15383899 |
| 38 | Management of Memory Array with Magnetic Random Access Memory (MRAM) | 15411913 |
| 39 | Selector device Incorporating Conductive Cluster for Memory Application | 15157607 |
| 40 | Method for Sensing Memory Element Coupled to Selector Device | 15264847 |
| 41 | Programming of Non-Volatile Memory Subjected to High Temperature Exposure | 15265774 |
| 42 | Selector device Incorporating Conductive Cluster for Memory Application | 15438637 |
| 43 | METHOD AND APPARATUS FOR ADJUSTMENT OF CURRENT THROUGH A MAGNETORESISTIVE TUNNEL JUNCTION (MTJ) BASED ON TEMPERATURE FLUCTUATIONS | 15434966 |

Registered Patents

| | Patent Title | Patent # |
|----|--|----------|
| 1 | Non-Uniform Switching Based Non-Volatile Magnetic Based Memory | 8477530 |
| 2 | Non-Uniform Switching Based Non-Volatile Magnetic Based Memory | 8389301 |
| 3 | Non-Uniform Switching Based Non-Volatile Magnetic Based Memory | 8084835 |
| 4 | A HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY | 8724413 |
| 5 | A HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY | 9047968 |
| 6 | A HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY | 8391054 |
| 7 | A HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY | 8058696 |
| 8 | NON-VOLATILE MAGNETIC MEMORY WITH LOW SWITCHING CURRENT AND HIGH THERMAL STABILITY | 8493777 |
| 9 | NON-VOLATILE MAGNETIC MEMORY WITH LOW SWITCHING CURRENT AND HIGH THERMAL STABILITY | 8405174 |
| 10 | NON-VOLATILE MAGNETIC MEMORY WITH LOW SWITCHING CURRENT AND HIGH THERMAL STABILITY | 8310020 |
| 11 | NON-VOLATILE MAGNETIC MEMORY WITH LOW SWITCHING CURRENT AND HIGH THERMAL STABILITY | 8183652 |
| 12 | Non-Volatile Magnetic Memory Element with Graded Layer | 8399942 |
| 13 | Non-Volatile Magnetic Memory Element with Graded Layer | 8399943 |
| 14 | Non-Volatile Magnetic Memory Element with Graded Layer | 8493778 |
| 15 | Non-Volatile Magnetic Memory Element with Graded Layer | 8493779 |
| 16 | Non-Volatile Magnetic Memory Element with Graded Layer | 8498148 |

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| 17 | Non-Volatile Magnetic Memory Element with Graded Layer | 8488376 |
| 18 | Non-Volatile Magnetic Memory Element with Graded Layer | 8493780 |
| 19 | Non-Volatile Magnetic Memory Element with Graded Layer | 8498149 |
| 20 | Non-Volatile Magnetic Memory Element with Graded Layer | 8498150 |
| 21 | Non-Volatile Magnetic Memory Element with Graded Layer | 8063459 |
| 22 | HIGH CAPACITY LOW COST MULTI-STACKED CROSS-LINE MAGNETIC MEMORY | 8947919 |
| 23 | CURRENT-CONFINED EFFECT OF MAGNETIC NANO-CURRENT-CHANNEL (NCC) FOR MAGNETIC RANDOM ACCESS MEMORY (MRAM) | 7981697 |
| 24 | CURRENT-CONFINED EFFECT OF MAGNETIC NANO-CURRENT-CHANNEL (NCC) FOR MAGNETIC RANDOM ACCESS MEMORY (MRAM) | 7732881 |
| 25 | High capacity low cost muliti state magnetic memory | 9218866 |
| 26 | SSTRAM element having multiple perpendicular MTJS Coupled in series | 9349941 |
| 27 | AN IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY | 9478279 |
| 28 | AN IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY | 9337413 |
| 29 | LOW COST MULTI-STATE MAGNETIC MEMORY | 8456897 |
| 30 | LOW COST MULTI-STATE MAGNETIC MEMORY | 8330240 |
| 31 | LOW COST MULTI-STATE MAGNETIC MEMORY | 8018011 |
| 32 | Low resistance high-TMR magnetic tunnel junction and process for fabrication thereof | 8508984 |
| 33 | METHOD FOR MANUFACTURING NON-VOLATILE MAGNETIC MEMORY | 8980649 |

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| 34 | METHOD FOR MANUFACTURING NON-VOLATILE MAGNETIC MEMORY | 8535952 |
| 35 | LOW CURRENT SWITCHING MAGNETIC TUNNEL JUNCTION DESIGN FOR MAGNETIC MEMORY USING DOMAIN WALL MOTION | 8427863 |
| 36 | A MAGNETIC MEMORY WITH A DOMAIN WALL | 8724379 |
| 37 | LOW CURRENT SWITCHING MAGNETIC TUNNEL JUNCTION DESIGN FOR MAGNETIC MEMORY USING DOMAIN WALL MOTION | 8164947 |
| 38 | LOW CURRENT SWITCHING MAGNETIC TUNNEL JUNCTION DESIGN FOR MAGNETIC MEMORY USING DOMAIN WALL MOTION | 7869266 |
| 39 | Magnetic memory write circuitry | 8760914 |
| 40 | Memory Sensing Circuit | 8363457 |
| 41 | A LOW-COST NON-VOLATILE FLASHRAM MEMORY | 8391058 |
| 42 | NON-VOLATILE FLASH-RAM MEMORY WITH MAGNETIC MEMORY | 8711613 |
| 43 | A HYBRID NON-VOLATILE MEMORY DEVICE | 9081669 |
| 44 | A LOW-COST NON-VOLATILE FLASHRAM MEMORY | 8440471 |
| 45 | A LOW-COST NON-VOLATILE FLASHRAM MEMORY | 8120949 |
| 46 | METHOD FOR MANUFACTURING HIGH DENSITY NON-VOLATILE MAGNETIC MEMORY | 8802451 |
| 47 | Magnetic Random Access Memory (MRAM) Manufacturing Process for a Small Magnetic Tunnel Junction (MTJ) Design with a Low Programming Current Requirement | 8542526 |
| 48 | Magnetic Random Access Memory (MRAM) Manufacturing Process for a Small Magnetic Tunnel Junction (MTJ) Design with a Low Programming Current Requirement | 8542524 |
| 49 | EMBEDDED MAGNETIC RANDOM ACCESS MEMORY (MRAM) | 8477529 |
| 50 | EMBEDDED MAGNETIC RANDOM ACCESS MEMORY (MRAM) | 8730716 |

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| 51 | EMBEDDED MAGNETIC RANDOM ACCESS MEMORY (MRAM) | 8634234 |
| 52 | EMBEDDED MAGNETIC RANDOM ACCESS MEMORY (MRAM) | 8289757 |
| 53 | Flash Memory With Nano-Pillar Charge Trap | 8687418 |
| 54 | A MULTI-STATE SPIN-TORQUE TRANSFER MAGNETIC RANDOM ACCESS MEMORY | 8917543 |
| 55 | SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY HAVING MAGNETIC TUNNEL JUNCTION WITH PERPENDICULAR MAGNETIC ANISOTROPY | 8593862 |
| 56 | Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) with Perpendicular Laminated Free layer | 8982616 |
| 57 | A Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) with Perpendicular Laminated Free layer | 9025371 |
| 58 | A Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) With Laminated Free Layer | 8374025 |
| 59 | MAGNETIC RANDOM ACCESS MEMORY WITH FIELD COMPENSATING LAYER AND MULTI-LEVEL CELL | 8565010 |
| 60 | MAGNETIC RANDOM ACCESS MEMORY WITH FIELD COMPENSATING LAYER AND MULTI-LEVEL CELL | 8598576 |
| 61 | Shared Transistor in a Spin-Torque Transfer Magnetic Random Access Memory (STTMRAM) Cell | 8724378 |
| 62 | Spin-Torque Transfer Magnetic Random Access Memory (STTMRAM) Device with Shared Transistor and Minimal Written Data Disturbance | 8611145 |
| 63 | Method and Apparatus for Programming a Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) Array | 8879309 |
| 64 | Shared Transistor in a Spin-Torque Transfer Magnetic Random Access Memory (STTMRAM) Cell | 8238145 |
| 65 | Low-crystallization temperature MTJ for Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) | 8422286 |
| 66 | A SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY (STTMRAM) USING A SYNTHETIC FREE LAYER | 8611147 |
| 67 | Low-crystallization temperature MTJ for Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) | 8169821 |

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| 68 | METHOD AND APPARATUS FOR PROGRAMMING A MAGNETIC TUNNEL JUNCTION (MTJ) | 9070458 |
| 69 | METHOD AND APPARATUS FOR PROGRAMMING A MAGNETIC TUNNEL JUNCTION (MTJ) | 9520174 |
| 70 | METHOD AND APPARATUS FOR PROGRAMMING A MAGNETIC TUNNEL JUNCTION (MTJ) | 8363460 |
| 71 | SPIN TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY (STTMRAM) HAVING GRADED SYNTHETIC FREE LAYER | 8772886 |
| 72 | SPIN TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY (STTMRAM) HAVING GRADED SYNTHETIC FREE LAYER | 8779537 |
| 73 | EMULATION OF STATIC RANDOM ACCESS MEMORY (SPAM) BY MAGNETIC RANDOM ACCESS MEMORY (MRAM) | 8971107 |
| 74 | EMULATION OF STATIC RANDOM ACCESS MEMORY (SPAM) BY MAGNETIC RANDOM ACCESS MEMORY (MRAM) | 8755221 |
| 75 | METHOD AND APPARATUS FOR INCREASING THE RELIABILITY OF AN ACCESS TRANSISTOR COUPLED TO A MAGNETIC TUNNEL JUNCTION (MTJ) | 8917546 |
| 76 | METHOD AND APPARATUS FOR INCREASING THE RELIABILITY OF AN ACCESS TRANSISTOR COUPLED TO A MAGNETIC TUNNEL JUNCTION (MTJ) | 9343134 |
| 77 | Method and Apparatus of increase the reliability of an Access Transistor Coupled to a Magnetic Tunnel Junction (MTJ) | 9530479 |
| 78 | METHOD AND APPARATUS FOR INCREASING THE RELIABILITY OF AN ACCESS TRANSISTOR COUPLED TO A MAGNETIC TUNNEL JUNCTION (MTJ) | 8295083 |
| 79 | SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR MAGNETIC ANISOTROPY MULTILAYERS | 9019758 |
| 80 | SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR MAGNETIC ANISOTROPY MULTILAYERS | 9444039 |
| 81 | SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR MAGNETIC ANISOTROPY MULTILAYERS | 9318179 |
| 82 | SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR MAGNETIC ANISOTROPY MULTILAYERS | 9.419.210 |
| 83 | Spin-transfer torque magnetic random access memory with multilayered storage layer | 8519496 |

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| 84 | MAGNETIC RANDOM ACCESS MEMORY (MRAM) WITH ENHANCED MAGNETIC STIFFNESS AND METHOD OF MAKING SAME | 8852676 |
| 85 | SST-MRAM MTJ manufacturing method with in-situ annealing | 8758850 |
| 86 | MAGNETIC RANDOM ACCESS MEMORY (MRAM) WITH ENHANCED MAGNETIC STIFFNESS AND METHOD OF MAKING SAME | 9070464 |
| 87 | MAGNETIC RANDOM ACCESS MEMORY (MRAM) WITH ENHANCED MAGNETIC STIFFNESS AND METHOD OF MAKING SAME | 9054298 |
| 88 | MTJ MANUFACTURING METHOD UTILIZING IN-SITU ANNEALING AND ETCH BACK | 9028910 |
| 89 | MAGNETIC RANDOM ACCESS MEMORY (MRAM) WITH ENHANCED MAGNETIC STIFFNESS AND METHOD OF MAKING SAME | 8623452 |
| 90 | ACCESS TRANSISTOR WITH A BURIED GATE | 8803200 |
| 91 | ACCESS TRANSISTOR WITH A BURIED GATE | 8723281 |
| 92 | VIALESS MEMORY STRUCTURE AND MEHTOD OF MANUFACTURING SAME | 9082695 |
| 93 | MAGNETIC TUNNEL JUNCTION (MTJ) FORMATION WITH TWO-STEP PROCESS | 8313960 |
| 94 | MAGNETIC TUNNEL JUNCTION (MTJ) FORMATION WITH TWO-STEP PROCESS | 8148174 |
| 95 | Method and apparatus fo rmeasuring magnetic parameters of magnetic thin film structures | 8633720 |
| 96 | MAPPING OF RANDOM DEFECTS IN A MEMORY DEVICE | 9224504 |
| 97 | MAPPING OF RANDOM DEFECTS IN A MEMORY DEVICE | 8887013 |
| 98 | ERPENDICULAR MAGNETIC TUNNEL JUNCTION (pMTJ) WITH IN-PLANE MAGNETO-STATIC SWITCHING-ENHANCING LAYER | 9196332 |
| 99 | RESISTIVE MEMORY DEVICE HAVING VERTICAL TRANSISTORS AND METHOD FOR MAKING THE SAME | 8575584 |
| 100 | MRAM with sidewall protection and method of fabrication | 8709956 |

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| 101 | MRAM with sidewall protection and method of fabrication | 9013045 |
| 102 | MRAM WITH SIDEWALL PROTECTION AND METHOD OF FABRICATION | 8796795 |
| 103 | High speed SST-MRAM with orthogonal pinned layer | 8860158 |
| 104 | MAGNETIC RANDOM ACCESS MEMORY WITH SWITCHABLE SWITCHING ASSIST LAYER | 8981506 |
| 105 | MAGNETIC LATCH MAGNETIC RANDOM ACCESS MEMORY (MRAM) | 8492860 |
| 106 | MRAM ETCHING PROCESSES | 8536063 |
| 107 | MRAM ETCHING PROCESSES | 8975088 |
| 108 | MEMORY WITH ON-CHIP ERROR CORRECTION | 9083382 |
| 109 | Memory with on-chip error correction | 8751905 |
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EXHIBIT C

Trademarks

| <u>Description</u> | <u>Registration/ Application Number</u> | <u>Registration/ Application Date</u> |
|----------------------|---|---|
| AVALANCHE TECHNOLOGY | 4,198,751 | 8/28/2012 |
| AVALANCHE | 4,237,990 | 11/6/2012 |
| AVA | 4,946,647 | 4/26/2016 |

EXHIBIT D

Mask Works

Description

Registration/
Application
Number

Registration/
Application
Date

None.