

TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

ETAS ID: TM439827

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|---|--------------------------------|-----------------------|-----------------------|
| SUBMISSION TYPE: | NEW ASSIGNMENT | | |
| NATURE OF CONVEYANCE: | SECURITY INTEREST | | |
| CONVEYING PARTY DATA | | | |
| Name | Formerly | Execution Date | Entity Type |
| ESILICON CORPORATION | | 07/31/2017 | Corporation: DELAWARE |
| RECEIVING PARTY DATA | | | |
| Name: | RUNWAY GROWTH CREDIT FUND INC. | | |
| Street Address: | 2925 WOODSIDE ROAD | | |
| City: | WOODSIDE | | |
| State/Country: | CALIFORNIA | | |
| Postal Code: | 94062 | | |
| Entity Type: | Corporation: MARYLAND | | |
| PROPERTY NUMBERS Total: 4 | | | |
| Property Type | Number | Word Mark | |
| Registration Number: | 2969847 | ESILICON | |
| Registration Number: | 3603342 | ESILICON ACCESS | |
| Registration Number: | 3412021 | ESILICON | |
| Registration Number: | 3591594 | ESILICON | |
| CORRESPONDENCE DATA | | | |
| Fax Number: | 8585506420 | | |
| <i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i> | | | |
| Phone: | 858-550-6433 | | |
| Email: | jmfitzpatrick@cooley.com | | |
| Correspondent Name: | JENNIFER FITZPATRICK | | |
| Address Line 1: | C/O COOLEY LLP | | |
| Address Line 2: | 4401 EASTGATE MALL | | |
| Address Line 4: | SAN DIEGO, CALIFORNIA 92121 | | |
| ATTORNEY DOCKET NUMBER: | 326420-105 | | |
| NAME OF SUBMITTER: | JENNIFER FITZPATRICK | | |
| SIGNATURE: | /JENNIFER FITZPATRICK/ | | |
| DATE SIGNED: | 08/18/2017 | | |
| Total Attachments: 7 | | | |

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INTELLECTUAL PROPERTY SECURITY AGREEMENT

This **INTELLECTUAL PROPERTY SECURITY AGREEMENT** (as amended, restated, supplemented or otherwise modified, this “**Agreement**”) is entered into as of July 31, 2017 by and between **RUNWAY GROWTH CREDIT FUND INC.**, a Maryland corporation (“**Lender**”) and **ESILICON CORPORATION**, a Delaware corporation (“**Grantor**”).

RECITALS

A. Lender and Grantor are entering into a Loan and Security Agreement as of the date hereof (as amended, restated, supplemented or otherwise modified from time to time, the “**Loan Agreement**”). Defined terms used herein without definition shall have the meanings set forth in the Loan Agreement.

B. The Obligations are secured by the Collateral, as defined in the Loan Agreement, including without limitation, all of Grantor’s Intellectual Property.

C. Grantor’s execution and delivery of this Agreement is a condition to the effectiveness of the Loan Agreement.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, Grantor and Lender hereby agree:

AGREEMENT

To secure the Obligations, Grantor grants Lender a security interest in all of Grantor’s right, title and interest in its Intellectual Property. Grantor hereby confirms that the attached schedules of Grantor’s copyright, patent and trademark applications and registrations, which are registered or filed with the United States Patent and Trademark Office or the United States Copyright Office, as applicable, attached hereto as Exhibits A, B and C hereto, respectively, are complete and accurate as of the date hereof.

Grantor hereby authorizes Lender to (a) modify this Agreement unilaterally by amending the exhibits to this Agreement to include any Intellectual Property which Grantor obtains subsequent to the date of this Agreement, and (b) file a duplicate of this Agreement containing amended exhibits reflecting such new Intellectual Property.

This Agreement shall be exclusively (without regard to any rules or principles relating to conflicts of laws) governed by, enforced and construed in accordance with the laws of the state of California and the federal laws of the United States applicable therein. This Agreement may be executed in counterparts, each of which shall be deemed an original but all of which together shall constitute the same instrument.

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

Address of Grantor:

ESILICON CORPORATION

2130 Gold Street, Suite 100
San Jose, CA 95002
Attn: Chief Financial Officer; General Counsel
Email: ~~pmorali@esilicon.com~~
cgartin@esilicon.com

By: Philippe Morali
Title: CEO
Name: Philippe Morali

LENDER:

Address of Lender:

RUNWAY GROWTH CREDIT FUND INC.

2925 Woodside Road
Woodside, CA 94062
Attention: David Spreng
Email: dspreng@gsvgc.com

By: _____
Title: _____
Name: _____

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

Address of Grantor:

ESILICON CORPORATION

2130 Gold Street, Suite 100
San Jose, CA 95002
Attn: Chief Financial Officer; General Counsel
Email: ~~pm@mail@esilicon.com~~
cgartin@esilicon.com

By: _____

Title: _____

Name: _____

LENDER:

Address of Lender:

RUNWAY GROWTH CREDIT FUND INC.

2925 Woodside Road
Woodside, CA 94062
Attention: David Spreng
Email: dspreng@gsvgc.com

By:  _____

Title: CFO

Name: DAVID SPRENG

EXHIBIT A

Copyrights

| Description | Registration Number | Registration Date |
|--|----------------------------|--------------------------|
| Component Auto-generator System for Test Chip: End-User Manual, Version 1.0. | TX0007537285 | 06/05/2012 |

EXHIBIT B

Patents

| Description | Patent / Application Number | Issue / Application Date |
|--|------------------------------------|---------------------------------|
| Duo content addressable memory (CAM) using a single CAM | 9,711,220 | 07/18/17 |
| Error detection and correction in binary content addressable memory (BCAM) | 9,529,669 | 12/27/16 |
| Parallel signal via structure | 9,461,000 | 10/04/16 |
| Scaling of integrated circuit design including high-level logic components | 9,460,257 | 10/04/16 |
| Integrated circuit design scaling for recommending design point | 9,460,256 | 10/04/16 |
| Scaling of integrated circuit design including logic and memory components | 9,460,255 | 10/04/16 |
| Scaling logic components of integrated circuit design | 9,460,254 | 10/04/16 |
| Integrated circuit design optimization | 9,454,636 | 09/27/16 |
| Scaling memory components of integrated circuit design | 9,454,628 | 09/27/16 |
| Testing of thru-silicon vias | 9,435,846 | 09/06/16 |
| Mixed-sized pillars that are probeable and routable | 9,263,409 | 02/16/16 |
| Variability-aware scheme for high-performance asynchronous circuit voltage regulation | 8,572,539 | 10/29/13 |
| Network of tightly coupled performance monitors for determining the maximum frequency of operation of a semiconductor IC | 8,446,224 | 05/21/13 |
| Asynchronous scheme for clock domain crossing | 8,433,875 | 04/30/13 |
| Pushed-rule bit cells with new functionality | 8,355,269 | 01/15/13 |
| System and method for automating integration of semiconductor work in progress updates | 7,756,598 | 07/13/10 |
| Variability-aware scheme for asynchronous circuit initialization | 7,701,255 | 04/20/10 |
| Crossbar switch with grouped inputs and outputs | 7,603,509 | 10/13/09 |
| System and method for automating integration of semiconductor work in progress updates | 7,474,933 | 01/06/09 |
| Prediction based optimization of a semiconductor supply chain using an adaptive real time work-in-progress tracking system | 7,218,980 | 05/15/07 |

| | | |
|--|------------|----------|
| Method and apparatus for distribution of bandwidth in a switch | 7,215,678 | 05/8/07 |
| Method and flow control in a switch and a switch controlled thereby | 7,061,868 | 06/13/06 |
| Apparatus and method for converting data in serial format to parallel format and vice versa | 7,016,346 | 03/21/06 |
| Device for datastream decoding | 7,158,529 | 01/02/07 |
| Device for datastream decoding | 7,002,983 | 02/21/06 |
| Method and arrangement for managing packet queues in switches | 6,977,940 | 12/20/05 |
| Scheduler method and device in a switch | 6,944,171 | 09/13/05 |
| Queue management system performing one read one write during one cycle by using free queues | 6,754,742 | 06/22/04 |
| Adaptive real-time work-in-progress tracking, prediction, and optimization system for a semiconductor supply chain | 6,748,287 | 06/08/04 |
| Multicasting method and arrangement | 6,625,151 | 09/23/03 |
| Apparatus and method for self-synchronization of data to a local clock | 6,604,203 | 08/05/03 |
| Method and apparatus for content addressable memory with a partitioned match line | 6,477,071 | 11/05/02 |
| CAM/RAM memory device with a scalable structure | 6,330,177 | 12/11/01 |
| Mask arrangement for scramble CAM/RAM structures | 6,134,135 | 10/17/00 |
| Wireless probes | 14/963,076 | 12/08/15 |
| Elongated pad structure | 14/963,081 | 12/08/15 |
| Communication interface architecture using serializer/deserializer | 14/810,261 | 07/27/15 |
| Scaling of integrated circuit design including high-level logic components | 15/250,885 | 08/29/16 |
| Memory optimization in VLSI design using generic memory models | 14/628,105 | 02/20/15 |
| Generating specific memory models using generic memory models for design memories in VLSI | 14/628,668 | 02/23/15 |
| Designing memories in VLSI design using specific memory models generated from generic memory | 14/628,676 | 02/23/15 |
| Error detection and correction in ternary content addressable memory (TCAM) | 14/502,954 | 09/30/14 |

EXHIBIT C

Trademarks

| Description | Registration/ Serial Number | Registration/ Application Date |
|--------------------|--|---|
| ESILICON | 2,969,847 | 07/19/05 |
| ESILICON ACCESS | 3,603,342 | 04/07/09 |
| ESILICON | 3,412,021 | 04/15/08 |
| ESILICON | 3,591,594 | 03/17/09 |