TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

ETAS ID: TM445626

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
Western Alliance Bank	FORMERLY Bridge Bank, National Association	10/03/2017	Corporation: ARIZONA

RECEIVING PARTY DATA

Name:	Adesto Technologies Corporation
Street Address:	1250 Borregas Avenue
City:	Sunnyvale
State/Country:	CALIFORNIA
Postal Code:	94089
Entity Type:	Corporation: DELAWARE
Name:	Artemis Acquisition LLC
Street Address:	1250 Borregas Avenue
City:	Sunnyvale
State/Country:	CALIFORNIA
Postal Code:	94089
Entity Type:	Limited Liability Company: CALIFORNIA

PROPERTY NUMBERS Total: 3

Property Type	Number	Word Mark
Serial Number:	85470695	ADESTO
Serial Number:	85470629	ADESTO TECHNOLOGIES
Serial Number:	85470550	CBRAM

CH $90.00 85470695

CORRESPONDENCE DATA

Fax Number: 6196992701

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 619-699-2700
Email: derek.monteblanco@dlapiper.com
Correspondent Name: DLA Piper LLP (US)
Address Line 1: 401 B Street, Suite 1700
Address Line 4: San Diego, CALIFORNIA 92101

NAME OF SUBMITTER:	Matt Schwartz

SIGNATURE:	/s/ Matt Schwartz
DATE SIGNED:	10/03/2017

Total Attachments: 5
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REASSIGNMENT AND RELEASE OF SECURITY INTEREST

This Reassignment and Release of Security Interest is executed as of October 3, 2017 by WESTERN ALLIANCE BANK, an Arizona corporation, successor-in-interest to BRIDGE BANK, NATIONAL ASSOCIATION (the "Assignor") for the benefit of ADESTO TECHNOLOGIES CORPORATION, a Delaware corporation and ARTEMIS ACQUISITION LLC, a California limited liability company (each an "Assignee" and together, the "Assignees"), with the principal executive office located at 1250 Borregas Avenue, Sunnyvale, California 94089.

RECITALS

A. WHEREAS, Assignees assigned certain interests in the intellectual property described on Exhibit A and Exhibit B (together, the "Intellectual Property") to Assignor pursuant to a certain Intellectual Property Security Agreement dated as of October 4, 2013 and recorded with the U.S. Patent and Trademark Office.

B. WHEREAS, Assignor wishes to release and reassign all interest that such Assignor may have in the Intellectual Property.

AGREEMENT

Now, therefore, Assignor agrees that it releases its security interest in the Intellectual Property and reassigns to Assignees, without warranty or recourse, all interest of Assignor in and to the Intellectual Property.

ASSIGNOR:

WESTERN ALLIANCE BANK

By: _____

Name: Lisa Ghent

Title: VP Relationship Manager

Address:

55 Almaden Boulevard, Suite 100
San Jose, CA 95113

EXHIBIT A

Trademarks

Title	Serial/Registration No.	File Date
ADESTO	85470695	11/11/11
ADESTO TECHNOLOGIES	85470629	11/11/11
CBRAM	85470550	11/11/11

EXHIBIT B

Patents

Title	Patent/Serial No.	Issue/Filing Date
Low power voltage regulator circuit for use in an integrated circuit device	6320454	11/20/01
Reference cell for high speed sensing in non-volatile memories	6411549	6/25/02
Method of establishing reference levels for sensing multilevel memory cell states	6618297	9/9/03
Row decoder circuit for use in programming a memory device	6621745	9/16/03
Method of programming a multi-level memory device	6714448	3/30/04
Method of recovering overerased bits in a memory device	6724662	4/20/04
Approach for zero dummy byte flash memory read operation	6879535	4/12/05
Method for identification of SPI compatible serial memory devices	7032039	4/18/06
Dual stage voltage regulation circuit	7064529	6/20/06
Functional register decoding system for multiple plane operation	7099226	8/29/06
Method and apparatus of a smart decoding scheme for fast synchronous read in a memory system	7143257	11/28/06
Column/sector redundancy CAM fast programming scheme using regular memory core array in multi-plane flash memory device	7196952	3/27/07
Method for fabricating a semiconductor memory cell	7214587	5/8/07
Semiconductor memory component in cross-point architecture	7215564	5/8/07
Resistive memory arrangement	7215568	5/8/07
PMC memory circuit and method for storing a datum in a PMC memory circuit	7257014	8/14/07
Integrated semiconductor memory with an arrangement of nonvolatile memory cells, and method	7277312	10/2/07
Redundant column read in a memory array	7296196	11/13/07
A memory device including electrical circuit configured to provide reversible bias across the PMC memory cell to perform erase and write functions	7327603	2/5/08
Memory system and process for controlling a memory component to achieve different kinds of memory characteristics on one and the same memory component	7337282	2/26/08
Read, write and erase circuit for programmable memory devices	7359236	4/15/08
Method for fabricating a resistive memory	7368314	5/6/08
Memory having CBRAM memory cells and method	7372716	5/13/08
Channel discharging after erasing flash memory devices	7397699	7/8/08
Programmable memory device circuit	7426131	9/16/08
Read, write and erase circuit for programmable memory devices	7483294	1/27/09
Voltage reference circuit using programmable metallization cells	7514706	4/7/09
Resistively switching memory	7442605	10/28/08

Method for preventing over-erasing of unused column redundant memory cells in a flash memory having single-transistor memory cells	7457167	11/25/08
Method for improving the thermal characteristics of semiconductor memory cells	7483293	1/27/09
Resistive memory element with shortened erase time	7511294	3/31/09
Method and system for reducing soft-writing in a multi-level flash memory	7522455	4/21/09
Integrated circuit including resistivity changing memory cells	7538411	5/26/09
Implementation of column redundancy for a flash memory with a high write parallelism	7551498	6/23/09
Resistive memory arrangement	7561460	7/14/09
Memory cell, memory device and method for the production thereof	7655939	2/2/10
Method for fabricating an integrated device comprising a structure with a solid electrolyte	7700398	4/20/10
A memory device including electrical circuit configured to provide reversible bias across the PMC memory cell to perform erase and write functions	7715226	5/11/10
Method for manufacturing a CBRAM semiconductor memory	7718537	5/18/10
Memory component with memory cells having changeable resistance and fabrication method therefor	7737428	6/15/10
NOR and NAND memory arrangement of resistive memory elements	7746683	6/29/10
Method for manufacturing an integrated circuit including an electrolyte material layer	7749805	7/6/10
Device and method for access time reduction by speculatively decoding non-memory read commands on a serial interface	7769909	8/3/10
Solid electrolyte memory element and method for fabricating such a memory element	7772614	8/10/10
Method for producing memory having a solid electrolyte material region	7829134	11/9/10
Method and system to access memory	7929356	4/19/11
Method for producing memory having a solid electrolyte material region	8062694	11/22/11
Integrated circuits having programmable metallization cells (PMCS) and operating methods therefor	8107273	1/31/12
Method and system to access memory	8208315	6/26/12
Variable impedance memory device having simultaneous program and erase, and corresponding methods and circuits	8274842	9/25/12
Programmable impedance element circuits and methods	8294488	10/23/12
PMC-based non-volatile CAM	8320148	11/27/12
Reconfigurable memory arrays having programmable impedance elements and corresponding methods	8331128	12/11/12
Methods of programming and erasing programmable metallization cells (PMCS)	8369132	2/5/13
Memory cell device and method of manufacture	8420481	4/16/13

Conducting bridge random access memory (CBRAM) device structures	8426839	4/23/13
Methods and circuits for temperature varying write operations of programmable impedance elements	8437171	5/7/13
Variable impedance memory device biasing circuits and methods	8498164	7/30/13
Method for operating an integrated circuit having a resistivity changing memory cell	8531863	9/10/13
Conductive filament based memory elements and methods with improved data retention and/or endurance	8531867	9/10/13
Contact structure and method for variable impedance memory element	8816314	8/26/14
Resistive switching devices having alloyed electrodes and methods of formation thereof	8847192	9/30/14
Resistive switching devices and methods of formation thereof	8941089	1/27/15
Resistive switching element	11746393	5/9/07
Current sense amplifier	6946882	9/20/05
CBRAM cell and CBRAM array, and method of operating thereof	7515454	4/7/09
Method for fabricating a solid electrolyte memory device and solid electrolyte memory device	7658773	2/9/10
Integrated circuit, method for manufacturing an integrated circuit, memory cell array, memory module, and device	7732888	6/8/10
Method of manufacturing an integrated circuit, an integrated circuit and a memory module	7888228	2/15/11
Methods of manufacturing a semiconductor device; method of manufacturing a memory cell; semiconductor device; semiconductor processing device; integrated circuit having a memory cell	8268664	9/18/12
Storage elements, structures and methods having edgeless features for programmable layer(s)	9412945	8/9/16
Memory cells with an anode comprising intercalating material and metal species dispersed therein	8115282	2/14/12