TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

ETAS ID: TM492889

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
QuickLogic Corporation		09/28/2018	Corporation: DELAWARE

RECEIVING PARTY DATA

Name:	Heritage Bank of Commerce
Street Address:	150 South Almaden Boulevard
Internal Address:	Attn: Mike Hansen
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95113
Entity Type:	Corporation: CALIFORNIA

PROPERTY NUMBERS Total: 6

Property Type	Number	Word Mark
Serial Number:	86385990	QUICKLOGIC
Serial Number:	86385987	QUICKLOGIC
Serial Number:	78481189	QUICKLOGIC
Serial Number:	77084189	ARCTICLINK
Serial Number:	74030976	PASIC
Serial Number:	74030945	VIALINK

CH $165.00 86385990

CORRESPONDENCE DATA

Fax Number: 8586385130

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 619-699-2700
Email: susan.reynholds@dlapiper.com
Correspondent Name: DLA Piper LLP (US)
Address Line 1: 401 B Street, Suite 1700
Address Line 4: San Diego, CALIFORNIA 92101

NAME OF SUBMITTER:	Matt Schwartz
SIGNATURE:	/s/ Matt Schwartz
DATE SIGNED:	10/05/2018

Total Attachments: 8
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INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement (this "Agreement") is entered into as of September 28, 2018 by and between HERITAGE BANK OF COMMERCE, a California corporation ("Bank") and QUICKLOGIC CORPORATION, a Delaware corporation ("Borrower").

RECITALS

Bank has agreed to make certain advances of money and to extend certain financial accommodations to Borrower under that certain Loan and Security Agreement by and between Bank and Borrower dated of even date herewith (as amended, supplemented, modified and/or restated from time to time, the "Loan Agreement"). Capitalized terms used herein are used as defined in the Loan Agreement. Pursuant to the terms of the Loan Agreement, Borrower has granted to Bank a security interest in its personal property.

NOW, THEREFORE, Borrower agrees as follows:

AGREEMENT

To secure its obligations under the Loan Agreement and under any other agreement now existing or hereafter arising between Borrower and Bank, Borrower grants to Bank a security interest in all of Borrower's right, title and interest in, its Intellectual Property (including without limitation those Copyrights, Patents and Trademarks listed on Schedules A, B and C attached hereto) and all proceeds thereof (such as, by way of example but not by way of limitation, license royalties and proceeds of infringement suits), the right to sue for past, present and future infringements, all rights corresponding thereto throughout the world and all re-issues, divisions continuations, renewals, extensions and continuations-in-part thereof. Borrower represents and warrants that Schedules A, B, and C attached hereto set forth any and all Intellectual Property rights in connection to which Borrower has registered or filed an application with either the United States Patent and Trademark Office or the United States Copyright Office, as applicable.

Borrower authorizes the Commissioner for Patents, the Commissioner for Trademarks and the Register of Copyrights and any other government officials to record and register this Agreement upon request by Bank.

Borrower hereby authorizes Bank to (a) modify this Agreement unilaterally by amending the exhibits to this Agreement to include any Intellectual Property which Borrower obtains subsequent to the date of this Agreement, and (b) file a duplicate original of this Agreement containing amended exhibits reflecting such new Intellectual Property.

This Agreement may be executed in two or more counterparts, each of which shall be deemed an original but all of which together shall constitute the same instrument.

Bank's remedies hereunder are set forth in Section 9 of the Loan Agreement.

[signature page follows]

IN WITNESS WHEREOF, the parties hereto have caused this Intellectual Property Security Agreement to be duly executed by authorized officers as of the first date written above.

Address of Borrower:

1277 Orleans Drive, Sunnyvale
California 94089-1138
Attn: Sue Cheung
Fax: (408) 990-4040
Email: scheung@quicklogic.com

BORROWER

QUICKLOGIC CORPORATION

By: _____
Name: Suping (Sue) Cheung
Title: CFO & Secretary

Address of Bank:

150 South Almaden Blvd.
San Jose, CA, 95113
Attn: Mike Hansen
Fax: (408) 947-6910
Email: Mike.Hansen@herbank.com

BANK

HERITAGE BANK OF COMMERCE

By: _____
Name: _____
Title: _____

IN WITNESS WHEREOF, the parties hereto have caused this Intellectual Property Security Agreement to be duly executed by authorized officers as of the first date written above.

Address of Borrower:

1277 Orleans Drive, Sunnyvale
California 94089-1138
Attn: Sue Cheung
Fax: (408) 990-4040
Email: scheung@quicklogic.com

BORROWER

QUICKLOGIC CORPORATION

By:_____
Name:_____
Title:_____

Address of Bank:

150 South Almaden Blvd.
San Jose, CA, 95113
Attn: Mike Hansen
Fax: (408) 947-6910
Email: Mike.Hansen@herbank.com

BANK

HERITAGE BANK OF COMMERCE

By: [signature]
Name: [illegible] SCHRADER
Title: VP

[Signature Page to Intellectual Property Security Agreement]

SCHEDULE A

Copyrights

If None, check this box: ☒

Description	Registration Number	Registration Date

SCHEDULE B

Patents

If None, check this box: ☐

Description	Patent/Application Number	Issue /Application Date
Assigning operational codes to lists of values of control signals selected from a processor design based on end-user software	9811335	11/7/17
Local routing network with selective fast paths for programmable logic device	9628083	4/18/17
Logic cell for programmable logic device	9,287,868	3/15/16
Routing network for programmable logic device	9118325	8/25/15
Adjustable interface buffer circuit between a programmable logic device and a dedicated device	8487652	7/16/13
PHY-less ULPI and UTMI bridges	8261002	9/4/12
FPGA programming structure for ATPG test coverage	8091001	1/3/12
Adjustable interface buffer circuit between a programmable logic device and a dedicated device	8018248	9/13/11
Low power mode	7646216	1/12/10
Programmable multiplexer	7482834	1/27/09
Dynamic clock control	7443222	10/28/08
Method of programming an antifuse	7187228	3/6/07
Differential charge pump	7184510	2/27/07
Programmable antifuse interfacing a programmable logic and a dedicated device	6552410	4/22/03
Serializer/deserializer embedded in a programmable device	6542096	4/1/03
Programmable device with an embedded portion for receiving a standard circuit design	6519753	2/11/03
Metal-to-metal antifuse with non-conductive diffusion barrier	6515343	2/4/03
Method of forming a metal-to-metal antifuse with non-conductive diffusion barrier	6509209	1/21/03
Configurable computational unit embedded in a programmable device	6483343	11/19/02
Architecture for field programmable gate array	6426649	7/30/02
Techniques and circuits for high yield improvements in programmable devices using redundant logic	6347378	2/12/02
Bond pad having vias usable with antifuse process technology	6300688	10/9/01
Techniques and circuits for high yield improvements in programmable devices using redundant routing resources	6237131	5/22/01
Virtual programmable device and method of programming	6188242	2/13/01
Programming architecture for field programmable gate array	6169416	1/2/01
Protection of logic modules in a field programmable gate array during antifuse programming	6157207	12/5/00
Programmable device having antifuses without programmable material edges and/or corners underneath metal	6154054	11/28/00
Method for fabrication of programmable interconnect structure	6150199	11/21/00
Techniques and circuits for high yield improvements in programmable devices using redundant logic	6148390	11/14/00
Charge pumps of antifuse programming circuitry powered from high voltage compatibility terminal	6140837	10/31/00
Programmable integrated circuit having a test circuit for testing the integrity of routing resource structures	6130554	10/10/00
Field programmable gate array having internal logic transistors with two different gate insulator thicknesses	6127845	10/3/00
Metal-to-metal antifuse having improved barrier layer	6107165	8/22/00
Power-up circuit for field programmable gate arrays	6101074	8/8/00
Precharge circuitry in RAM circuit	6097651	8/1/00

Description	Patent/Application Number	Issue /Application Date
Programmable interconnect structures and programmable integrated circuits	6097077	8/1/00
Programmable integrated circuit having shared programming conductors between columns of logic modules	6084428	7/4/00
Field programmable gate array having testable antifuse programming architecture and method therefore	6081129	6/27/00
Programmable application specific integrated circuit and logic cell	6078191	6/20/00
Three-statable net driver for antifuse field programmable gate array	6028444	2/22/00
Programmable integrated circuit having parallel routing conductors coupled to programming drivers in different locations	6018251	1/25/00
Programmable integrated circuit having a routing conductor that is driven with programming current from two different programming voltage terminals	6011408	1/4/00
Method for fabrication of programmable interconnect structure	5989943	11/23/99
Programmable integrated circuit having L-shaped programming power buses that extend along sides of the integrated circuit	5986469	11/16/99
Programmable application specific integrated circuit and logic cell therefor	5986468	11/16/99
Programming architecture for a programmable integrated circuit employing test antifuses and test transistors	5966028	10/12/99
Programmable device having antifuses without programmable material edges and/or corners underneath metal	5955751	9/21/99
Techniques and circuits for high yield improvements in programmable devices using redundant routing resources	5925920	7/20/99
Interface cell for a programmable integrated circuit employing antifuses	5900742	5/4/99
Security antifuse that prevents readout of some but not other information from a programmed field programmable gate array	5898776	4/27/99
Programmable application specific integrated circuit employing antifuses and methods therefor	5892684	4/6/99
Clock network for field programmable gate array	5892370	4/6/99
Programmable interconnect structures and programmable integrated circuits	5880512	3/9/99
Programming architecture for a programmable integrated circuit employing antifuses	5859543	1/12/99
Method for forming programmable interconnect structures and programmable integrated circuits	5786268	7/28/98
Power-up circuit for field programmable gate arrays	5828538	10/27/98
Electrically programmable interconnect structure having a PECVD amorphous silicon element	5780919	7/14/98
Reducing propagation delays in a programmable device	5729468	3/17/98
Programmable application specific integrated circuit and logic cell therefor	5726586	3/10/98
Field programmable gate array having reproducible metal-to-metal amorphous silicon antifuses	5717230	2/10/98
Programmable interconnect structures and programmable integrated circuits	5701027	12/23/97
Logic module for field programmable gate array	5682106	10/28/97
Estimating propagation delays in a programmable device	5675502	10/7/97
Reducing programming time of a field programmable gate array employing antifuses	5661412	8/26/97
Programmable application specific integrated circuit employing antifuses and methods therefor	5654649	8/5/97
Integrated circuit facilitating simultaneous programming of multiple antifuses	5600262	2/4/97
Programmable application specific integrated circuit and logic cell therefor	5594364	1/14/97

Description	Patent/Application Number	Issue /Application Date
Programmable application specific integrated circuit and logic cell therefor	5587669	12/24/96
Programmable interconnect structures and programmable integrated circuits	5557136	9/17/96
Method for simultaneous programming of multiple antifuses	5552720	9/3/96
Programmed programmable device and method for programming antifuses of a programmable device	5544070	8/6/96
Select set-based technology mapping method and apparatus	5526276	6/11/96
Electrically programmable interconnect structure having a PECVD amorphous silicon element	5502315	3/26/96
Integrated circuit facilitating simultaneous programming of multiple antifuses	5495181	2/27/96
Programmable application specific integrated circuit using logic circuits to program antifuses therein	5477167	12/19/95
Programming of antifuses	5471154	11/28/95
Method and apparatus for programming anti-fuse devices	5469109	11/21/95
Field programmable antifuse device and programming method therefor	5469077	11/21/95
Method and apparatus for programming anti-fuse devices	5448184	9/5/95
Programmable application specific integrated circuit and logic cell therefor	5430390	7/4/95
Programmable application specific integrated circuit employing antifuses and methods therefor	5424655	6/13/95
Programmable application specific integrated circuit and logic cell therefor	5416367	5/16/65
Programming of antifuses	5397939	3/14/95
Programmable application specific integrated circuit and logic cell therefor	5396127	3/7/95
Programmable interconnect structures and programmable integrated circuits	5362676	11/8/94
Field programmable antifuse device and programming method therefor	5327024	7/5/94
Programmable interconnect structures and programmable integrated circuits	5319238	6/7/94
Programming of antifuses	5302546	4/12/94
Method of determining an electrical characteristic of an antifuse and apparatus therefor	5293133	3/8/94
Programmable application specific integrated circuit and logic cell therefor	5280202	1/18/94
Programming of antifuses	5243226	9/7/93
Programmable application specific integrated circuit and logic cell therefor	5220213	6/15/93
Programmable interconnect structures and programmable integrated circuits	5196724	3/23/93
Programmable application specific integrated circuit and logic cell therefor	5122685	6/16/92
Multiple axis wrist worn pedometer	14602188	1/21/15
Heart rate monitor	15054022	2/25/16
Sensor hub batch packing	15163474	5/24/16
Switchable power islands having configurably on routing paths	15658206	7/24/17

SCHEDULE C

Trademarks

If None, check this box; □

Description	Serial / Registration Number	Application / Registration Date
QUICKLOGIC	86385990	9/4/14
QUICKLOGIC	86385987	9/4/14
QUICKLOGIC	78481189	9/9/04
ARCTICLINK	77084189	1/16/07
PASIC	74030976	2/20/90
VIALINK	74030945	2/20/90