### TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1 Stylesheet Version v1.2 ETAS ID: TM532179

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

### **CONVEYING PARTY DATA**

Name	Formerly	Execution Date	Entity Type
JPMORGAN CHASE BANK, N.A., AS ADMINISTRATIVE AGENT		07/16/2019	National Banking Association: UNITED STATES

### **RECEIVING PARTY DATA**

Name:	VISHAY DALE ELECTRONICS, INC.
Street Address:	1122 23RD STREET
City:	COLUMBUS
State/Country:	NEBRASKA
Postal Code:	68601-3647
Entity Type:	Corporation: DELAWARE
Name:	VISHAY INTERTECHNOLOGY, INC.
Street Address:	63 LANCASTER AVENUE
City:	MALVERN
State/Country:	PENNSYLVANIA
Postal Code:	19355
Entity Type:	Corporation: DELAWARE
Name:	SILICONIX INCORPORATED
Street Address:	2585 JUNCTION AVENUE
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95134
Entity Type:	Corporation: DELAWARE
Name:	VISHAY SILICONIX TECHNOLOGY C.V.
Street Address:	2585 JUNCTION AVENUE
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95134
Entity Type:	Corporation: DELAWARE
Name:	VISHAY SPRAGUE, INC.
Street Address:	2813 WEST ROAD
City:	BENNINGTON
	TRADEMARK

REEL: 006695 FRAME: 0221 900506861

State/Country:	VERMONT
Postal Code:	05201
Entity Type:	Corporation: DELAWARE
Name:	VISHAY THIN FILM, LLC
Street Address:	2813 WEST ROAD
City:	BENNINGTON
State/Country:	VERMONT
Postal Code:	05201
Entity Type:	Limited Liability Company: DELAWARE

### **PROPERTY NUMBERS Total: 45**

Property Type	Number	Word Mark
Registration Number:	1383220	DALE
Registration Number:	3394307	IHLP
Registration Number:	2074628	POWER METAL STRIP
Registration Number:	3431324	WSL
Registration Number:	3264991	WSR
Registration Number:	2602606	FUNCTIONPAK
Registration Number:	1979712	QUICK-NET
Registration Number:	1790212	VISHAY
Registration Number:	1015163	VISHAY
Registration Number:	837476	VISHAY
Registration Number:	3530560	VISHAY
Registration Number:	1692580	VISHAY
Registration Number:	3530559	VISHAY
Registration Number:	1687032	VISHAY
Registration Number:	1689517	VISHAY INTERTECHNOLOGY
Registration Number:	3256028	TMBS
Registration Number:	2696001	CHIPFET
Registration Number:	1727230	LITTLE FOOT
Registration Number:	2701037	MICRO FOOT
Registration Number:	2990388	POLARPAK
Registration Number:	3732445	POWERPAIR
Registration Number:	3087499	SI
Registration Number:	3469285	SKYFET
Registration Number:	2035560	TRENCHFET
Registration Number:	2672428	POWERPAK
Registration Number:	3759042	TURBOFET
Registration Number:	3073909	FLIPKY

Property Type	Number	Word Mark
Registration Number:	1753724	HEXFRED
Registration Number:	3704345	POWERTAB
Registration Number:	3662946	FRED PT
Registration Number:	3256019	HVARC GUARD
Registration Number:	3526660	MICROTAN
Registration Number:	858837	SPECTROL
Registration Number:	859975	SPRAGUE
Registration Number:	1492049	SUPERTAN
Registration Number:	1380243	TANTAMOUNT
Registration Number:	1238139	VITRAMON
Registration Number:	839908	VITRAMON
Registration Number:	3762167	SPRAGUE
Registration Number:	2126097	CBTV
Serial Number:	77953395	VISHAY PRECISION GROUP
Serial Number:	77952995	VISHAY PRECISION GROUP
Serial Number:	77900236	MICROBUCK
Serial Number:	77896876	VRPOWER
Serial Number:	77945647	THUNDERFET

### **CORRESPONDENCE DATA**

**Fax Number:** 8004947512

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

**Phone:** 202-370-4756

**Email:** ipteam@cogencyglobal.com

Correspondent Name: Jay daSilva

Address Line 1: 1025 Vermont Ave NW, Suite 1130

Address Line 2: COGENCY GLOBAL INC.

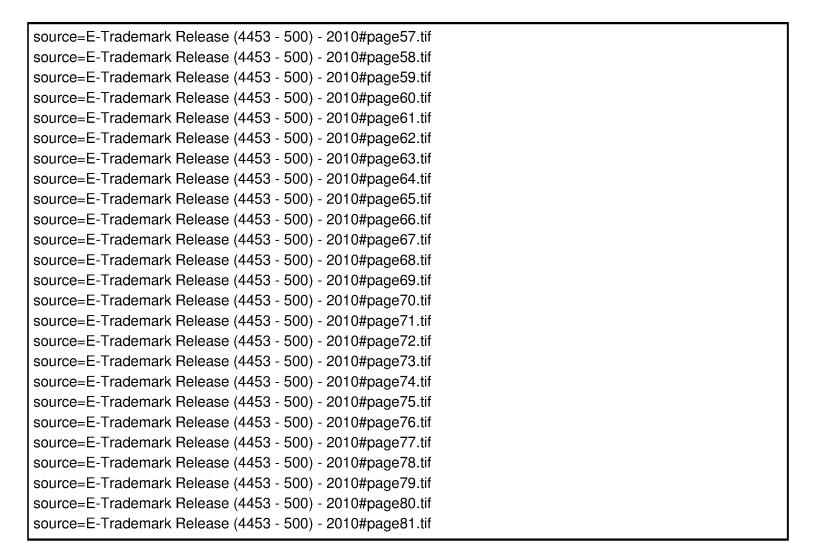
Address Line 4: Washington, D.C. 20005

ATTORNEY DOCKET NUMBER:	1107704 TM REL E
NAME OF SUBMITTER:	Elizabeth Wagenbach
SIGNATURE:	/Elizabeth Wagenbach/
DATE SIGNED:	07/17/2019

### **Total Attachments: 79**

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RELEASE OF SECURITY INTEREST IN PATENTS AND TRADEMARKS, dated as of July 16, 2019 (this "Release"), by JPMORGAN CHASE BANK, N.A., as Administrative Agent.

- A. Reference is made to (i) the Credit Agreement dated as of December 1, 2010, as amended and restated as of August 8, 2013, as further amended and restated as of December 10, 2015 (as further amended, restated, supplemented or otherwise modified from time to time, the "Credit Agreement"), among Vishay Intertechnology, Inc., a Delaware corporation (the "Borrower"), the Subsidiary Borrowers from time to time party thereto, the Lenders from time to time party thereto and JPMorgan Chase Bank, N.A., as administrative agent, (ii) the Guarantee and Collateral Agreement dated as of December 1, 2010, as amended by that certain Reaffirmation Agreement dated as of August 8, 2013 among the Borrower, the subsidiaries of the Borrower party thereto and JPMorgan Chase Bank, N.A., as administrative agent (as further amended, restated, supplemented or otherwise modified from time to time, the "Collateral Agreement"), among the Borrower, the Domestic Subsidiary Loan Parties from time to time party thereto and JPMorgan Chase Bank, N.A., as administrative agent (in such capacity, the "Administrative Agent"), and (iii) the Patent and Trademark Security Agreements dated as of December 1, 2010, August 8, 2013 and December 10, 2015, in each case, among the Borrower, the Domestic Subsidiaries of the Borrower from time to time party thereto (together with the Borrower, the "Grantors") and the Administrative Agent (the documents set forth in clauses (ii) and (iii) above, the "Security Agreements" and each a "Security Agreement").
- B. Pursuant to the Security Agreements, the Grantors granted to the Administrative Agent, for the benefit of the Secured Parties, a security interest in all right, title and interest of the Grantors in, among other things, the patents and trademarks set forth on Schedule I hereto (the "Patent and Trademark Collateral"), which security interests were recorded with the United States Patent and Trademark Office on (i) January 14, 2011 at Reel/Frame 004453/0500, (ii) January 21, 2011 at Reel/Frame 025675/0001, (iii) September 5, 2013 at Reel/Frame 031170/0001, (iv) September 5, 2013 at Reel/Frame 5105/0896, (v) December 10, 2015 at Reel/Frame 037261/0616 and (vi) December 10, 2015 at Reel/Frame 5686/0277.
- C. Pursuant to the Payoff Letter dated as of June 5, 2019, between the Borrower and the Administrative Agent, the Administrative Agent agreed to release any and all security interests it may have in the Patent and Trademark Collateral pursuant to the Security Agreements.

Accordingly, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the Administrative Agent, on behalf of the Secured Parties, does hereby state as follows:

SECTION 1. <u>Terms</u>. Each capitalized term used but not otherwise defined herein shall have the meaning specified in the Credit Agreement or the applicable Security Agreement.

[[5202801]]

SECTION 2. <u>Release</u>. The Administrative Agent, on behalf of itself, the Secured Parties and their permitted successors and assigns, does hereby terminate, release, relinquish and discharge its and their security interest granted under the Security Agreements in the Patent and Trademark Collateral and any right, title or interest granted under the Security Agreements it has in the Patent and Trademark Collateral shall hereby cease and become void. This Release is made without representation or warranty, express or implied, of any kind, by, or recourse to, the Administrative Agent or any other Secured Party.

THIS RELEASE SHALL BE CONSTRUED IN ACCORDANCE WITH AND GOVERNED BY THE LAWS OF THE STATE OF NEW YORK.

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[[5202801]]

IN WITNESS WHEREOF, the Administrative Agent has caused this Release to be duly executed as of the day and year first above written.

JPMORGAN CHASE BANK, N.A., as

Administrative Agent,

by

Name: Title: Daglas P Panchal Executive Director

[Signature Page - Release of Security Interest in Patents and Trademarks]

### SCHEDULE I

[See attached]

[[5202801]]

# Patents and Trademarks of Vishay Dale Electronics, Inc.

## U.S. Patent Registrations and Patent Applications

(a)

Type	Serial No.	Patent No.	Title: (Patent Description)	Status	File Date	Issue Date	Domestic Loan Party
UTL	08/963,224	6,204,744	HIGH CURRENT, LOW PROFILE INDUCTOR	ISSUED	11/3/1997	3/20/2001	Vishay Dale Electronics, Inc.
UTL	09/547,155	6,460,244	METHOD FOR MAKING A HIGH CURRENT LOW PROFILE INDUCTOR	ISSUED	4/11/2000	10/8/2002	Vishay Dale Electronics, Inc.
TTU	08/350,960	5,604,477	SURFACE MOUNT RESISTOR AND METHOD FOR MAKING SAME	ISSUED	12/7/1994	2/18/1997	Dale Electronics, Inc.
UTL	07/860,403	5,287,083	BULK METAL CHIP RESISTOR	ISSUED	3/30/1992	2/15/1994	Dale Electronics, Inc.
UTI	07/881,856	5,302,932	MONOLYTHIC MULTILAYER CHIP INDUCTOR AND METHOD FOR MAKING SAME	ISSUED	5/12/1992	4/12/1994	Dale Electronics, Inc.
UTL	08/665,788	5,986,533	MONOLITHIC THICK FILM INDUCTOR METHOD FOR MAKING SAME	ISSUED	6/18/1996	11/16/1999	Dale Electronics, Inc.
UTL	08/881,480	5,970,604	METHOD OF MAKING A MONOLITHIC THICK FILM INDUCTOR	ISSUED	6/24/1997	10/26/1999	Dale Electronics, Inc.
UTL	08/936,193	5,922,514	THICK FILM LOW VALUE HIGH FREQUENCY INDUCTOR, AND METHOD OF MAKING THE SAME	ISSUED	9/17/1997	7/13/1999	Dale Electronics, Inc.

12/11/2006

UTL	UTL	UTL	UTL	UTL	UTL	TTU	UTL	TTU	UTL	Туре
09/774,854	09/474,448	09/471,617	10/797,866	10/078,311	09/715,252	09/471,622	12/535,757	12/013,725	11/782,020	e Serial No.
6,587,025	6,181,234	6,510,605	6,901,655	6,725,529	6,441,718	6,401,329			7,345,562	Patent No.
SIDE-BY-SIDE COIL INDUCTOR	MONOLYTHIC METAL STRIP RESISTOR WITH HEAT SINKING WINGS	METHOD FOR MAKING FORMED SURFACE MOUNT RESISTOR	METHOD FOR MAKING OVERLAY SURFACE MOUNT RESISTOR	METHOD FOR MAKING OVERLAY SURFACE MOUNT RESISTOR.	OVERLAY SURFACE MOUNT RESISTOR	METHOD FOR MAKING OVERLAY SURFACE MOUNT RESISTOR	METHOD FOR MAKING A HIGH CURRENT LOW PROFILE INDUCTOR	METHOD FOR MAKING A HIGH CURRENT LOW PROFILE INDUCTOR	METHOD FOR MAKING A HIGH CURRENT LOW PROFILE INDUCTOR.	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	PUBLISHED	PUBLISHED	ISSUED	Status
1/31/2001	12/29/1999	12/21/1999	3/10/2004	2/18/2002	11/17/2000	12/21/1999	8/5/2009	1/14/2008	7/24/2007	File Date
7/1/2003	1/30/2001	1/28/2003	6/7/2005	4/27/2004	8/27/2002	6/11/2002			3/18/2008	Issue Date
Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

UTL	UTL	UTL	UTL	UTL	UTL	Туре
11/123,508	10/744,846	10/441,649	09/811,844	10/079,010	09/829,169	Serial No.
7,042,328	6,925,704	7,102,484	7,038,572	7,170,389	7,214,295	Patent No.
HIGH POWER RESISTOR HAVING AN IMPROVED OPERATING TEMPERATURE RANGE	METHOD FOR MAKING HIGH POWER RESISTOR HAVING IMPROVED OPERATING TEMPERATURE RANGE	HIGH POWER RESISTOR HAVING AN IMPROVED OPERATING TEMPERATURE RANGE AND METHOD OF MAKING SAME	POWER CHIP RESISTOR	APPARATUS FOR TANTALUM PENTOXIDE MOISTURE BARRIER IN FILM RESISTORS	METHOD FOR TANTALUM PENTOXIDE MOISTURE BARRIER IN FILM RESISTORS	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	<u>Status</u>
5/5/2005	12/23/2003	5/20/2003	3/19/2001	2/19/2002	4/9/2001	<u>File Date</u>
5/9/2006	8/9/2005	9/5/2006	5/2/2006	1/30/2007	5/8/2007	<u>Issue Date</u>
Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, I.nc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

UTL	UTL	UTL	UTL	UTL	UTL	UTL	UTL	UTL	Туре
12/536,792	12/205,197	12/114,057	12/026,939	12/134,240	11/862,572	11/535,758	11/380,293	11/066,865	Serial No.
								7,190,252	Patent No.
METAL STRIP RESISTOR FOR MITIGATING EFFECTS OF THERMAL EMF	RESISTOR AND METHOD FOR MAKING SAME	HIGHLY COUPLED INDUCTOR	RESISTOR AND METHOD FOR MAKING SAME	HIGH POWERED INDUCTORS USING A. MAGNETIC BIAS	POWER RESISTOR.	INDUCTOR WITH THERMALLY STABLE RESISTANCE	FLUX CHANNELED, HIGH CURRENT INDUCTOR	SURFACE MOUNT ELECTRICAL RESISTOR WITH THERMALLY CONDUCTIVE, ELECTRICALLY INSULATIVE FILLER AND METHOD FOR USING SAME	<u>Title:</u> (Patent Description)
PUBLISHED	PUBLISHED	PUBLISHED	PUBLISHED	PUBLISHED	PUBLISHED	PUBLISHED	PUBLISHED	ISSUED	Status
8/6/2009	9/5/2008	5/2/2008	2/6/2008	6/6/2008	9/27/2007	9/27/2006	4/26/2006	2/25/2005	File Date
								3/13/2007	Issue Date
Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

			-					
031170/0001	Vishay Dale Electronics, Inc.		5/17/2011	PENDING	METHOD FOR MAKING A HIGH CURRENT LOW PROFILE INDUCTOR		13/109,576	UTL
031170/0001	Vishay Dale Electronics, Inc.		11/30/2012	PENDING	SURFACE MOUNT RESISTOR WITH TERMINALS FOR HIGH POWER DISSIPATION AND METHOD FOR MAKING SAME		13/689,928	UIL
025675/0001	Vishay Dale Electronics, Inc.		12/28/2009	PENDING	SURFACE MOUNT RESISTOR WITH TERMINALS FOR HIGH POWER DISSIPATION AND METHOD FOR MAKING SAME		61/290,429	PRV
025675/0001	Vishay Dale Electronics, Inc.		6/28/2010	PENDING	RESISTOR WITH TEMPERATURE COEFFICIENT OF RESISTANCE (TCR) COMPENSATION		61/359,000	PRV
025675/0001	Vishay Dale Electronics, Inc.		12/30/2009	PENDING	SURFACE MOUNT RESISTOR WITH TERMINALS FOR HIGH POWER DISSIPATION AND METHOD FOR MAKING SAME		12/650,079	UIL
025675/0001	Vishay Dale Electronics, Inc.		9/2/2010	PENDING	RESISTOR WITH TEMPERATURE COEFFICIENT OF RESISTANCE (TCR) COMPENSATION		12/874,514	UTL
Reel/Frame	Domestic Loan Party	Issue Date	File Date	Status	Title: (Patent Description)	Patent No.	Serial No.	Туре

031170/0001	Vishay Dale Electronics, Inc.		1/25/2013	PENDING	INTEGRATED CIRCUIT ELEMENT AND ELECTRONIC CIRCUIT FOR LIGHT EMITTING DIODE APPLICATIONS		13/750,404	UTL
031170/0001	Vishay Dale Electronics, Inc.		12/19/2012	PENDING	METHOD FOR MAKING INDUCTOR COIL STRUCTURE		13/720,618	UTL
031170/0001	Vishay Dale Electronics, Inc.		8/31/2012	PENDING	HIGHLY COUPLED INDUCTOR		13/600,770	UTL
031170/0001	Vishay Dale Electronics, Inc.		8/8/2012	PENDING	RESISTOR AND METHOD FOR MAKING SAME		13/569,721	UTL
031170/0001	Vishay Dale Electronics, Inc.		6/11/2012	PENDING	RESISTOR WITH TEMPERATURE COEFFICIENT OF RESISTANCE (TCR) COMPENSATION		13/493,402	UTL
031170/0001	Vishay Dale Electronics, Inc.		5/1/2012	PENDING	HEAT SPREADER FOR ELECTRICAL COMPONENTS		13/462,958	UTL
031170/0001	Vishay Dale Electronics, Inc.		8/19/2011	PENDING	HIGH POWERED INDUCTORS USING A MAGNETIC BIAS		13/213,877	UTL
031170/0001	Vishay Dale Electronics, Inc.		5/5/2011	PENDING	FOUR-TERMINAL RESISTOR WITH FOUR RESISTORS AND ADJUSTABLE TEMPERATURE COEFFICIENT OF RESISTANCE		13/127,838	UIL
Reel/Frame	Domestic Loan Party	<u>Issue Date</u>	File Date	Status	<u>Title:</u> (Patent Description)	Patent No.	Serial No.	Туре

					STANDED INDICATION			
031170/0001	Vishay Dale Electronics, Inc.	2/19/2013	8/4/2011	ISSUED	INDUCTOR WITH THERMALLY STARI E RESISTANCE	8,378,772	13/198,274	UTL
031170/0001	Vishay Dale Electronics, Inc.	1/1/2013	3/18/2011	ISSUED	RESISTOR AND METHOD FOR MAKING SAME	8,344,843	13/051,585	UTL
031170/0001	Vishay Dale Electronics, Inc.	11/27/2012	11/19/2010	ISSUED	POWER RESISTOR	8,319,598	12,950,177	UTL
031170/0001	Vishay Dale Electronics, Inc.	9/4/2012	4/28/2011	ISSUED	HIGHLY COUPLED INDUCTOR	8,258,907	13/096,715	UTL
031170/0001	Vishay Dale Electronics, Inc.	8/23/2011	6/6/2008	ISSUED	HIGH POWERED INDUCTORS USING A MAGNETIC BIAS	8,004,379	12/134,240	UTL
031170/0001	Vishay Dale Electronics, Inc.		1/14/2013	PENDING	ELECTRONIC MODULE AND METHOD FOR MAKING SAME		61/752,278	PRV
031170/0001	Vishay Dale Electronics, Inc.		1/11/2013	PENDING	WIRELESS SIDE CHARGING		61/751,562	PRV
031170/0001	Vishay Dale Electronics, Inc.		1/26/2012	PENDING	INTEGRATED CIRCUIT ELEMENT AND ELECTRONIC CIRCUIT FOR LIGHT EMITTING DIODE APPLICATIONS		61/591,018	PRV
031170/0001	Vishay Dale Electronics, Inc.		2/15/2013	PENDING	INDUCTOR WITH THERMALLY STABLE RESISTANCE		13/768,039	UTL
031170/0001	Vishay Dale Electronics, Inc.		1/25/2013	PENDING	LOW PROFILE HIGH CURRENT COMPOSITE TRANSFORMER		13/750,762	UTL
Reel/Frame	<u>Domestic Loan Party</u>	Issue Date	File Date	<u>Status</u>	<u>Title:</u> (Patent Description)	Patent No.	Serial No.	Type

7/26/2011 Vishay Dale Electronics, Inc.
4/12/2011
3/18/2008
9/4/2007
5/22/2007
4/25/2006
9/20/2005
9/17/2002
3/6/2001
12/7/1999
3/13/2001
Issue Date

UTL	UTL	UTL	UTL	UTL	UTL	UTL	UTL	PRV	<u>Type</u>
13/768,039	13,689,928	13/720,618	12,950,177	13/569,721	13/600,770	13/462,958	13/493,402	61/591,018	Serial No.
8,975,994			8,319,598	8,686,828		9,001,512	8,525,637		Patent No.
INDUCTOR WITH THERMALLY STABLE RESISTANCE	SURFACE MOUNT RESISTOR WITH TERMINALS FOR HIGH POWER DISSIPATION AND METHOD FOR MAKING SAME	METHOD FOR MAKING INDUCTOR COIL STRUCTURE	POWER RESISTOR	RESISTOR AND METHOD FOR MAKING SAME	HIGHLY COUPLED INDUCTOR	HEAT SPREADER FOR ELECTRICAL COMPONENTS	RESISTOR WITH TEMPERATURE COEFFICIENT OF RESISTANCE (TCR) COMPENSATION	INTEGRATED CIRCUIT ELEMENT AND ELECTRONIC CIRCUIT FOR LIGHT EMITTING DIODE APPLICATIONS	<u>Title:</u> (Patent Description)
ISSUED	PENDING	PENDING	ISSUED	ISSUED	PENDING	ISSUED	ISSUED	PENDING	Status
2/15/2013	11/30/2012	12/19/2012	11/19/2010	8/8/2012	8/31/2012	5/3/2012	6/11/2012	1/26/2012	<u>File Date</u>
3/10/2015			11/27/2012	4/1/2014		4/7/2015	9/3/2013		Issue Date
Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, LLC	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Domestic Loan Party
037261/0616	037261/0616	037261/0616	037261/0616	037261/0616	037261/0616	037261/0616	037261/0616	037261/0616	Reel/Frame

037261/0616	Dale Electronics, Inc.		5/16/2014	PENDING	RESISTOR AND METHOD FOR MAKING SAME		14/280,230	UTL
037261/0616	Dale Electronics, Inc.		4/2/2014	PENDING	MAGNETIC COMPONENTS AND METHODS FOR MAKING SAME		14/242,982	UTL
037261/0616	Dale Electronics, Inc.	5/20/2014	12/28/2012	ISSUED	RESISTOR AND METHOD FOR MAKING SAME	8,730,003	13/730,155	UTL
037261/0616	Vishay-Dale		3/10/2014	PENDING	RESISTOR AND METHOD OF MANUFACTURE		14/203,234	UTL
037261/0616	Dale Electronics, Inc.		3/28/2014	PENDING	RESISTOR AND METHOD FOR MAKING SAME		14/228,780	UTL
037261/0616	Vishay Dale Electronics, Inc.	11/4/2014	8/30/2013	ISSUED	RESISTOR WITH TEMPERATURE COEFFICIENT OF RESISTANCE (TCR) COMPENSATION	8,878,643	14/015,488	UTL
037261/0616	Vishay Dale Electronics, Inc.		1/14/2013	PENDING	ELECTRONIC MODULE AND METHOD FOR MAKING SAME		61/752,278	PRV
037261/0616	Vishay Dale Electronics, Inc.		1/25/2013	PENDING	LOW PROFILE HIGH CURRENT COMPOSITE TRANSFORMER		13/750,762	UTL
037261/0616	Vishay Dale Electronics, Inc.		1/25/2013	PENDING	INTEGRATED CIRCUIT ELEMENT AND ELECTRONIC CIRCUIT FOR LIGHT EMITTING DIODE APPLICATIONS		13/750,404	UTL
Reel/Frame	Domestic Loan Party	Issue Date	File Date	Status	<u>Title:</u> (Patent Description)	Patent No.	Serial No.	Type

	Т		Ι				
Prov	UTL	UTL	UTL	UTL	Design	UTL	<u>Type</u>
62/202,580	14/563,560	14/531,505	14/473,118	13/725,018	29/491,946	14/287,883	Serial No.
				8,823,483			Patent No.
MOLDED PASSIVE COMPONENT FOR HIGH VOLTAGE APPLICATIONS	THERMALLY SPRAYED THIN FILM RESISTOR AND METHOD OF MAKING	RESISTOR WITH TEMPERATURE COEFFICIENT OF RESISTANCE (TCR) COMPENSATION	POWER RESISTOR WITH INTEGRATED HEAT SPREADER	POWER RESISTOR WITH INTEGRATED HEAT SPREADER	EDGE-WOUND RESISTOR	EDGE-WOUND RESISTOR, RESISTOR ASSEMBLY, AND METHOD OF MAKING SAME	<u>Title:</u> (Patent Description)
PENDING	PENDING	PENDING	PENDING	ISSUED	PENDING	PENDING	Status
8/7/2015	12/8/2014	11/3/2014	8/29/2014	12/21/2012	5/27/2014	5/27/2014	<u>File Date</u>
				9/2/2014			Issue Date
Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Vishay Dale Electronics, Inc.	Dale Electronics, Inc.	Dale Electronics, Inc.	Dale Electronics, Inc.	Dale Electronics, Inc.	Domestic Loan Party
037261/0616	037261/0616	037261/0616	037261/0616	037261/0616	037261/0616	037261/0616	Reel/Frame

# (b) <u>U.S. Trademarks and Trademark Applications</u>

\* Some of the trademarks listed below have been filed with the USPTO under Dale Electronics, Inc. or Vishay Dale Electronics, Inc. March 26, 2015. Dale Electronics, Inc. changed its name to Vishay Dale Electronics, Inc. on June 4, 1997 and to Vishay Dale Electronics, LLC on

WSR	WSL	POWER METAL STRIP	IHLP	DALE	WSR	WSL	POWER METAL STRIP	IHLP	DALE	Trademark
Vishay Dale Electronics, Inc.	Legal Owner									
United States	Country									
3264991	3431324	2074628	3394307	1383220	3264991	3431324	2074628	3394307	1383220	Reg.#
7/17/2007	5/20/2008	6/24/1997	3/11/2008	2/18/1986	7/17/2007	5/20/2008	6/24/1997	3/11/2008	2/18/1986	Reg. Date
5686/0277	5686/0277	5686/0277	5686/0277	5686/0277	004453/0500	004453/0500	004453/0500	004453/0500	004453/0500	Reel/Frame

# Patents and Trademarks of Vishay Intertechnology, Inc.

## U.S. Patent Registrations and Patent Applications

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	UTL	UTI	UTI	UTL	UTL	UTE	UTL	Type
10/233,184	10/002,868	09/820,064	09/810,206	10/964,357	10/079,085	09/765,901	09/568,937	Serial No.
6,727,798	6,873,028	6,669,435	6,880,234	7,247,250	6,671,945	6,680,668	RE39,660	Patent No.
FLIP CHIP RESISTOR AND ITS MANUFACTURING	SURGE CURRENT CHIP RESISTOR	PRECISION RESISTOR TUBE FEEDER	METHOD FOR THIN FILM NTC THERMISTOR	METHOD FOR MANUFACTURING A FAST HEAT RISE RESISTOR	METHOD FOR MAKING A RESISTOR USING RESISTIVE FOIL	METHOD AND APPARATUS FOR FAST HEAT RISE RESISTOR USING RESISTIVE FOIL WITH FOIL WITH PHOTOLITHOGRAP HIC PRODUCTION	SURFACE MOUNTED FOUR TERMINAL RESISTOR	Title: (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
9/3/2002	11/15/200	3/28/2001	3/16/2001	10/13/2004	2/20/2002	1/19/2001	5/11/2000	File Date
4/27/2004	3/29/2005	12/30/2003	4/19/2005	7/24/2007	1/6/2004	1/20/2004	5/29/2007	Issue Date
Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

HIGH-FREQUENCY HIGH-	UTL 10/208,121 6,621,142 FREQUENCY CAPACITOR ISSUED SEMICONDUCTOR SUBSTRATE	UTL 09/661,483 6,538,300 FORMED ON SEMICONDUCTOR SUBSTRATE	UTL 11/050,077 7,394,845 METHOD FOR ISSUED SPREADING CODES	UTL 10/967,883 7,278,201 MANUFACTURING ISSUED A RESISTOR	UTL10/762,6097,154,370HIGH PRECISION POWER RESISTORSISSUED	UTL 10/304,261 6,892,443 MANUFACTURING ISSUED A RESISTOR	10/440,941	Type Serial No. Patent No. (Patent Description) Status
	D 7/29/2002 9/16/2003	D 9/14/2000 3/25/2003	D 2/3/2005 7/1/2008	D 10/18/2004 10/9/2007	D 1/22/2004 12/26/2006	D 11/25/2002 5/17/2005	5/19/2003	S File Date Issue Date
	Vishay Intertechnology Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.		6 Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	e Domestic Loan Party
	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

UTL	UTL	UTL	UTL	UTL	Туре
11/415,039	10/157,584	09/844,934	09/395,094	09/395,095	Serial No.
7,426,102	6,876,061	6,562,647	6,316,287	6,271,060	Patent No.
HIGH PRECISION CAPACITOR WITH STANDOFF	CHIP SCALE SURFACE MOUNT PACKAGE FOR SEMICONDUCTOR DEVICE AND PROCESS OF FABRICATING THE SAME	CHIP SCALE SURFACE MOUNT PACKAGE FOR SEMICONDUCTOR DEVICE AND PROCESS OF FABRICATING THE SAME	CHIP SCALE SURFACE MOUNT PACKAGES FOR SEMICONDUCTOR DEVICE AND PROCESS OF FABRICATING THE SAME	PROCESS OF FABRICATING A CHIP SCALE SURFACE MOUNT PACKAGE FOR. SEMICONDUCTOR DEVICE	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
5/1/2006	5/28/2002	4/26/2001	9/13/1999	9/13/1999	File Date
9/16/2008	4/5/2005	5/13/2003	11/13/2001	8/7/2001	Issue Date
Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

PRECISION HIGH- FREQUENCY CAPACITOR FORMED ON SEMICONDUCTOR	12/28/2007		Vishay Intertechnology, Inc.
PRECISION HIGH- FREQUENCY CAPACITOR FORMED ON SEMICONDUCTOR SUBSTRATE	Ľ	11/16/2006	1/16/2006
PRECISION HIGH- FREQUENCY CAPACITOR FORMED ON SEMICONDUCTOR SUBSTRATE		6/5/2003	6/5/2003 12/19/2006
CHIP SCALE SURFACE MOUNT PACKAGE FOR SEMICONDUCTOR DEVICE AND PROCESS OF FABRICATING THE SAME		4/10/2007	4/10/2007 9/15/2009
CHIP SCALE SURFACE MOUNT PACKAGE FOR SEMICONDUCTOR DEVICE AND PROCESS OF FABRICATING THE SAME		3/15/2005	
Title: (Patent Description) Status		File Date	File Date Issue Date

UTL	UTL	UTL	Type
13/075,752	11/759,523	13/592,091	Serial No.
8,324,711	7,907,090		Patent No.
PRECISION HIGH FREQUENCY CAPACITOR FORMED ON SEMICONDUCTOR SUBSTRATE	CERAMIC DIELECTRIC FORMULATION FOR BROAD BAND UHF ANTENNA	PRECISION HIGH- FREQUENCY CAPACITOR FORMED ON SEMICONDUCTOR SUBSTRATE	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	PENDING	Status
3/30/2011	6/7/2007	12/3/2012	File Date
12/4/2012	3/15/2011		Issue Date
Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Domestic Loan Party
031170/0001	031170/0001	031170/0001	Reel/Frame

VISHAY (In Middle of Pyramid) VISHAY (In Middle of Pyramid)	VISHAY (In Middle Pyramid)		VISHAY	VISHAY	VISHAY	VISHAY	QUICK NET	FUNCTIONPAK	Trademark	(b) <u>U.S. Trademar</u>	UTL 13/075,752		UTL 11/759,523			UTL 13/592,091	
VISHAY (Triangle & Circle   Vi			Vi	Vi	Vi	Vi	Vi	Vi		ks and Tradem	8,324,711		7,907,090				
Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Vishay Intertechnology, Inc.	Legal Owner	U.S. Trademarks and Trademark Applications	CAPACITOR FORMED ON SEMICONDUCTOR SUBSTRATE	PRECISION HIGH FREQUENCY	DIELECTRIC FORMULATION FOR BROAD BAND UHF ANTENNA	CERAMIC	SEMICONDUCTOR SUBSTRATE	FORMED ON	PRECISION HIGH-
United States	United States	United States	United States	United States	United States	United States	United States	United States	Country		ISSUED		ISSUED			PENDING	
ates	ates	ates	ates	ates	ates	ates	ates	ates	Y		3/30/2011		6/7/2007			12/3/2012	
1687033	3530559	1692580	3530560	837476	1015163	1790212	1979712	2602606	Reg.#		12/4/2012		3/15/2011				
5/12/1992	11/11/2008	6/9/1992	11/11/2008	10/24/1967	7/8/1975	8/31/1993	6/11/1996	7/30/2002	Reg. Date		Vishay Intertechnology, Inc.		Vishay Intertechnology, Inc.			Vishay Intertechnology, Inc.	
004453/0500	004453/0500	004453/0500	004453/0500	004453/0500	004453/0500	004453/0500	004453/0500	004453/0500	Reel/Frame		031170/0001		031170/0001			031170/0001	

Trademark	<u>Legal Owner</u>	Country	Reg.#	Reg. Date	<u>Reel/Frame</u>
TMBS	Vishay Intertechnology, Inc.	United States	3256028	6/26/2007	004453/0500
VISHAY PRECISION	Vichou Intertochnology Inc	I Inited States	77/052 205	0106/8/2	004452/0500
GROUP b&w logo	vishay intertechnology, inc.	Officer States	111733,373	3/6/2010	00##JJ/0J00
VISHAY PRECISION	Victor Intertechnology Inc	I Inited Ctates	200 CS0/LL	0100/0/E P 1:3	00115210500
GROUP color logo	vishay intertechnology, inc.	Officer States	111732,773	1'1160 3/6/2010	00##33/0300

### Patents and Trademarks of Siliconix incorporated

## U.S. Patent Registrations and Patent Applications

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UTL	UTL	UTL	UTL	UTL	UTL	Type
08/067,373	08/289,358	08/031,798	08/236,299	07/949,288	08/047,723	Serial No.
5,517,379	5,474,943	5,341,011	5,439,842	5,328,866	5,410,170	Patent No.
REVERSE BATTERY PROTECTION DEVICE ISSUED CONTAINING POWER MOSFET	METHOD FOR FABRICATING A SHORT CHANNEL TRENCHED DMOS TRANSISTOR	SHORT CHANNEL TRENCHED DMOS TRANSISTOR	LOW TEMPERATURE OXIDE LAYER OVER ISSUED FIELD IMPLANT MASK	LOW TEMPERATURE OXIDE LAYER OVER FIELD IMPLANT FIELD IMPLANT MASK	DMOS POWER TRANSISTORS WITH REDUCED NUMBER OF CONTACTS USING INTEGRATED BODY-SOURCE CONNECTIONS	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
5/26/1993	8/11/1994	3/15/1993	5/2/1994	9/21/1992	4/14/1993	File Date
5/14/1996	12/12/1995	8/23/1994	8/8/1995	7/12/1994	4/25/1995	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	<u>Domestic Loan Party</u>
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	<u>Reel/Frame</u>

UTL	UTL	UTL	UTL	UTL	UTL	Туре
08/367,486	08/062,969	08/062,503	08/062,968	08/062,504	08/067,372	Serial No.
5,665,996	5,459,654	5,508,874	5,455,496	5,377,094	5,414,292	Patent No.
VERTICAL POWER MOSFET HAVING THICK METAL LAYER TO REDUCE DISTRIBUTED RESISTANCE	APPARATUS FOR GENERATING POSITIVE AND NEGATIVE SUPPLY RAILS FROM OPERATING MOTOR CONTROL CIRCUIT	DISCONNECT SWITCH CIRCUIT TO POWER HEAD RETRACT IN HARD DISK DRIVE MEMORIES	HEAD-RETRACT CIRCUIT FOR MOVING MEDIA STORAGE APPARATUS	PUSH-PULL OUTPUT STAGE FOR DRIVING MOTORS WHICH GENERATES AUXILIARY VOLTAGE SUPPLY	A JUNCTION- ISOLATED FLOATING DIODE	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
12/30/1994	5/14/1993	5/14/1993	5/14/1993	5/14/1993	5/26/1993	File Date
9/9/1997	10/17/1995	4/16/1996	10/3/1995	12/27/1994	5/9/1995	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

1/1995
3/8/1999 12/12/2000
8/6/1997 8/31/1999
12/30/1994 6/16/1998
11/10/1997 3/28/2000
1/6/1997 5/23/2000
File Date Issue Date

UTL	UTL	UTL	UTL	UTL	UTL	UTL	Type
08/062,370	07/854,162	08/362,674	08/180,265	07/881,589	08/040,684	08/318,027	<u>Serial No.</u>
5,465,000	5,248,627	5,521,409	5,429,964	5,304,831	5,374,843	5,514,608	Patent No.
THRESHOLD ADJUSTMENT IN VERTICAL DMOS DEVICES	THRESHOLD ADJUSTMENT IN FABRICATING VERTICAL DMOS DEVICES	STRUCTURE AND FABRICATION OF POWER MOSFETS INCLUDING TERMINATION STRUCTURES	LOW ON- RESISTANCE POWER MOS TECHNOLOGY	LOW ON- RESISTANCE POWER MOS TECHNOLOGY	LIGHTLY-DOPED DRAIN MOSFET WITH IMPROVED BREAKDOWN CHARACTERISTICS	LIGHTLY-DOPED DRAIN MOSFET WITH IMPROVED BREAKDOWN CHARACTERISTICS	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
5/14/1993	3/20/1992	12/22/1994	1/12/1994	5/12/1992	3/31/1993	10/4/1994	File Date
11/7/1995	9/28/1993	5/28/1996	7/4/1995	4/19/1994	12/20/1994	5/7/1996	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

025675/0001	Siliconix incorporated	7/30/1996	6/5/1995	ISSUED	METHOD FOR FORMING A BIPOLAR TRANSISTOR HAVING SELECTED BREAKDOWN VOLTAGE	5,541,123	08/463,647	UTL
025675/0001	Siliconix incorporated	8/20/1996	6/5/1995	ISSUED	METHOD FOR FORMING A ZENER FORMING A ZENER DIODE REGION AND AN ISOLATION REGION	5,547,880	08/464,978	UTL
025675/0001	Siliconix incorporated	12/10/1996	6/5/1995	ISSUED	PMOS TRANSISTORS WITH DIFFERENT BREAKDOWN VOLTAGES FORMED IN THE SAME SUBSTRATE	5,583,061	08/464,435	UTL
025675/0001	Siliconix incorporated	9/24/1996	10/17/1994	ISSUED	BICDMOS PROCESS, TECHNOLOGY	5,559,044	08/323,950	UTL
025675/0001	Siliconix incorporated	6/20/1995	4/11/1994	ISSUED	BICDMOS STRUCTURES	5,426,328	08/226,419	UTL
025675/0001	Siliconix incorporated	6/20/1995	8/4/1993	ISSUED	METAL CROSSOVER IN HIGH VOLTAGE IC WITH GRADUATED DOPING CONTROL	5,426,325	08/101,886	UTL
025675/0001	Siliconix incorporated	3/22/1994	3/20/1992	ISSUED	DRIVER CIRCUIT FOR SINKING CURRENT TO TWO SUPPLY VOLTAGES	5,296,765	07/855,377	UTL
025675/0001	Siliconix incorporated	3/10/1998	6/6/1995	ISSUED	THRESHOLD ADJUSTMENT IN FIELD EFFECT SEMICONDUCTOR DEVICES	5,726,477	08/482,341	UTL
Reel/Frame	<u>Domestic Loan Party</u>	Issue Date	File Date	Status	<u>Title:</u> (Patent Description)	Patent No.	Serial No.	Type

UTL	UTL	UTL	UTL	UTL	UTL	Туре
08/026,930	08/705,910	08/026,932	08/667,219	08/647,073	08/463,165	Serial No.
5,422,508	5,751,054	5,374,569	5,643,820	5,648,281	5,541,125	Patent No.
BICDMOS STRUCTURE	ZENER DIODES ON SAME WAFER WITH BICDMOS STRUCTURES	METHOD FOR FORMING A BICDMOS	METHOD FOR FABRICATING AND MOS CAPACITOR USING ZENER DIODE REGION	METHOD FOR FORMING AN ISOLATION STRUCTURE AND A ISSUED BIPOLAR TRANSISTOR ON A SEMICONDUCTOR SUBSTRATE	METHOD FOR FORMING A LATERAL MOS TRANSISTOR HAVING LIGHTLY DOPED DRAIN FORMED ALONG WITH OTHER TRANSISTORS IN THE SAME SUBSTRATE	Title: (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	<u>Status</u>
3/5/1993	8/29/1996	3/5/1993	6/19/1996	5/8/1996	6/5/1995	File Date
6/6/1995	5/12/1998	12/20/1994	7/1/1997	7/15/1997	7/30/1996	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

UTL	UTL	UTL	UTL	UTL	Type
08/447,484	08/386,895	07/918,954	08/131,114	08/463,417	e Serial No.
5,532,179	5,558,313	5,910,669	5,479,037	7 5,618,743	Patent No.
METHOD OF MAKING A FIELD EFFECT TRENCH TRANSISTOR HAVING LIGHTLY DOPED EPITAXIAL REGION ON THE SURFACE PORTION THEREOF	TRENCH FIELD EFFECT TRANSISTOR WITH REDUCED PUNCH- THROUGH SUSCEPTIBILITY AND LOW RDSON	FIELD EFFECT TRENCH TRANSISTOR HAVING LIGHTLY DOPED EPITAXIAL REGION ON THE SURFACE PORTION THEREOF	LOW THRESHOLD VOLTAGE EPITAXIAL DMOS TECHNOLOGY	MOS TRANSISTOR HAVING ADJUSTED THRESHOLD VOLTAGE FORMED ALONG WITH OTHER TRANSISTORS	Title: (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
5/23/1995	2/10/1995	7/24/1992	10/1/1993	6/5/1995	File Date
7/2/1996	9/24/1996	6/8/1999	12/26/1995	4/8/1997	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

11/30/1993 4/23/1996
5/2/1995
2/25/1997
7/4/1995
8/29/1995
7/4/1995
11/9/1999
<u>Issue Date</u>

ed	Siliconix incorporated	8/13/1996	10/19/1994	ISSUED	ELECTROSTATIC DISCHARGE PROTECTION DEVICE FOR INTEGRATED CIRCUIT	5,545,909	08/326,172	UTL
	Siliconix incorporated	9/19/1995	10/5/1994	ISSUED	A BIDIRECTIONAL BLOCKING LATERAL MOSFET WITH IMPROVED ON-RESISTANCE	5,451,533	08/318,323	UTL
_	Siliconix incorporated	5/30/1995	11/30/1993	ISSUED	A BIDIRECTIONAL BLOCKING LATERAL MOSFET WITH IMPROVED ON-RESISTANCE	5,420,451	08/160,539	UTL
	Siliconix incorporated	6/1/1999	8/5/1997	ISSUED	METHOD AND APPARATUS FOR PROVIDING GATE DRIVE VOLTAGE TO SWITCHING DEVICE	5,909,139	08/907,216	UTL
<u></u>	Siliconix incorporated	3/24/1998	4/22/1996	ISSUED	GATE DRIVE TECHNIQUE FOR A BIDIRECTIONAL BLOCKING LATERAL MOSFET	5,731,732	08/636,258	UTL
_	Siliconix incorporated	3/18/1997	12/8/1995	ISSUED	BIDERECTIONAL BLOCKING LATERAL MOSFET WITH IMPROVED ON-RESISTANCE	5,612,566	08/569,334	UTL
	Domestic Loan Party	<u>Issue Date</u>	<u>File Date</u>	Status	<u>Title:</u> (Patent Description)	Patent No.	Serial No.	Type

UTL 08/	UTL 08/	UTL 08/	UTL 08/	UTL 08/	UTL 08/	Type Se
08/253,527	08/268,755	08/295,271	08/873,781	08/486,280	08/472,943	Serial No.
5,468,982	5,486,772	5,528,483	5,877,534	5,654,574	5,677,205	Patent No.
TRENCHED DMOS TRANSISTOR WITH CHANNEL BLOCK AT CELL TRENCH CORNERS	RELIABILITY TEST METHOD FOR SEMICONDUCTOR TRENCH DEVICES	VOLTAGE CONVERTER WITH SHIFT PROTECTION AGAINST OVERLOAD CURRENT	METHOD OF FORMING ELECTROSTATIC DISCHARGE PROTECTION DEVICE FOR INTEGRATED CIRCUIT	ELECTROSTATIC DISCHARGE PROTECTION DEVICE FOR INTEGRATED CIRCUIT	METHOD FOR FORMING ELECTROSTATIC DISCHARGE PROTECTION DEVICE FOR INTEGRATED CIRCUIT	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
6/3/1994	6/30/1994	8/23/1994	6/12/1997	6/6/1995	6/6/1995	<u>File Date</u>
11/21/1995	1/23/1996	6/18/1996	3/2/1999	8/5/1997	10/14/1997	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

UTL	UTL	UTL	UTL	UTL	UTL	UTL	<u>Type</u>
08/326,408	08/325,860	08/367,515	08/632,052	08/423,588	08/701,035	08/429,414	Serial No.
5,559,424	5,585,991	5,689,209	5,614,751	5,597,765	5,895,952	5,674,766	Patent No.
VOLTAGE REGULATOR HAVING IMPROVED STABILITY	PROTECTIVE CIRCUIT FOR PROTECTING LOAD AGAINST EXCESSIVE INPUT VOLTAGE	LOW-SIDE BIDIRECTIONAL BATTERY DISCONNECT SWITCH	EDGE TERMINATION STRUCTURE FOR POWER MOSFET	METHOD FOR MAKING TERMINATION STRUCTURE FOR POWER MOSFET	TRENCH MOSFET WITH MULTI- RESISTIVITY DRAIN TO PROVIDE LOW ON-RESISTANCE	METHOD OF MAKING A TRENCH MOSFET WITH MULTI-RESISTIVITY DRAIN TO PROVIDE LOW ON- RESISTANCE BY VARYING DOPANT	Title: (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
10/20/1994	10/19/1994	12/30/1994	4/15/1996	4/17/1995	8/21/1996	4/26/1995	File Date
9/24/1996	12/17/1996	11/18/1997	3/25/1997	1/28/1997	4/20/1999	10/7/1997	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	<u>Domestic Loan Party</u>
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

Type	Serial No.	Patent No.	<u>Title:</u> (Patent Description)	Status	File Date	Issue Date	Domestic Loan Party	Reel/Frame
UTL	08/388,535	5,596,265	BAND GAP VOLTAGE	ISSUED	2/14/1995	1/21/1997	Siliconix incorporated	025675/0001
OIL	08/388,333	3,390,203	COMPENSATION CIRCUIT	ISSUED	2/14/1993	1/21/1997	Sincomx incorporated	1079070
			OUTPUT CONTROL					
UTL	08/389,705	5,506,496	CIRCUIT FOR A VOLTAGE	ISSUED	2/14/1995	4/9/1996	Siliconix incorporated	025675/0001
			REGULATOR					
			HIGH DENSITY					
UTL	08/533,814	5,689,128	TRENCHED DMOS TRANSISTOR	ISSUED	8/21/1995	11/18/1997	Siliconix incorporated	025675/0001
			PUNCH-THROUGH					
UTL	08/415,009	5,592,005	FIELD EFFECT TRANSISTOR	ISSUED	3/31/1995	1/7/1997	Siliconix incorporated	025675/0001
			METHOD OF					
			MAKING PUNCH-					
UTL	08/962,885	6,069,043	THROUGH HELD EFFECT	ISSUED	11/21/1997	5/30/2000	Siliconix incorporated	0256/5/0001
			TRANSISTOR					
			VOLTAGE-					
UTL	08/459,054	5,856,692	ACCUMULATION-	ISSUED	6/2/1995	1/5/1999	Siliconix incorporated	025675/0001
			MODE MOSFET					
			BIDIRECTIONAL					
			TRENCH GATED					
			POWER MOSFET					
UTL	08/884,826	5,877,538	BODY BUS	ISSUED	6/30/1997	3/2/1999	Siliconix incorporated	025675/0001
			EXTENDING					
			UNDERNEATH GATE TRENCH					

UTL	UTL	TTU	UTL	UTL	UIL	Type
08/962,867	08/919,523	08/846,688	08/537,157	08/610,563	09/186,216	Serial No.
6,140,678	5,998,837	5,998,836	5,629,543	5,821,583	6,096,608	Patent No.
TRENCH-GATED POWER MOSFET WITH PROTECTIVE DIODE	TRENCH-GATED POWER MOSFET WITH PROTECTIVE DIODE HAVING ADJUSTABLE BREAKDOWN VOLTAGE	TRENCH-GATED POWER MOSFET WITH PROTECTIVE DIODE	TRENCHED DMOS TRANSISTOR WITH BURIED LAYER FOR REDUCED ON- RESISTANCE AND RUGGEDNESS	TRENCHED DMOS TRANSISTOR WITH LIGHTLY DOPED TUB	BIDIRECTIONAL TRENCH GATED POWER MOSFET WITH SUBMERGED BODY BUS EXTENDING UNDERNEATH GATE TRENCH	Title: (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	<u>Status</u>
11/3/1997	8/28/1997	4/30/1997	8/21/1995	3/6/1996	11/3/1998	File Date
10/31/2000	12/7/1999	12/7/1999	5/13/1997	10/13/1998	8/1/2000	<u>Issue Date</u>
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	<u>Reel/Frame</u>

9/21/1999 Siliconix incorporated
2/2/1996 4/7/1998
2/2/1996 6/16/1998
11/4/1997 7/27/1999
5/15/1996 10/6/1998
6/2/1995 8/26/1997
8/28/1997 4/11/2000
File Date Issue Date

UTL	UTL	UTL	UTL	UTL	UTL	UTL	<u>Type</u>
08/616,393	08/570,876	08/828,474	08/542,611	09/041,368	08/538,105	08/946,613	Serial No.
-			·				
5,814,858	5,939,752	5,973,367	5,616,945	6,087,862	5,726,594	6,046,470	Patent No.
VERTICAL POWER MOSFET HAVING REDUCED SENSITIVITY TO VARIATIONS IN THICKNESS OF EPITAXIAL LAYER	LOW VOLTAGE MOSFET WITH LOW ON-RESISTANCE AND HIGH BREAKDOWN VOLTAGE	MULTIPLE GATED MOSFET FOR USE IN DC-DC CONVERTER	MULTIPLE GATED MOSFET FOR USE IN DC-DC CONVERTER	POWER MOSFET INTERNAL POWER SUPPLY CIRCUITRY	SWITCHING DEVICE INCLUDING POWER MOSFET WITH INTERNAL POWER SUPPLY CIRCUIT	TRENCH-GATED MOSFET WITH INTEGRAL TEMPERATURE DETECTION DIODE	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
3/15/1996	12/12/1995	3/31/1997	10/13/1995	3/11/1998	10/2/1995	10/7/1997	File Date
9/29/1998	8/17/1999	10/26/1999	4/1/1997	7/11/2000	3/10/1998	4/4/2000	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

UTL	UTL	UTL	UTL	UTL	UTL	<u>Type</u>
08/649,747	08/937,941	08/956,257 08/767,708 08/651,232 08/648,266			Serial No.	
5,689,144	5,929,690	5,744,994	5,998,834	6,090,716	6,031,702	
FOUR-TERMINAL POWER MOSFET SWITCH HAVING REDUCED THRESHOLD VOLTAGE AND ON- RESISTANCE	THREE-TERMINAL POWER MOSFET SWITCH FOR USE AS SYNCHRONOUS RECTIFIER OR VOLTAGE CLAMP	THREE-TERMINAL POWER MOSFET SWITCH FOR USE AS SYNCHRONOUS RECTIFIER OR VOLTAGE CLAMP	LONG-CHANNEL TRENCH-GATED POWER MOSFET: HAVING FULLY DEPLETED BODY REGION	METHOD OF FABRICATING A FIELD EFFECT TRANSISTOR	SHORT CIRCUIT PROTECTED DC-DC CONVERTER USING DISCONNECT SWITCHING AND METHOD OF PROTECTING LOAD AGAINST SHORT CIRCUITS	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
5/15/1996	9/25/1997		5/22/1996	12/17/1996	10/22/1997	<u>File Date</u>
11/18/1997	7/27/1999		12/7/1999	7/18/2000	2/29/2000	Issue Date
Siliconix incorporated	Siliconix incorporated			Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

UTL	UTL	UTL	UTL	UTL	UTL	Type
08/646,593	08/742,326	08/556,369	08/895,497	08/482,357	08/701,114	Serial No.
5,904,525	5,917,216	6,066,890	6,008,520	5,688,725	5,808,453	Patent No.
FABRICATION OF HIGH-DENSITY TRENCH DMOS USING SIDEWALL SPACERS	TRENCHED FIELD  EFFECT TRANSISTOR EFFECT TRANSISTOR WITHIN DEPLETION BARRIER	SEPARATE CIRCUIT DEVICES IN AN INTRA-PACKAGE CONFIGURATION AND ASSEMBLY TECHNIQUES	TRENCH MOSFET WITH HEAVILY DOPED DELTA LAYER TO PROVIDE LOW ON- RESISTANCE	METHOD OF MAKING A TRENCH MOSFET WITH DOPE HEAVILY D DELTA LAYER TO PROVIDE LOW ON- RESISTANCE	SYNCHRONOUS CURRENT SHARING PULSE WIDTH MODULATOR	<u>Title:</u> (Patent Description)
ISSUED		ISSUED	ISSUED	ISSUED	ISSUED	Status
5/8/1996	10/31/1996	11/13/1995	7/16/1997	6/6/1995	8/21/1996	File Date
5/18/1999	6/29/1999	5/23/2000	12/28/1999	11/18/1997	9/15/1998	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

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UTL	UTL	UTL	UTL	UTL	UTL	UTL	Туре
08/046,058	07/904,402	09/071,729	09/002,179	08/922,672	08/899,001	08/832,012	<u>Serial No.</u>
5,306,656	6,072,216 5,485,027		6,060,752	5,923,979	5,909,103	6,078,090	Patent No.
METHOD FOR REDUCING ON RESISTANCE AND IMPROVING CURRENT CHARACTERISTICS OF A MOSFET	COMPLIMENTARY ISOLATED DMOS IC TECHNOLOGY	VERTICAL DMOS FIELD EFFECT TRANSISTOR WITH CONFORMAL BURIED LAYER FOR REDUCED ON- RESISTANCE	ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT	PLANAR DMOS TRANSISTOR FABRICATED BY A THREE MASK PROCESS	SAFETY SWITCH FOR LITHIUM ION BATTERY	TRENCH-GATED SCHOTTKY DIODE WITH INTEGRAL CLAMPING DIODE	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
4/12/1993	5/1/1998		12/31/1997	9/3/1997	7/24/1997	4/2/1997	File Date
4/26/1991	1/16/1996	6/6/2000	5/9/2000	7/13/1999	6/1/1999	6/20/2000	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

UTL	UTL	UTL	UTL	UTL	UTL	Type
08/067,365	09/306,003	07/978,201	07/910,864	07/762,103	09/200,197	Serial No.
5,539,610	6,172,383	5,576,245	5,298,781	5,298,442	6,084,264	Patent No.
FLOATING DRIVE TECHNIQUE FOR REVERSE BATTERY PROTECTION	POWER MOSFET HAVING VOLTAGE- CLAMPED GATE	METHOD OF MAKING A VERTICAL CURRENT FLOW FIELD EFFECT TRANSISTOR	VERTICAL CURRENT FLOW FIELD EFFECT TRANSISTOR WITH THICK INSULATOR OVER NON- CHANNEL AREAS	TRENCH DMOS POWER TRANSISTOR WITH FIELD-SHAPING BODY PROFILE AND THREE- DIMENSIONAL GEOMETRY	TRENCH MOSFET HAVING IMPROVED BREAKDOWN AND ON-RESISTANCE CHARACTERISTICS	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
5/26/1993	5/5/1999	11/18/1992	7/8/1992	9/18/1991	11/25/1998	File Date
7/23/1996	1/9/2001	11/19/1996	3/29/1994	3/29/1994	7/4/2000	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	<u>Domestic Loan Party</u>
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	<u>Reel/Frame</u>

UTL	UTL	UTL	UTL	UTL	Туре
09/006,774	08/636,367	08/541,345	08/634,957	08/603,512	Serial No.
6,087,740	5,747,891	5,682,050	5,767,578	5,757,081	Patent No.
PORTABLE COMPUTER CONTAINING BIDIRECTIONAL CURRENT BLOCKING MOSFET FOR BATTERY DISCONNECT SWITCHING	METHOD OF BLOCKING BIDIRECTIONAL FLOW OF CURRENT	BIDIRECTIONAL CURRENT BLOCKING MOSFET FOR BATTERY DISCONNECT SWITCHING INCLUDING PROTECTION AGAINST REVERSE CONNECTED BATTERY CHARGER	SURFACE MOUNT AND FLIP CHIP TECHNOLOGY WITH DIAMOND FILM PASSIVATION FOR TOTAL INTEGRATED CIRCUIT ISOLATION	SURFACE MOUNT AND FLIP CHIP TECHNOLOGY FOR TOTAL INTEGRATED CIRCUIT ISOLATION	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
1/14/1998	4/23/1996	10/10/1995	4/19/1996	2/20/1996	File Date
7/11/2000	5/5/1998	10/28/1997	6/16/1998	5/26/1998	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	<u>Domestic Loan Party</u>
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	<u>Reel/Frame</u>

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			TRENCHED DMOS					
ITTI.	07/928-909	5.316.959	TRANSISTOR	ISSUED	8/12/1992	5/31/1994	Siliconix incorporated	025675/0001
(	0110110,000	0,010,00	FABRICATION USING SIX MASKS	10000110	OI XEI XXXX	010111001	STIROUMA THEOT POT MORE	o ho or or o o o r
			TRENCHED DMOS					
			TRANSISTOR					
UTL	08/603,047	5,639,676	FABRICATION HAVING THICK	ISSUED	2/16/1996	6/17/1997	Siliconix incorporated	025675/0001
			TERMINATION					
			REGION OXIDE					
			TRENCHED DMOS					
			TRANSISTOR					
UTL	08/625,639	5,578,851	HAVING THICK FIELD OXIDE IN	ISSUED	3/29/1996	11/26/1996	Siliconix incorporated	025675/0001
			TERMINATION					
			REGION					
UTL	08/480,469	5,621,604	PWM MULTIPLEXED SOLENOID DRIVER	ISSUED	6/7/1995	4/15/1997	Siliconix incorporated	025675/0001
			METHOD OF					
			FORMING A					
			LATERAL FIELD					
UTL	08/479,308	5,750,416	EFFECT TRANSISTOR	ISSUED	6/7/1995	5/12/1998	Siliconix incorporated	025675/0001
			HAVING REDUCED					
			DRAIN-TO-SOURCE					
			ON-RESISTANCE					
			SUPER TRENCH					
			MOSFET					
UTL	11/698,519	7,557,409	INCLUDING BURIED	ISSUED	1/26/2007	7/7/2009	Siliconix incorporated	025675/0001
			SOURCE					
			ELECTRODE					

UTL	UTL	UTL	UTL	UTL	Туре
10/454,031	11/158,382	10/996,148	11/335,747	10/872,931	Serial No.
7,291,884	7,326,995	7,394,150	7,416,947	7,435,650	Patent No.
TRENCH MIS DEVICE HAVING IMPLANTED DRAIN- DRIFT REGION AND THICK BOTTOM OXIDE	TRENCH MIS DEVICE HAVING IMPLANTED DRAIN- DRIFT REGION AND THICK BOTTOM OXIDE	SEMICONDUCTOR PACKAGE INCLUDING DIE INTERPOSED BETWEEN CUP- SHAPED LEAD FRAME AND LEAD FRAME HAVING MESAS AND VALLEYS	METHOD OF FABRICATING TRENCH MIS DEVICE WITH THICK OXIDE LAYER IN BOTTOM OF TRENCH	PROCESS FOR MANUFACTURING TRENCH MIS DEVICE HAVING IMPLANTED DRAIN- DRIFT REGION AND THICK BOTTOM OXIDE	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED ISSUED	ISSUED	ISSUED	Status
6/4/2003	6/22/2005	11/23/2004	1/19/2006	6/21/2004	File Date
1 1/6/2007	2/5/2008	7/1/2008	8/26/2008	10/14/2008	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

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UTL	UTL	UTL	UTL	TITU	UTL	Туре
10/810,031	11/141,942	10/836,833	11/150,016	10/996,149	11/232,613	Serial No.
7,045,857	7,118,953	7,183,610	7,233,043	7,238,551	7,268,032	Patent No.
TERMINATION FOR TRENCH MIS DEVICE HAVING IMPLANTED DRAIN- DRIFT REGION	PROCESS OF FABRICATING TERMINATION REGION FOR TRENCH MIS DEVICE	SUPER TRENCH MOSFET INCLUDING BURIED SOURCE ELECTRODE AND METHOD OF FABRICATING THE SAME	TRIPLE-DIFFUSED TRENCH MOSFET	METHOD OF FABRICATING SEMICONDUCTOR PACKAGE INCLUDING DIE INTERPOSED BETWEEN CUP- SHAPED LEAD FRAME HAVING MESAS AND VALLEYS	TERMINATION FOR TRENCH MIS DEVICE HAVING IMPLANTED DRAIN- DRIFT REGION	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
3/26/2 004	6/1/2005	4/30/2004		11/23/2004	9/21/2005	File Date
5/16/2006	10/10/2006	2/27/2007	6/19/2007	7/3/2007	9/11/2007	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

UTL	UTL	UTL	UTL	UTL	UTL	Type
10/657,830	10/264,816	10/811,443	10/722,984	10/180,154	10/326,311	Serial No.
6,913,977	6,921,697	6,927,451	7,009,247	7,012,005	7,033,876	Patent No.
TRIPLE-DIFFUSED TRENCH MOSFET AND METHOD OF FABRICATING THE SAME	METHOD FOR MAKING TRENCH MIS DEVICE WITH REDUCED GATE-TO- DRAIN CAPACITANCE	TERMINATION FOR TRENCH MIS DEVICE HAVING IMPLANTED DRAIN- DRIFT REGION	TRENCH MIS DEVICE WITH THICK OXIDE LAYER IN BOTTOM OF GATE CONTACT TRENCH	SELF-ALIGNED DIFFERENTIAL OXIDATION IN TRENCHES BY ION IMPLANTATION	TRENCH MIS DEVICE HAVING IMPLANTED DRAIN- DRIFT REGION AND THICK BOTTOM OXIDE AND PROCESS FOR MANUFACTURING THE SAME	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
9/8/2003	10/3/2002	3/26/2004	11/25/2003	6/25/2002	12/19/2002	<u>File Date</u>
7/5/2005	7/26/2005	8/9/2005	3/7/2006	3/14/2006	4/25/2006	<u>Issue Date</u>
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

UTL 10/104,811 6,838,722 FABRICATING TRENCH-GATED MIS DEVICES	UTL 09/927,143 6,849,898 TRENCH MIS  OF THICK BOTTOM OXIDE AND METHOD OF MAKING THE SAME	UTL 10/106,896 6,875,657 GRADUATED GATE OXIDE LAYER	UTL 09/927,320 6,882,000 REDUCED GATE-TO- DRAIN CAPACITANCE	UTL 10/106,812 6,903,412 GRADUATED GATE OXIDE LAYER	UTL 10/291,153 6,909,170 SEMICONDUCTOR ASSEMBLY WITH PACKAGE USING CUP-SHAPED LEAD FRAME	
URES OF HODS OF ATING ISSUED VICES	H MIS  WITH  TRENCH RS AND OTTOM S AND OD OF THE SAME	OD OF 'ATING 'H MIS 'E WITH 'ED GATE LAYER  ISSUED	H MIS WITH GATE-TO- ISSUED AIN TANCE	H MIS WITH ED GATE LAYER ISSUED	DUCTOR LY WITH E USING PED LEAD ME	(1 attil Description) Status
3/22/2002	8/10/2001	3/26/2002	8/10/2001	3/26/2002	11/7/2002	File Date
1/4/2005	2/1/2005	4/5/2005	4/19/2005	6/7/2005	6/21/2005	ISSUE D'AIE
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Farty
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UTL	UTL	UTL	UTL	UTL	UTL	Type
08/800,972	10/211,438	08/851,608	10/176,570	09/468,429	10/317,568	Serial No.
6,590,440	6,600,193	6,627,950	6,709,930	6,744,124	6,764,906	Patent No.
LOW-SIDE BIDIRECTIONAL BATTERY DISCONNECT SWITCH	TRENCH MOSFET HAVING IMPLANTED DRAIN- DRIFT REGION	TRENCH DMOS POWER TRANSISTOR WITH FIELD-SHAPING BODY PROFILE AND THREE- DIMENSIONAL GEOMETRY	THICKER OXIDE FORMATION AT THE TRENCH BOTTOM BY SELECTIVE OXIDE DEPOSITION	SEMICONDUCTOR DIE PACKAGE INCLUDING CUP- SHAPED LEADFRAME	METHOD FOR MAKING TRENCH MOSFET HAVING IMPLANTED DRAIN- DRIFT REGION	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
2/19/1997	8/2/2002	5/5/1997	6/21/2002	12/10/1999	12/12/2002	File Date
7/8/2003	7/29/2003	9/30/2003	3/23/2004	6/1/2004	7/20/2004	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	<u>Domestic Loan Party</u>
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	<u>Reel/Frame</u>

	UTL	UTL	TTU	UTL	TTU	UTL	UTL	Type
UTL								<u>pe</u>
09/089,310	09/293,380	09/476,320	09/545,287	09/037,557	10/094,476	09/816,717	09/898,652	Serial No.
6,249,041	6,277,695	6,285,060	6,392,290	6,476,442	6,509,233	6,534,366	6,569,738	Patent No.
IC CHIP PACKAGE WITH DIRECTLY	METHOD OF FORMING VERTICAL PLANAR DMOSFET WITH SELF-ALIGNED CONTACT	BARRIER ACCUMULATION MODE MOSFET	VERTICAL STRUCTURE FOR SEMICONDUCTOR WAFER-LEVEL CHIP SCALE PACKAGES	PSEUDO-SCHOTTKY DIODE	METHOD OF MAKING TRENCH- GATED MOSFET HAVING CESIUM GATE OXIDE LAYER	METHOD OF FABRICATING TRENCH-GATED POWER MOSFET	PROCESS FOR MANUFACTURING TRENCH GATED MOSFET HAVING DRAIN/DRIFT REGION	Title: (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
6/2/1998	4/16/1999	12/30/1999	4/7/2000	3/9/1998	3/7/2002	3/21/2001	7/3/2001	File Date
6/19/2001	8/21/2001	9/4/2001	5/21/2002	11/5/2002	1/21/2003	3/18/2003	5/27/2003	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	<u>Domestic Loan Party</u>
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	<u>Reel/Frame</u>

PRV 61/257,362	Design 29/151,069	Design 29/151,024	UTL 09/502,546	UTL 09/481,135	UTL 08/487,789	UTL 09/089,250	UTL 08/919,386	Type Serial No.
362	069 D,472,528	024 D,466,873	546 6,300,744	135 6,444,527	789 5,925,411	250 6,204,533	386 6,239,463	No. Patent No.
TRANSISTOR STRUCTURE WITH FEED THROUGH SOURCE-TO- SUBSTRATE CONTACT	SEMICONDUCTOR CHIP PACKAGE	SEMICONDUCTOR CHIP PACKAGE	HIGH-EFFICIENCY BATTERY CHARGER	METHOD OF OPERATION OF PUNCH-THROUGH FIELD EFFECT TRANSISTOR	GAS-BASED SUBSTRATE DEPOSITION PROTECTION	VERTICAL TRENCH- GATED POWER MOSFET HAVING STRIPE GEOMETRY AND HIGH CELL DENSITY	LOW RESISTANCE POWER MOSFET OR OTHER DEVICE CONTAINING SILICON- GERMANIUM LAYER	<u>Title:</u> (Patent Description)
PENDING	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Ganssi	ISSUED	Status
	10/31/2002	10/31/2002	2/10/2000	1/11/2000	6/7/1995	6/2/1998	8/28/1997	File Date
11/2/2009	4/1/2003	12/10/2002	10/9/2001	9/3/2002	7/20/1999	3/20/2001	5/29/2001	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

UTL	UTL	UTL	UTL	UTL	UTL	PRV	Type
06/757,582	08/225,270	07/802,352	07/451,518	08/777,636	07/498,170	61/309,824	Serial No.
4,682,405	5,416,039	5,243,212	5,108,940	5,866,931	5,132,753		Patent No.
METHOD FOR FORMING AN ELECTRICAL CONTACT IN A TRANSISTOR	METHOD OF MAKING DICDMOS STRUCTURES	A TRANSISTOR WITH A CHARGE INDUCED DRAIN EXTENSION	A MOS TRANSISTOR WITH A CHARGE INDUCED DRAIN EXTENSION	DMOS POWER TRANSISTOR WITH REDUCED NUMBER OF CONTACTS USING INTEGRATED BODY-SOURCE CONNECTIONS	OPTIMIZATION OF BV AND RDS-ON BY GRADED DOPING IN LDD AND OTHER HIGH VOLTAGE ICS	STRUCTURES OF AND METHODS OF FABRICATING DUAL GATE MIS DEVICES	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	PENDING	<u>Status</u>
7/22/1985	4/8/1994	12/4/1991	12/15/1989	12/31/1996	3/23/1990	3/2/2010	File Date
7/28/1987	5/16/1995	9/7/1993	4/28/1992	2/2/1999	7/21/1992		<u>Issue Date</u>
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

025675/0001	Siliconix incorporated	1/17/1989	3/10/1986	ISSUED	METHOD FOR MANUFACTURING A POWER MOS TRANSISTOR	4,798,810	06/838,217	UTL
025675/0001	Siliconix incorporated	1/23/1990	9/8/1988	ISSUED	VERTICAL DMOS POWER TRANSITOR WITH AN INTEGRAL OPERATING CONDITION SENSOR	4,896,196	07/243,166	UTL
025675/0001	Siliconix incorporated	10/18/1988	12/13/1985	ISSUED	INSULATED GATE TRANSISTOR ARRAY	4,779,123	06/808,904	UTL
025675/0001	Siliconix incorporated	7/26/1988	8/12/1987	ISSUED	ION IMPLANTATION OF THIN FILM CRSI2 AND SIC RESISTORS	4,759,836	07/084,541	UTL
025675/0001	Siliconix incorporated	4/25/1989	2/5/1987	ISSUED	METHOD FOR OBTAINING REGIONS OF DIELECTRICALLY ISOLATED SINGLE CRYSTAL SILICON	4,824,795	07/010,924	UTL
025675/0001	Siliconix incorporated	12/18/1990	7/25/1986	ISSUED	CURRENT SOURCE WITH A PROCESS SELECTABLE TEMPERATURE COEFFICIENT	4,978,631	06/890,218	UTL
025675/0001	Siliconix incorporated	8/23/1988	1/6/1986	ISSUED	INTEGRATED BURIED ZENER DIODE AND TEMPERATURE COMPENSATION TRANSISTOR	4,766,469	06/816,593	UTL
025675/0001	Siliconix incorporated	10/30/2002	12/21/1995	ISSUED	METHOD FOR MAKING TERMINATION STRUCTURE FOR POWER MOSFET	0895290	98111605. 6	UTL
Reel/Frame	Domestic Loan Party	Issue Date	File Date	Status	<u>Title:</u> (Patent Description)	Patent No.	Serial No.	Type

UTL	UTL	UTL	UTL	UTL	UTL	UTL	UTL	Type
07/246,937	07/195,436	07/036,777	09/978,603	06/871,006	07/138,989	06/808,575	06/894,418	Serial No.
4,920,388	4,794,436	4,853,563	6,744,119	4,716,126	4,816,882	4,674,020	4,707,909	Patent No.
POWER TRANSISTOR WITH INTEGRATED GATE RESISTOR	HIGH VOLTAGE DRIFTED-DRAIN MOS TRANSISTOR	SWITCH INTERFACE CIRCUIT FOR POWER MOSFET GATE DRIVE CONTROL	LEADFRAME HAVING SLOTS IN A DIE PAD	FABRICATION OF DOUBLE DIFFUSED METAL OXIDE SEMICONDUCTOR TRANSISTOR	POWER MOS TRANSISTOR WITH EQUIPOTENTIAL RING	POWER SUPPLY HAVING DUAL RAMP CONTROL CIRCUIT	MANUFACTURE OF TRIMMABLE HIGH VALUE POLYCRYSTALLINE SILICON RESISTORS	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
9/19/1988	5/16/1988	4/10/1987	10/15/2001	6/5/1986	12/29/1987	12/13/1985	8/8/1986	<u>File Date</u>
4/24/1990	12/27/1988	8/1/1989	6/1/2004	12/29/1987	03/28/1989	6/16/1987	11/24/1987	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

U	U.	UTL	U.	U	U	U	<u>Type</u>
UTL	UTL	TL	UTL	UTL	UTL	UTL	pe
07/849,723	09/135,716	12/401,549	10/789,799	10/113,526	06/927,882	07/014,961	Serial No.
5,218,228			7,501,086B2	6,856,006	4,827,324	4,799,100	Patent No.
METHOD FOR FABRICATING A HIGH VOLTAGE MOS TRANSISTOR	MULTILAYER SOLDER/BARRIER ATTACH FOR SEMICONDUCTOR CHIP	LEADLESS SEMICONDUCTOR PACKAGES	ENCAPSULATION METHOD FOR LEADLESS SEMICONDUCTOR PACKAGES	ENCAPSULATION METHOD AND LEADFRAME FOR LEADLESS SEMICONDUCTOR PACKAGES (as amended)	IMPLANTATION OF IONS INTO AN INSULATING LAYER TO INCREASE PLANAR PN JUNCTION BREAKDOWN VOLTAGE	METHOD AND APPARATUS FOR INCREASING BREAKDOWN OF A PLANAR JUNCTION	<u>Title:</u> (Patent Description)
ISSUED	PENDING	PENDING	ISSUED	ISSUED	ISSUED	ISSUED	Status
3/11/1992	8/17/1998	3/10/2009	2/27/2004	3/28/2002	11/6/1986	2/17/1987	<u>File Date</u>
6/8/1993			3/10/2009	2/15/2005	5/2/1989	1/17/1989	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

UTL	UTL	UTL	UTL	UTL	UTL	UTL	UTL	Type
07/089,184	09/314,621	07/141,877	07/453,367	07/167,617	07/138,999	07/095,481	07/678,578	Serial No.
4,774,196	6,268,242	4,936,930	4,958,204	4,967,245	4,914,058	4,791,462	5,132,235	Patent No.
METHOD OF BONDING SEMICONDCUTOR WAFERS	METHOD OF FORMING VERTICAL MOSFET DEVICE HAVING VOLTAGE CLAMPED GATE AND SELF-ALIGNED CONTACT	METHOD FOR IMPROVED ALIGNMENT FOR SEMICONDUCTOR DEVICES WITH BURIED LAYERS	JUNCTION FIELD- EFFECT TRANSISTOR WITH A NOVEL GATE	TRENCH POWER MOSTEF DEVICE	GROOVED DMOS PROCESS WITH VARYING GATE DIELECTRIC THICKNESS	DENSE VERTICAL J- MOS TRANSISTOR	METHOD FOR FABRICATING A HIGH VOLTAGE MOS TRANSISTOR	<u>Title:</u> (Patent Description)
ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	Status
8/25/1987	5/19/1999	1/6/1988	12/21/1989	3/14/1988	12/19/1987	9/10/1987	3/29/1991	File Date
9/27/1988	7/31/2001	6/26/1990	9/18/1990	10/30/1990	4/3/1990	12/13/1988	7/21/1992	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	<u>Domestic Loan Party</u>
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

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UTL	UTL	UTL	UTL	UTL	UTL	UTL	UTL	UTL	Type
12/487,666	11/151,749	07/133,710	07/268,839	07/406,844	07/107,725	07/115,076	07/099,452	07/334,806	Serial No.
	7,595,547	4,890,146	5,156,989	4,952,992	5,164,325	4,845,051	4,835,586	4,929,991	Patent No.
SEMICONDUCTOR PACKAGING TECHNIQUES	SEMICONDUCTOR DIE PACKAGE INCLUDING CUP- SHAPED LEADFRAME	HIGH VOLTAGE LEVEL SHIFT SEMICONDUCTOR DEVICE	COMPLEMENTARY, ISOLATED DMOS IC TECHNOLOGY	METHOD AND APPARATUS FOR IMPROVING THE ON- CHARACTERISTICS OF A SEMICONDUCTOR DEVICE	METHOD OF MAKING A VERTICAL CURRENT FLOW FIELD EFFECT TRANSISTOR	BURIED GATE JFET	DUAL-GATE HIGH DENSITY FET	RUGGED LATERAL DMOS TRANSISTOR STRUCTURE	<u>Title:</u> (Patent Description)
PENDING	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	ISSUED	<u>Status</u>
6/19/2009	6/13/2005	12/16/1987	1 1/8/1988	9/13/1989	10/8/1987	10/29/1987	9/21/1987	4/5/1989	<u>File Date</u>
	9/29/2009	12/26/1989	10/20/1992	8/28/1990	11/17/1992	7/4/1989	5/30/1989	5/29/1990	<u>Issue Date</u>
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	<u>Reel/Frame</u>

	UTL 10/898,431 7,335,946	UTL 10/832,776 7,005,347	UTL 07/285,842 5,055,896 T	UTL 07/290,546 5,072,266 Bt	Type Serial No. Patent No.
STRUCTURES OF AND METHOD OF FABRICATING	STRUCTURES OF AND METHOD OF FABRICATING TRENCH-GATED MIS DEVICES	STRUCTURES OF AND METHOD OF FABRICATING TRENCH-GATED MIS DEVICES	SELF-ALIGNED LDD LATERAL DMOS TRANSISTOR WITH HIGH-VOLTAGE INTERCONNECT CAPABILITY	TRENCH DMOS POWER TRANSISTOR WITH FIELD-SHAPING BODY PROFILE AND THREE- DIMENSIONAL GEOMETRY	Title: (Patent Description)
PENDING	ISSUED	ISSUED	ISSUED	ISSUED	Status
11/5/2007	7/22/2004	4/27/2004	12/15/1988	12/27/1988	<u>File Date</u>
	2/26/2008	2/28/2006	10/8/1991	12/10/1991	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	<u>Reel/Frame</u>

UTL 10/951,831 7,642,164B1	UTL 10/378,766	UTL 10/254,385	UTL 09/908,178 6,552,889	UTL 11/112,403 7,494,876
METHOD OF FORMING SELF ALIGNED CONTACTS FOR A POWER MOSFET	METHOD OF FORMING SELF ALIGNED CONTACTS FOR A POWER MOSFET METHOD OF FORMING SELF	METHOD OF FORMING SELF ALIGNED CONTACTS FOR A POWER MOSFET	CURRENT LIMITING TECHNIQUE FOR HYBRID POWER MOSFET CIRCUITS	TRENCH-GATED MIS DEVICE HAVING THICK POLYSLICON INSULATION LAYER TRENCH BOTTOM AND METHOD OF FABRICATING THE SAME
ISSUED	PENDING	PENDING	ISSUED	ISSUED
9/27/2004	3/3/2003	9/24/2002	7/17/2001	4/21/2005
1/5/2010			4/22/2003	2/24/2009
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001

UTL	UTL	UTL	UTL	UTL	UTL	Туре
12/107,738	11/040,129	10/726,922	11/724,961	10/869,382	10/247,906	Serial No.
7,833,863	7,361,558	7,279,743			6,858,471	Patent No.
METHOD OF MANUFACTURING A ISSUED CLOSED CELL TRENCH MOSFET	METHOD OF MANUFACTURING A CLOSED CELL TRENCH MOSFET	CLOSED CELL TRENCH METAL- OXIDE- SEMICONDUCTOR FIELD EFFECT TRANSISTOR	SELF-ALIGNED CONTACT IN A SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME	SELF-ALIGNED CONTACT IN A SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME	SEMICONDUCTOR SUBSTRATE WITH TRENCHES FOR REDUCING SUBSTRATE RESISTANCE	<u>Title:</u> (Patent Description)
	ISSUED	ISSUED	PENDING	PENDING	ISSUED	Status
4/22/2008	1/20/2005	12/2/2003	3/16/2007	6/15/2004	9/20/2002	<u>File Date</u>
11/16/2010	4/22/2008	10/9/2007			2/22/2005	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

UTL	UTL	UTL	UTL	UTL	UTL	Type
11/386,927	12/571,194	11/352,031	11/023,327	12/050,929	10/846,339	Serial No.
			7,344,945		6,906,380	Patent No.
ULTRA-LOW DRAIN-SOURCE RESISTANCE POWER MOSFET	ADAPTIVE FREQUENCY COMPENSATION FOR DC-TO-DC CONVERTER	ADAPTIVE FREQUENCY COMPENSATION FOR DC-TO-DC CONVERTER	METHOD OF MANUFACTURING A DRAIN SIDE GATE TRENCH METAL- OXIDE- SEMICONDUCTOR FIELD EFFECT TRANSISTOR	STACKED TRENCH- OXIDE- OXIDE- SEMICONDUCTOR FIELD EFFECT TRANSISTOR DEVICE	DRAIN SIDE GATE TRENCH METAL- OXIDE- SEMICONDUCTOR FIELD EFFECT TRANSISTOR	<u>Title:</u> (Patent Description)
ALLOWED	ALLOWED	ALLOWED	ISSUED	PENDING	ISSUED	Status
3/21/2006	9/30/2009	2/10/2006	12/22/2004	3/18/2008	5/13/2004	File Date
			3/18/2008		6/14/2005	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	<u>Reel/Frame</u>

UTL	UTL	UTL	UTL	UTL	UTL	UTL	UTL	Type
11/322,040	11/710,041	12/552,205	11/190,682	12/030,809	11/373,630	11/799,889	12/069,712	<u>Serial No.</u>
7,544,545B2			7,583,485B1					Patent No.
TRENCH POLYSILICON DIODE	PROCESS FOR FORMING A SHORT CHANNEL TRENCH MOSFET AND DEVICE FORMED THEREBY	ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT FOR INTEGRATED CIRCUITS	ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT FOR INTEGRATED CIRCUITS	NARROW SEMICONDUCTOR TRENCH STRUCTURE	NARROW SEMICONDUCTOR TRENCH STRUCTURE	POWER MOSFET CONTACT METALLIZATION	ULTR-LOW DRAIN- SOURCE RESISTANCE POWER MOSFET	Title: (Patent Description)
ISSUED	PENDING	PENDING	ISSUED	PENDING	PENDING	PENDING	PENDING	Status
12/28/2005	2/23/2007	9/1/2009	7/26/2005	2/13/2008	3/9/2006	5/2/2007	2/11/2008	<u>File Date</u>
6/9/2009			9/1/2009					Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

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UTL	UTL	UTL	UTL	UTL	UTL	UTL	Type
11/479,619	12/779,815	11/479,671	11/651,258	12/098,950	12/611,865	12/009,379	Serial No.
						7,612,431B2	Patent No.
POWER MANAGEMENT SYSTEM IMPLEMENTED IN A SINGLE SURFACE MOUNT PACKAGE	COMPLETE POWER MANAGEMENT SYSTEM IMPLEMENTED IN A SINGLE SURFACE MOUNT PACKAGE	POWER MANAGEMENT SYSTEM IMPLEMENTED IN A SINGLE, SURFACE MOUNT PACKAGE	HIGH-DENSITY POWER MOSFET WITH PLANARIZED METALIZATION	TRENCH METAL OXIDE SEMICONDUCTOR WITH RECESSED TRENCH MATERIAL AND REMOTE CONTACTS	TRENCH POLYSILICON DIODE	TRENCH POLYSILICON DIODE	<u>Title:</u> (Patent Description)
PENDING	PENDING	PENDING	PENDING	PENDING	PENDING	ISSUED	Status
6/30/2006	5/13/2010	6/30/2006	1/8/2007	4/7/2008		1/17/2008	File Date
						11/3/2009	Issue Date
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

025675/0001	Siliconix incorporated		5/12/2008	PENDING	HIGH CURRENT DENSITY POWER FIELD EFFECT TRANSISTOR		12/119,367	UTL
025675/0001	Siliconix incorporated		9/3/2008	PENDING	MOSFET ACTIVE AREA AND EDGE TERMINATION CHARGE BALANCE		12/203,846	UTL
025675/0001	Siliconix incorporated		2/13/2008	PENDING	SELF-REPAIRING FIELD EFFECT TRANSISTOR		12/030,719	UTL
025675/0001	Siliconix incorporated		1/17/2008	PENDING	SELF-ALIGNED TRENCH MOSFET AND METHOD OF MANUFACTURE		12/015,723	UTL
025675/0001	Siliconix incorporated		6/26/2007	PENDING	A CURRENT MODE BOOST CONVERTER USING SLOPE COMPENSATION		11/823,375	UTL
025675/0001	Siliconix incorporated		1/18/2007	PENDING	FLOATING GATE STRUCTURE WITH HIGH ELECTROSTATIC DISCHARGE PERFORMANCE		11/655,493	UTL
025675/0001	Siliconix incorporated		5/20/2008	ALLOWED	HIGH MOBILITY POWER METAL- OXIDE SEMICONDUCTOR FIELD-EFFECT TRANSISTORS		12/123,664	UTL
025675/0001	Siliconix incorporated		12/22/2006	PENDING	HIGH MOBILITY POWER METAL- OXIDE SEMICONDUCTOR FIELD-EFFECT TRANSISTORS		11/644,553	UTL
Reel/Frame	Domestic Loan Party	Issue Date	File Date	Status	<u>Title:</u> (Patent Description)	Patent No.	Serial No.	<u>Type</u>

UTL	UTL	UTL	UTL	UTL	UTL	UTL	UTL	Type
12/824,075	61/257,362	12/610,148	12/829,247	12/873,147	12/549,190	12/548,841	12/603,028	Serial No.
								Patent No.
FIELD BOOSTED METAL-OXIDE- SEMICONDUCTOR FIELD EFFECT TRANSISTOR	TRANSISTOR STRUCTURE WITH FEED THROUGH SOURCE-TO - SUBSTRATE CONTACT	SEMICONDUCTOR DEVICE WITH TRENCH-LIKE FEED-THROUGHS	POWER SWITCH WITH ACTIVE SNUBBER	SYSTEM AND METHOD FOR SUBSTRATE WAFER BACK SIDE AND EDGE CROSS SECTION SEALS	SUPER JUNCTION TRENCH POWER MOSFET DEVICE FABRICATION	SUPER JUNCTION TRENCH POWER MOSFET DEVICES	SPLIT GATE SEMICONDUCTOR DEVICE WITH CURVED GATE OXIDE PROFILE	Title: (Patent Description)
PENDING	PENDING	PENDING	PENDING	PENDING	PENDING	PENDING	PENDING	Status
6/25/2010	11/02/2009	10/30/2009	7/1/2010	8/31/2010	8/27/2009	8/27/2009	10/21/2009	<u>File Date</u>
						8/27/2009		<u>Issue Date</u>
Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Siliconix incorporated	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	<u>Reel/Frame</u>

Siliconix incorporated		3/9/2006	PENDING	NARROW SEMICONDUCTOR TRENCH STRUCTURE		11/373,630	UTL
Siliconix incorporated	07/26/2005	10/03/2002	ISSUED	METHOD FOR MAKING TRENCH MIS DEVICE WITH REDUCED GATE-TO- DRAIN CAPACITANCE	6,921,697	10/264,816	UTL
Siliconix incorporated	2/19/2002	10/27/1999	ISSUED	HIGH DENSITY TRENCH-GATED POWER MOSFET	6,348,712	09/428,299	UTL
	3/6/2007	5/14/2002	ISSUED	METHOD OF FABRICATING TRENCH JUNCTION BARRIER ERCTIFIER	7,186,609	10/146,539	UTL
		3/02/2010	PENDING	STRUCTURES OF AND METHODS OF FABRICATING DUAL GATE MIS DEVICES		61/309,824	UTL
		3/24/2010	PENDING	SEMICONDUCTOR PACKAGES INCLUDING DIE AND L-SHAPED LEAD AND METHOD OF MANUFACTURING		12/730,230	UTL
		5/26/2010	PENDING	SUPER-HIGH DENSITY POWER TRENCH MOSFET		12/788,158	TTU
		8/26/2010	PENDING	STRUCTURES OF AND METHODS OF FABRICATING SPLIT GATE MIS DEVICES		12/869,554	TLU
	Issue Date	<u>File Date</u>	<u>Status</u>	<u>Title:</u> (Patent Description)	Patent No.	Serial No.	Туре

031170/0001	Siliconix incorporated		7/17/2012	PENDING	CURRENT MODE BOOST CONVERTER USING SLOPE COMPENSATION		13/551,516	UTL
031170/0001	Siliconix incorporated		5/30/2012	PENDING	ADAPTIVE CHARGE BALANCED EDGE TERMINATION		13/484,114	UTL
031170/0001	Siliconix incorporated		5/22/2012	PENDING	STACKED TRENCH METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR DEVICE		13/478,037	UTL
031170/0001	Siliconix incorporated		5/18/2012	PENDING	SEMICONDUCTOR DEVICE HAVING REDUCED GATE CHARGES AND SUPERIOR FIGURE OF MERIT		13/475,255	TLU
031170/0001	Siliconix incorporated		4/30/2012	PENDING	METHOD OF FORMING A HYBRID SPLIT GATE SEMICONDUCTOR		13/460,600	TLU
031170/0001	Siliconix incorporated		4/30/2012	PENDING	HYBRID SPLIT GATE SEMICONDUCTOR		13/460,567	TTU
031170/0001	Siliconix incorporated		2/9/2012	FILED	STRUCTURES OF AND METHODS OF FABRICATING POWERMOS WITH TERMINATION TRENCH HAVING THICK OXIDE FOR THE HIGH BDdss		13/370,243	UTL
Reel/Frame	Domestic Loan Party	Issue Date	File Date	Status	<u>Title:</u> (Patent Description)	Patent No.	Serial No.	Туре

031170/0001	Siliconix incorporated		3/14/2013	PENDING	METHOD OF FABRICATING STACKED DIE PACKAGE		13/830,041	UTL
031170/0001	Siliconix incorporated		3/14/2013	PENDING	POWER MOSFET PACKAGE WITH STACK DIE, LDMOS DIE STRUCTURE, FLIP CHIP ON LEADFRAME AND SOURCE, DRAIN AND GATE CLIPS		13/829,623	UTL
031170/0001	Siliconix incorporated		12/31/2012	PENDING	ADAPTIVE CHARGE BALANCED MOSFET TECHNIQUES		13/732,284	UTL
1000/071160	Siliconix incorporated		12/27/2012	PENDING	TRENCH METAL OXIDE SEMICONDUCTOR WITH RECESSED TRENCH MATERIAL AND REMOTE CONTACTS		13/728,997	UTL
031170/0001	Siliconix incorporated		10/17/2012	PENDING	POWER MOSFET CONTACT METALIZATION		13/654,230	UTL
000/071180	Siliconix incorporated		9/19/2012	PENDING	BREAKDOWN VOLTAGE BLOCKING DEVICE		13/622,997	UTL
1000/071150	Siliconix incorporated		9/18/2012	PENDING	HIGH CURRENT DENSITY POWER FIELD EFFECT TRANSISTOR		13/622,322	UTL
1000/071120	Siliconix incorporated		8/2/2012	PENDING	PREVENTING REVERSE CONDUCTION		13/565,672	UTL
Reel/Frame	<u>Domestic Loan Party</u>	<u>Issue Date</u>	<u>File Date</u>	<u>Status</u>	<u>Title:</u> (Patent Description)	Patent No.	Serial No.	Туре

#### Type UTL UTL 08/487,789 13/867,964 Serial No. Patent No. 5,925,411 CURRENT LIMITING SYSTEMS AND <u>Title:</u> (Patent Description) GAS-BASED SUBSTRATE **PROTECTION** DEPOSITION METHODS PENDING ISSUED Status 4/22/2013 File Date 6/7/1995 Issue Date 7/20/1999 Siliconix incorporated Siliconix incorporated Domestic Loan Party 031170/0001 031170/0001 Reel/Frame

## (b) U.S. Trademarks and Trademark Applications

004453/0500	12/18/2009	77/896,876	United States	Siliconix incorporated	VRPower
004453/0500	12/23/2009	77/900,236	United States	Siliconix incorporated	MICROBUCK
004453/0500	8/4/2009	3,662,946	United States	Vishay Siliconix Technology C.V. composed of Siliconix incorporated, General Partner, Siliconix Semiconductor, Inc. and Vishay Siliconix LLC	FRED PT
004453/0500	11/3/2009	3,704,345	United States	Vishay Siliconix Technology C.V. composed of Siliconix incorporated, General Partner, Siliconix Semiconductor, Inc. and Vishay Siliconix LLC	POWERTAB
004453/0500	2/23/1993	1,753,724	United States	Vishay Siliconix Technology C.V.	HEXFRED
004453/0500	3/28/2006	3,073,909	United States	Vishay Siliconix Technology C.V.	FLIPKY
004453/0500	3/9/2010	3759042	United States	Siliconix incorporated	TurboFET
004453/0500	1/7/2003	2672428	United States	Siliconix incorporated	POWERPAK
004453/0500	2/4/1997	2035560	United States	Siliconix incorporated	TRENCHFET
004453/0500	7/15/2008	3469285	United States	Siliconix incorporated	SKYFET
004453/0500	5/2/2006	3087499	United States	Siliconix incorporated	SI STYLIZED
004453/0500	12/29/2009	3732445	United States	Siliconix incorporated	POWERPAIR
004453/0500	8/30/2005	2990388	United States	Siliconix incorporated	POLARPAK
004453/0500	3/25/2003	2701037	United States	Siliconix incorporated	MICRO FOOT
004453/0500	10/27/1992	1727230	United States	Siliconix incorporated	LITTLE FOOT
004453/0500	3/11/2003	2696001	United States	Siliconix incorporated	CHIPFET
Reel/Frame	Reg. Date	Reg.#	Country	Legal Owner	Trademark

5105/0896	8/28/2012	4,198,891	United States	Siliconix incorporated	VRPower
5105/0896	11/22/2011	4,060,661	United States	Siliconix incorporated	THUNDERFET
5105/0896	11/8/2011	4,053,107	United States	Siliconix incorporated	SILICONIX
5105/0896	12/2/1975	3.929,833	United States	Siliconix incorporated	MICROBUCK
004453/0500	Filed 2/26/2010	77/945,647	United States	Siliconix incorporated	THUNDERFET
Reel/Frame	Reg. Date	Reg.#	Country	<u>Legal Owner</u>	<u>Trademark</u>

#### Patents and Trademarks of Vishay Sprague, Inc.

# (a) U.S. Patent Registrations and Patent Applications

Type	Serial No.	Patent No.	<u>Title:</u> (Patent Description)	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	Domestic Loan Party	<u>Reel/Frame</u>
UTL	09/441,434	6,184,775	SURFACE MOUNT RESISTOR	ISSUED	11/16/1999	2/6/2001	Vishay Sprague, Inc.	025675/0001
UTL	10/091,792	6,859,999	METHOD FOR MANUFACTURING A POWER CHIP RESISTOR	ISSUED	3/6/2002	3/1/2005	Vishay Techno Components, LLC	025675/0001
UTL	09/074,185	6,159,817	MULTI-TAP THIN FILM INDUCTOR	ISSUED	5/7/1998	12/12/2000	Vishay EFI, Inc.	025675/0001
UTL	11/759,523		CERAMIC DIELECTRIC FORMULATION FOR BROAD BAND UHF ANTENNA	PUBLISHED	6/7/2007		Vishay Sprague, Inc.	025675/0001
UTL	11/266,915	7,449,032	METHOD OF MANUFACTURING SURFACE MOUNT CAPACITOR	ISSUED	11/4/2005	11/11/2008	Vishay Sprague, Inc.	025675/0001
UTL	11/359,711	7,336,475	HIGH VOLTAGE CAPACITORS	ISSUED	2/22/2006	2/26/2008	Vishay Vitramon, Inc.	025675/0001
UTL	11/293,673	7,283,350	SURFACE MOUNT CHIP CAPACITOR	ISSUED	12/2/2005	10/16/2007	Vishay Sprague, Inc.	025675/0001
UTL	11/264,977	7,221,555	SURFACE MOUNT CHIP CAPACITOR	ISSUED	11/2/2005	5/22/2007	Vishay Sprague, Inc.	025675/0001
UTL	11/266,632	7,179,309	SURFACE MOUNT CHIP CAPACITOR	ISSUED	11/3/2005	2/20/2007	Vishay Sprague, Inc.	025675/0001
UTL	11/259,503	7,167,357	SURFACE MOUNT MELF CAPACITOR	ISSUED	10/26/2005	1/23/2007	Vishay Sprague, Inc.	025675/0001
UTL	11/132,116	7,161,797	SURFACE MOUNT CAPACITOR AND METHOD OF MAKING SAME	ISSUED	5/17/2005	1/9/2007	Vishay Sprague, Inc.	025675/0001
UTL	10/792,138	7,088,573	SURFACE MOUNT MELF CAPACITOR	ISSUED	3/2/2004	8/8/2006	Vishay Sprague, Inc.	025675/0001

TTU	UTL	UTL	UTL	UTL	UTL	UTL	UTL	UTL	UTL	UTL	<u>Type</u>
T	T	L	T	Ľ	L	Ľ	Ľ	Ľ	T	T	12
07/677,204	07/677,203	12/553,508	12/189,465	12/052,251	12/189,492	12/107,349	12/759,769	09/758,800	10/792,135	10/792,639	Serial No.
5,053,927	5,099,397							6,541,302	6,914,770	7,085,127	Patent No.
MOLDED FUZED SOLID ELECTROLYTE CAPACITOR	FUZED SOLID ELECTROLYTE CAPACITOR	BULK CAPACITOR AND METHOD	HIGH VOLTAGE CAPACITORS	ELECTROPHORETIC ALLY DEPOSITED CATHODE CAPACITOR	HIGH VOLTAGE CAPACITORS	FRAME PACKAGED ARRAY ELECTRONIC COMPONENT	HERMETICALLY SEALED WET ELECTROLYTIC CAPACITOR	METHOD OF FORMING TERMINATION ON CHIP COMPONENTS	SURFACE MOUNT FLIPCHIP CAPACITOR	SURFACE MOUNT CHIP CAPACITOR	Title: (Patent Description)
ISSUED	ISSUED	PUBLISHED	PUBLISHED	PUBLISHED	PUBLISHED	PUBLISHED	PUBLISHED	ISSUED	ISSUED	ISSUED	Status
3/29/1991	3/29/1991	9/3/2009	8/11/2008	3/20/2008	8/11/2008	4/22/2008	4/14/2010	1/11/2001	3/2/2004	3/2/2004	File Date
10/1/1991	3/24/1992							4/1/2003	7/5/2005	8/1/2006	Issue Date
Sprague Electric Company	Sprague Electric Company	Vishay Sprague, Inc.	Vishay Sprague, Inc.	Vishay Sprague, Inc.	Vishay Sprague, Inc.	Vishay Sprague, Inc.	Vishay Sprague, Inc.	Vishay Sprague, Inc.	Vishay Sprague, Inc.	Vishay Sprague, Inc.	Domestic Loan Party
025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	025675/0001	Reel/Frame

### U.S. Trademarks and Trademark Applications

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CERA_MITE   V:	SPRAGUE V	VITRAMON Vi	VITRAMON Vi	TANTAMOUNT Vi	SUPERTAN Vi	SPRAGUE Vi	SPECTROL Vis	MICROTAN Vi	HVARC GUARD Vi	<u>Trademark</u>
Vishay Sprague, Inc.	Vishay Thin Film, LLC	Vishay Sprague, Inc.	Vishay Sprague, Inc.	Legal Owner						
United States	United States	United States	Country							
2126097	3762167	839,908	1238139	1380243	1492049	859,975	858837	3526660	3256019	Reg.#
3/7/2000	3/23/2016	3/10/1966	5/17/1983	1/28/1986	6/14/1988	11/12/1968	10/22/1968	11/4/2008	6/26/2007	Reg. Date
004453/0500	004453/0500	004453/0500	004453/0500	004453/0500	004453/0500	004453/0500	004453/0500	004453/0500	004453/0500	Reel/Frame

TRADEMARK REEL: 006695 FRAME: 0304

RECORDED: 07/17/2019

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