TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1

Stylesheet Version v1.2

ETAS ID: TM536533

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
Chelsio Communications, Inc.		08/09/2019	Corporation: CALIFORNIA

RECEIVING PARTY DATA

Name:	Western Alliance Bank, an Arizona corporation
Street Address:	55 Almaden Boulevard, Suite 100
City:	San Jose
State/Country:	CALIFORNIA
Postal Code:	95113
Entity Type:	Corporation: ARIZONA

PROPERTY NUMBERS Total: 4

Property Type	Number	Word Mark
Serial Number:	78175893	CHELSIO COMMUNICATIONS
Serial Number:	78175890	
Serial Number:	78175534	CHELSIO COMMUNICATIONS
Serial Number:	78175529	CHELSIO

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone:	7033826485
Email:	DHall@VLPLawGroup.com
Correspondent Name:	Davis Hall
Address Line 1:	1029 N Stuart Street
Address Line 2:	Unit 200
Address Line 4:	Arlington, VIRGINIA 22201

NAME OF SUBMITTER:	Davis Hall
SIGNATURE:	/DavisHall/
DATE SIGNED:	08/14/2019

Total Attachments: 13

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OP $115.00 78175893

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INTELLECTUAL PROPERTY SECURITY AGREEMENT

This INTELLECTUAL PROPERTY SECURITY AGREEMENT, dated as of August 9, 2019 (the "Agreement"), between WESTERN ALLIANCE BANK, an Arizona corporation ("Lender") and CHELSIO COMMUNICATIONS, INC., a California corporation ("Grantor"), is made with reference to the Business Financing Agreement, dated as of September 5, 2018 (as amended from time to time, the "Financing Agreement'), between Lender and Grantor. Terms defined in the Financing Agreement have the same meaning when used in this Agreement.

For good and valuable consideration, receipt of which is hereby acknowledged, Grantor hereby covenants and agrees as follows:

To secure the Obligations under the Financing Agreement, Grantor grants to Lender a security interest in all right, title, and interest of Grantor in any of the following, whether now existing or hereafter acquired or created in any and all of the following property (collectively, the "Intellectual Property Collateral"):

(a)   copyright rights, copyright applications, copyright registrations and like protections in each work or authorship and derivative work thereof, whether published or unpublished and whether or not the same also constitutes a trade secret, now or hereafter existing, created, acquired or held (collectively, the "Copyrights"), including the Copyrights described in Exhibit A;

(b)   trademark and servicemark rights, whether registered or not, applications to register and registrations of the same and like protections, and the entire goodwill of the business of Borrower connected with and symbolized by such trademarks (collectively, the "Trademarks"), including the Trademarks described in Exhibit B;

(c)   patents, patent applications and like protections including without limitation improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the same (collectively, the "Patents"), including the Patents described in Exhibit C;

(d)   mask work or similar rights available for the protection of semiconductor chips or other products (collectively, the "Mask Works");

(e)   trade secrets, and any and all intellectual property rights in computer software and computer software products;

(f)   design rights;

(g)   claims for damages by way of past, present and future infringement of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above;

(h)   licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works, and all license fees and royalties arising from such use to the extent permitted by such license or rights;

(i)   amendments, renewals and extensions of any of the Copyrights, Trademarks, Patents, or Mask Works; and

(j)   proceeds and products of the foregoing, including without limitation all payments under insurance or any indemnity or warranty payable in respect of any of the foregoing.

The rights and remedies of Lender with respect to the security interests granted hereunder are in addition to those set forth in the Financing Agreement, and those which are now or hereafter available to Lender as a matter of law or equity. Each right, power and remedy of Lender provided for herein or in the Financing Agreement, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right, power or remedy provided for herein, and the exercise by Lender of any one or more of such rights, powers or remedies does not preclude the simultaneous or later exercise by Lender of any other rights, powers or remedies.

IN WITNESS WHEREOF, the parties have executed this Agreement as of the date first written above.

GRANTOR:	LENDER:
CHELSIO COMMUNICATIONS, INC., a California corporation	WESTERN ALLIANCE BANK, an Arizona corporation

By: _~Kaiwash Nahshinen~_

Name: _KIAWASH NAAHSHINEH_

Title: _CEO_

By: _~signature~_

Name: _Lisa Chang on behalf of Raelene Supple_
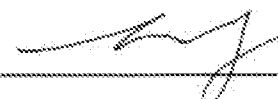
Title: _VP RM_

Address for Notices:
Attn:

209 North Fair Oaks Avenue
Sunnyvale, CA 94085
Fax: «Fax»

Address for Notices:
Attn:
55 Almaden Blvd. Ste. 100
San Jose, CA 95113
Tel: (408) 423-8500
Fax:(408) 423-8520

EXHIBIT A

COPYRIGHTS

Please Check if No Copyrights Exist **X**

Type of Work:	Title:	International Standard Serial Number (ISSN):	Registration Number:	Filing Date:	Preregistered?

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Exhibit B
TRADEMARKS

Please Check if No Trademarks Exist ☐

Mark / Title:	U.S. Serial Number:	U.S. Registration Number:	UPTO Reference Number:	Filing Date:
CHELSIO COMMUNICATIONS	78175893	3218510		10/18/2012
	78175890	3197200		10/18/2002
CHELSIO COMMUNICATIONS	78175534	3218509		10/17/2002
CHELSIO	78175529	3184329		10/17/2002

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EXHIBIT C

PATENTS

Please Check if No Patents Exist ☐

Title:	Patent Number:	Application Serial Number:	Issued or Published?	Issue Date:
Method for in-line TLS/SSL cleartext encryption and authentication	10225239	15279894		03/05/2019
Distributed cache coherent shared memory controller integrated with a protocol offload network interface card	9684597	14454564		06/20/2017
Method for efficient routing in a network interface card	9628370	15179710		04/18/2017
Method and apparatus for configuring and booting with more than one protocol using single option ROMBIOS code on multi function converged network adapter	9619245	13631266		04/11/2017
Network adaptor configured for connection establishment offload	9537878	14569584		01/03/2017
Method for out of order placement in PDU-oriented protocols	9444769	14675619		09/13/2016
Method for congestion control in a network interface card	9444754	14276947		09/13/2016
Multi-function interconnect having a plurality of switch	9413695	13622288		08/09/2016

building blocks				
Method for efficient routing in a network interface card	9390056	13330513		07/12/2016
Failover and migration for full-offload network interface devices	9357003	14513170		05/31/2016
Network adaptor configured for connection establishment offload	8935406	11735861		01/13/2015
Failover and migration for full-offload network interface devices	8886821	13690976		11/11/2014
Method for flow control in a packet switched network	8873389	12853248		10/28/2014
Intrusion detection and prevention processing within network interface circuitry	8856947	14099577		10/07/2014
Thin provisioning row snapshot with reference count map	8806154	13168886		08/12/2014
Virtualizing the operation of intelligent network interface circuitry	8686838	13081392		04/01/2014
Intrusion detection and prevention processing within network interface circuitry	8621627	12704884		12/31/2013
Protocol offload in intelligent network adaptor, including application level signalling	8589587	11747790		11/19/2013
Intelligent network adaptor with end-to-end flow control	8356112	13249077		01/15/2013
Failover and migration for full-	8346919	12749769		01/01/2013

offload network interface devices				
Protocol offload transmit traffic management	8339952	13413196		12/25/2012
Method for traffic scheduling in intelligent network interface circuitry	8213427	12643897		07/03/2012
Protocol offload transmit traffic management	8155001	12752719		04/10/2012
Method to implement an L4-L7 switch using split connections and an offloading NIC	8139482	12567581		03/20/2012
RDMA write completion semantics	8122155	12490242		02/21/2012
Intelligent network adaptor with end-to-end flow control	8060644	11747673		11/15/2011
Configurable switching network interface controller using forwarding engine	8032655	12255112		10/04/2011
Method for using a protocol language to avoid separate channels for control messages involving encapsulated payload data messages	7945705	11137146		05/17/2011
Virtualizing the operation of intelligent network interface circuitry	7924840	12645324		04/12/2011
Scalable direct memory access using validation of host and scatter gather engine (SGE) generation indications	7831745	11137140		11/09/2010
Full offload of stateful	7831720	12122570		11/09/2010

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connections, with partial connection offload				
Intelligent network adaptor with adaptive direct data placement scheme	7826350	11747650		11/02/2010
Filtering ingress packets in network interface circuitry	7760733	11250894		07/20/2010
Protocol offload transmit traffic management	7724658	11217661		05/25/2010
Method for UDP transmit protocol offload processing with traffic management	7715436	11282933		05/11/2010
Virtualizing the operation of intelligent network interface circuitry	7660306	11330898		02/09/2010
Method for traffic schedulign in intelligent network interface circuitry	7660264	11313003		02/09/2010
Method to implement an L4-L7 switch using split connections and an offloading NIC	7616563	11356850		11/10/2009
Multi-purpose switching network interface controller	7447795	10474500		11/04/2008
Reduced-overhead DMA	6813652	10474499		11/02/2004
INTELLIGENT NETWORK ADAPTOR WITH DDP OF OUT-OF-ORDER SEGMENTS		11747793		
METHOD FOR EFFICIENT TRAFFIC MANAGEMENT IN A NETWORK INTERFACE		13196749		

CARD			
REPLICATION IN A PROTOCOL OFFLOAD NETWORK INTERFACE CONTROLLER		14580117	
A METHOD TO INTEGRATE CO-PROCESSORS WITH A PROTOCOL PROCESSING PIPELINE		14804007	

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EXHIBIT D

Patent Applications in Process

CHELP034 REPLICATION IN A PROTOCOL OFFLOAD NETWORK INTERFACE CONTROLLER INVENTOR(S): EIRIKSSON APPLICATION NO.: 14/580,117

ABSTRACT

Data replication can be supported efficiently in a protocol offload device (such as a protocol offload device to offload transport layer protocol processing from a host) by supporting a shared memory (SHM) abstraction for the send and receive buffers that are used in protocol offload devices. The protocol offload send and receive buffers are accessed using a per offloaded connection virtual address method that maps transport protocol sequence numbers (such as TCP protocol sequence numbers), to memory locations within buffers, and, for example, either page tables and paged memory or segment tables and segmented memory tables are used to access the memory.

CHELP036 A METHOD TO INTEGRATE CO-PROCESSORS WITH A PROTOCOL PROCESSING PIPELINE Inventor(s): EIRIKSSON et al. Application No.: 14/804,007

ABSTRACT

A protocol offload device is implemented with a processing pipeline and the device is integrated with different operating systems with a suite of software. The current invention describes how coprocessors can be integrated with the protocol processing pipeline to implement additional features while retaining compatibility with the existing software

A METHOD FOR IN-LINE TLS/SSL CLEARTEXT ENCRYPTION AND AUTHENTICATION INVENTORS: ASGEIR EIRIKSSON, ATUL GUPTA, VENKATA SUMAN KUMAR M

ABSTRACT

We describe a method, device and system for communicating to a peer via a network. A segment is received formatted according to a first network protocol, the received segment having clear-text payload data in a payload portion of the received segment. A cryptographic operation is performed on at least a portion of the clear-text payload data of the received segment, according to a cryptographic protocol, and a PDU is embedded according to the cryptographic protocol into the payload portion of the received segment. Header data, in a header portion of the received segment, is to account for a change to the received segment resulting from the cryptographic operation performance. The received segment, having the embedded PDU according to the cryptographic protocol and the adjusted header data, is transmitted to a peer via the network

EXHIBIT E

TRADE SECRETS

1. A METHOD TO IMPLEMENT THE PIPELINED FULL DUPLEX PROCESSING
   OF TCP PROTOCOL MESSAGES

   INVENTOR: ASGEIR EIRIKSSON, CHELSIO COMMUNICATIONS
   INC

2. A METHOD TO INTEGRATE THE PROCESSING OF CONTROL
   PLANE MESSAGES AND PIO OPERATIONS WITH THE PIPELINED
   FULL DUPLEX PROCESSING OF TCP PROTOCOL MESSAGES

   INVENTORS: ASGEIR EIRIKSSON, CHELSIO COMMUNICATIONS
   INC

3. A METHOD TO INTEGRATE THE PROCESSING OF TCP TIMERS
   WITH THE PIPELINED FULL DUPLEX PROCESSING OF TCP
   PROTOCOL MESSAGES

   INVENTORS: ASGEIR EIRIKSSON, CHELSIO COMMUNICATIONS
   INC

4. A METHOD TO COORDINATE THE PIPELINED FULL DUPLEX
   PROCESSING OF TCP PROTOCOL MESSAGES, AND TCP PAYLOAD
   INFORMATION

   INVENTORS: ASGEIR EIRIKSSON, CHELSIO COMMUNICATIONS
   INC

5. A METHOD TO COORDINATE THE PIPELINED FULL DUPLEX
   PROCESSING OF TCP PROTOCOL MESSAGES, AND THE
   PROCESSING OF L5-L7 USER LEVEL PROTOCOLS

   INVENTORS: ASGEIR EIRIKSSON, CHELSIO COMMUNICATIONS
   INC

6. A METHOD TO IMPLEMENT THE PIPELINED FULL DUPLEX
   PROCESSING OF TCP PROTOCOL PAYLOAD INFORMATION

   INVENTORS: ASGEIR EIRIKSSON, CHELSIO COMMUNICATIONS
   INC

7. A METHOD TO IMPLEMENT THE DELAYED ACKNOWLEDGE TCP
   PROTOCOL TIMERS USING ON- CHIP AND OFF-CHIP RAM
   MEMORY

   INVENTORS: ASGEIR EIRIKSSON, CHRIS MAO, CHELSIO
   COMMUNICATIONS INC

8. A METHOD TO IMPLEMENT THE VARIOUS TIMEOUT AND KEEP-ALIVE
   TCP PROTOCOL TIMERS USING ON-CHIP AND OFF-CHIP RAM MEMORY

   INVENTORS: ASGEIR EIRIKSSON, CHELSIO COMMUNICATIONS
   INC

9. A METHOD TO IMPLEMENT THE TCP PROTOCOL EGRESS FLOW
   CONTROL AND MEMORY MANAGER USING OFF- CHIP RAM
   MEMORY

   INVENTORS: ASGEIR EIRIKSSON, CHELSIO COMMUNICATIONS
   INC

10. A METHOD TO IMPLEMENT THE TCP PROTOCOL INGRESS FLOW
    CONTROL AND MEMORY MANAGER USING OFF-CHIP RAM
    MEMORY

    INVENTORS: ASGEIR EIRIKSSON, CHELSIO COMMUNICATIONS
    INC

11. A METHOD TO IMPLEMENT THE TCP PROTOCOL RECEIVE
    REORDER BUFFER USING OFF-CHIP RAM MEMORY

    INVENTORS: ASGEIR EIRIKSSON, CHELSIO COMMUNICATIONS
    INC

12. A METHOD TO IMPLEMENT TCP INGRESS COALESCING USING OFF-CHIP RAM MEMORY

INVENTORS: ASGEIR EIRIKSSON, CHELSIO COMMUNICATIONS INC

13. A METHOD TO ALIGN TCP EMBEDDED PROTOCOL DATA UNITS ON PROTOCOL DATA UNIT BOUNDARIES

INVENTOR: ASGEIR EIRIKSSON, CHELSIO COMMUNICATIONS INC.

14. A METHOD TO IMPLEMENT TCP SEQUENCE NUMBER COMPARISON LOGIC WITHOUT REQUIRING THE USE OF ADDER LOGIC

INVENTORS: ASGEIR EIRIKSSON, AND BALEKUDRU KRISHNA, CHELSIO COMMUNICATIONS INC