TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

ETAS ID: TM551785

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
Silicon Valley Bank		06/20/2019	Corporation: CALIFORNIA

RECEIVING PARTY DATA

Name:	Esilicon Corporation
Street Address:	2130 Gold Street, Suite 100
City:	San Jose
State/Country:	CALIFORNIA
Postal Code:	95002
Entity Type:	Corporation: DELAWARE

PROPERTY NUMBERS Total: 3

Property Type	Number	Word Mark
Registration Number:	3591594	ESILICON
Registration Number:	2969847	ESILICON
Registration Number:	3412021	ESILICON

CH $90.00 3591594

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 8015339800
Email: lwilliams@fenwick.com, trademarks@fenwick.com, cellerbach@fenwick.com
Correspondent Name: Connie Ellerbach
Address Line 1: 801 California Street
Address Line 4: Mountain View, CALIFORNIA 94041

ATTORNEY DOCKET NUMBER:	22272-00070-5836
NAME OF SUBMITTER:	Connie Ellerbach
SIGNATURE:	/cle1087/
DATE SIGNED:	12/04/2019

Total Attachments: 14
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RELEASE OF SECURITY INTEREST IN INTELLECUAL PROPERTY

This Release of Security Interest in Intellectual Property is made as of June 20, 2019, by SILICON VALLEY BANK ("Lender") in favor of ESILICON COROPRATION, Delaware Corporation ("Grantor") with its principal place of business located at 2130 Gold Street, Suite 100, San Jose, CA 95002.

Recital

WHEREAS Grantor granted to Lender a security interest in the patents and trademarks described on Exhibits A and B attached hereto, and the copyrights described on Exhibit C attached hereto (collectively, the "Intellectual Property") under (i) an Intellectual Property Security Agreement dated as of March 5, 2003 (the "IP Security Agreement #1"), (ii) an Intellectual Property Security Agreement dated as of August 10, 2012 (the "IP Security Agreement #2"), (iii) a Supplement No. 1 to Intellectual Property Security Agreement dates as of September 5, 2017 (the "IP Security Agreement #3"); and (iv) a Supplement No. 2 to Intellectual Property Security Agreement dates as of March 15, 2019 (the "IP Security Agreement #4" and together with the IP Security Agreement #1, the IP Security Agreement #2, and the IP Security Agreement #3, the IP Security Agreements") and recorded with the U.S. Patent and Trademark Office as set forth on Exhibits A and B, and the U.S. Copyright Office as set forth on Exhibit C.

WHEREAS, Grantor has no outstanding Secured Obligations to Lender under the terms of the IP Security Agreements, and Lender agrees to release its security interest in the Intellectual Property.

Agreement

Now, therefore, Lender agrees that it terminates and releases its security interest in the Intellectual Property and reassigns to Grantor, without warranty or recourse, all interest of Lender in the Intellectual Property.

[Signature Page Follows]

LENDER:

SILICON VALLEY BANK

By: _____
Name: Derek Beebe
Title: Director

3003 Tasman Drive
Santa Clara, CA 95054

Exhibit A - Patents

Country	Description	Application Number	Registration Number	Registration/ Application Date
CN (China)	Method and Arrangement for Managing Packet Queues in Switches (ENQUEUER)	CN1244252C C	ZL 01809144.X	3/1/2006
CN (China)	Method and Apparatus for Distribution of Bandwidth in a Switch (WFHBD)	CN1271830C C	ZL 018088535.7	8/23/2006
DE (Germany)	An apparatus for transferring information from a first to a second electronic unit (ANORDNING FOR OVERFORING AV INFORMATION)	69330406.8/ DE69330406T T2	69323703.8	7/4/2001
EG (Egypt)	Method and Apparatus for Distribution of Bandwidth in a Switch (WFHBD)	EG22886 A	353/2001	10/22/2003
EP [European Patent Organization] (Germany, France, Great Britain, Italy)	An apparatus for transferring information from a first to a second electronic unit (ANORDNING FOR OVERFORING AV INFORMATION)	EP0672322	69323703.8	7/4/2001
EP [European Patent Organization] (Germany, France, Great Britain, Italy)	A Variability Aware Asynchronous Scheme based on Two Phase Protocol	EP08848308.1		5/12/2010
IL (Israel)	Method and Arrangement for Managing Packet Queues in Switches (ENQUEUER)		152463	2/1/2008
IL (Israel)	Method and Apparatus for Distribution of Bandwidth in a Switch (WFHBD)	IL152149D D0	152149	4/7/2008
KR (South Korea)	Method and Arrangement for Managing Packet Queues in Switches (ENQUEUER)	739567	2002-7014308	7/9/2007

PCT	A Variability-Aware Asynchronous Scheme for High Performance Delay Matching	PCT/US08/82870		11/06/2008
PCT	A Variability-Aware Scheme for Asynchronous Circuit Initialization	PCT/US08/82870		11/06/2008
PCT	A Variability-Aware Scheme for High-Performance Asynchronous Circuit	PCT/US08/82887		11/06/2008
SG (Singapore)	Method and Apparatus for Distribution of Bandwidth in a Switch (WFHBD)	82219 (WO0178420)	200208049-9	6/30/2005
TW (Taiwan)	Method and Arrangement for Managing Packet Queues in Switches (ENQUEUER)	182378	90110138 TWI284617	4/6/2004
US	Adaptive Real-Time Work-in-Progress Tracking, Prediction, and Optimization System for a Semiconductor Supply Chain	US6746287	09/912028	6/8/2004
US	Prediction Based Optimization of a Semiconductor Supply Chain Using an Adaptive Real Time Work-in-Progress Tracking System	US7218980	09/912030	5/15/2007
US	System and Method for Automating Integration of Semiconductor Work In Process Updates	US7474933	10/619738	7/14/2003
US	System and Method for Automating Integration of Semiconductor Work In Process Updates	US7474933	10/619738	Recorded 12/31/2008 Issued 01/06/2009
US	Mask Arrangement for Scalable Cam/Ram Structures (CAM/RAM MED INTEGRERAD MASK)	US6134135	09/490827	10/17/2000
US	Cam/Ram Memory Device with a Scalable Structure (WORD LINE BLOCK)	US6330177	09/574364	12/11/2001
US	Apparatus and Method for Self-Synchronization of Data to a Local Clock	US6804203	09/394376	8/5/2003
US	Multicasting Method and Arrangement (MULTICASTING)	US6625151	09/420909	9/23/2003

US	Queue Management System Performing One Read One Write During One Cycle By Using Free Queues (KOHANTERING)	US6754742	09/428288	6/22/2004
US	Scheduler Method and Device in a Switch (IDWRR SCHEDULER)	US6944171	09/804691	9/13/2005
US	Method and Arrangement for Managing Packet Queues in Switches (ENQUEUER)	US6977940	09/560106	12/20/2005
US	Device for Datastream Decoding (TINTIN)	US7158529	11/255759	1/2/2007
US	Method and Apparatus for Distribution of Bandwidth in a Switch (WFHBD)	US7215678	09/991030	5/8/2007
US	Variability Aware Scheme for High Performance Asynchronous Circuit Voltage Regulation		12/265585	Filed 11/5/2008
US	Crossbar switch with grouped inputs and outputs	US7603509	12/069037	10/13/2009
US	Pushed Rule BitCell with New Functionality		12/592472	Filed 11/24/2009
US	An Aynchronous Scheme for Clock Domain Crossing		12/711909	Filed 2/24/2010
US	A Variability-Aware Scheme for Asynchronous Circuit Initialization	US7701255	12/286571	4/20/2010
US	System and Method for Automating Integration of Semiconductor Work In Process Updates	US7756598	12/349651	7/13/2010
US	Network of Tightly Coupled Performance Monitors for Determining th eFrequency of Operation of a Semiconductor IC		13/181362	Filed 7/12/2011
ZA (South Africa)	Method and Arrangement for Managing Packet Queues in Switches (ENQUEUER)	ZA200208610 A	2002/8608	12/31/2003
ZA (South Africa)	Method and Apparatus for Distribution of Bandwidth in a Switch (WFHBD)	ZA200208608 A	2002/8610	12/31/2003

Lender's security interest recorded at the U.S. Patent and Trademark Office on August 14, 2012 at Reel Number 028782 and Frame Number 0322.

Patents continued:

Description	Registration/ Application Number	Registratic Applicatic Date
Duo content addressable memory (CAM) using a single CAM	9,711,220	07/18/17
Error detection and correction in binary content addressable memory (BCAM)	9,529,669	12/27/16
Parallel signal via structure	9,461,000	10/04/16
Scaling of integrated circuit design including high-level logic components	9,460,257	10/04/16
Integrated circuit design scaling for recommending design point	9,460,256	10/04/16
Scaling of integrated circuit design including logic and memory components	9,460,255	10/04/16
Scaling logic components of integrated circuit design	9,460,254	10/04/16
Integrated circuit design optimization	9,454,636	09/27/16
Scaling memory components of integrated circuit design	9,454,628	09/27/16
Testing of thru-silicon vias	9,435,846	09/16/16
Mixed-sized pillars that are probeable and routable	9,263,409	02/16/16
Variability-aware scheme for high-performance asynchronous circuit voltage regulation	8,572,539	10/29/13
Asynchronous scheme for clock domain crossing	8,433,875	04/30/13
Method and apparatus for distribution of bandwidth in a switch	7,215,678	05/8/07
Method and flow control in a switch and a switch controlled thereby	7,061,868	06/13/06
Apparatus and method for converting data in serial format to parallel format and vice versa	7,016,346	03/21/06
Device for datastream decoding	7,158,529	01/02/07
Device for datastream decoding	7,002,983	02/21/06
Method and arrangement for managing packet queues in switches	6,977,940	12/20/05
Scheduler method and device in a switch	6,944,171	09/13/05
Queue management system performing one read one write during one cycle by using free queues	6,754,742	06/22/04
Multicasting method and arrangement	6,625,151	09/23/03
Apparatus and method for self-synchronization of data to a local clock	6,604,203	08/05/03
Method and apparatus for content addressable	6,477,071	11/05/02

memory with a partitioned match line		
CAM/RAM memory device with a scalable structure	6,330,177	12/11/01
Wireless probes	14/963,076	12/08/15
Elongated pad structure	14/963,081	12/08/15
Communication interface architecture using serializer/deserializer	14/810,261	07/27/15
Scaling of integrated circuit design including high-level logic components	15/250,885	08/26/16
Memory optimization in VLSI design using generic memory models	14/628,105	02/20/15
Generating specific memory models using generic memory models for design memories in VLSI	14/628,668	02/23/15
Designing memories in VLSI design using specific memory models generated from generic memory	14/628,676	02/23/15
Error detection and correction in ternary content addressable memory (TCAM)	14/502,954	09/30/14

Lender's security interest recorded at the U.S. Patent and Trademark Office on September 22, 2017 at Reel Number 043669 and Frame Number 0832.

Patents continued:

Description	Registration/ Application Number	Registration/ Application Date
DUO CONTENT ADDRESSABLE MEMORY (CAM) USING A SINGLE CAM	10032516	July 24, 2018
Wireless Probes	10018670	July 10, 2018
Elongated Pad Structure	10050003	August 14, 2018
Communication Interface Architecture Using Serializer/Deserializer	9984997	May 29, 2018
Analog Baseline Wander Compensation for ADC based Serdes	16/270,512	February 7, 2019
Tuning Range for Voltage Controlled Oscillators	16/273,047	February 6, 2019
Successive Approximation Register (SAR) Analog to Digital Converter (ADC) with Partial Loop-Unrolling	16/239,421	January 3, 2019
Inductor Design for Electromagnetic Coupling Reduction	16/229,823	December 21, 2018
Bandgap Circuits with Voltage Calibration	16/222,929	January 14, 2019
Trans-impedance Amplifier (TIA) with a T-coil Feedback Loop	16/298,945	March 11, 2019

Lender's security interest recorded at the U.S. Patent and Trademark Office on March 15, 2019 at Reel Number 048616 and Frame Number 0009.

Exhibit B - Trademarks

TRADEMARK DESCRIPTION	COUNTRY	SERIAL NO.	REG. NO	STATUS
ESILICON	U.S.A.	78-177,028		PENDING

Lender's security interest recorded at the U.S. Patent and Trademark Office on March 18, 2003 at Reel Number 2696 and Frame Number 0870.

Trademarks continued:

Description	Registration Number	Application Number	Registration/ Application Date
ESILICON		(PRC) 6,740,909	5/23/2008
ESILICON	(EU) 006,493,258		5/27/2008
ESILICON	(HK) 301,009,737		12/6/2007
ESILICON	(Israel) 206,419		12/6/2007
ESILICON	(Japan) 5,262,675	2007/122035	9/4/2009
ESILICON		(Taiwan) 97,000,320	1/3/2008
ESILICON	(US) 2,869,847	78/256197	7/19/2005
ESILICON (Child)	(US) 3,412,021	78/678628	4/15/2008
ESILICON (Chinese Characters)		(PRC) 6,740,930	5/23/2008
ESILICON (Chinese Characters)	(PRC) 301,135,340		6/10/2008
ESILICON (Parent)	(US) 3,591,594	78/177028	3/17/2009
ESILICON ACCESS	(US) 3,603,342		4/7/2009
SWITCHCORE & DESIGN	(US) 2867715	78/2[illegible]	
XPEDIUM	(US) 2867715	78/2[illegible]	8/21/2004
XPEDIUM2	(US) 2964234	78/423509	6/28/2005
XPEDIUM3	(US) 2965270	78/423511	7/5/2005
SWITCHCORE	(Madrid) 715327		1999-04-19
SWITCHCORE	(Singapore) T99/03667E		1999-04-20
SWITCHCORE	(Ireland) 219766	99/1316	1999-04-20
SWITCHCORE	(Sweden) 340834	99-00498	2000-09-29
SWITCHCORE, SWITCHCORE LOGO	(Japan) 4439010	11-34678	2000-12-08

SWITCHCORE, SWITCHCORE LOGO	(South Korea) 475815	99-12820	2000-06-22
SWITCHCORE, SWITCHCORE LOGO	(Sweden) 340843	99-02988	2000-09-29
SWITCHCORE	(Taiwan) 064485	88017778	2001-08-16
SWITCHCORE	(Hong Kong) 2000B14824	99/04820	2000-11-03

Lender's security interest recorded at the U.S. Patent and Trademark Office on August 14, 2012 at Reel Number 4841 and Frame Number 0896.

Trademarks continued:

Description	Registration/ Application Number	Registration/ Application Date
NEUASIC	87950807	June 6, 2018

Lender's security interest recorded at the U.S. Patent and Trademark Office on March 15, 2019 at Reel Number 6592 and Frame Number 0816.

Exhibit C – Copyrights

Description	Registration Number	Registration Date
Component Auto-generator System for Test Chip: End-User Manual, Version 1.0	TX0007537285	06/05/2012

Lender's security interest recorded at the U.S. Copyright Office on August 16, 2012 at Volume Number 3608 and Document Number 517.