TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

ETAS ID: TM562092

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
Avalanche Technology, Inc.		02/12/2020	Corporation: DELAWARE

RECEIVING PARTY DATA

Name:	Structured Alpha LP
Street Address:	65 Queen Street West
Internal Address:	Suite 2400
City:	TORONTO, ONTARIO
State/Country:	CANADA
Postal Code:	M5H 2M8
Entity Type:	Limited Partnership: CAYMAN ISLANDS

PROPERTY NUMBERS Total: 4

Property Type	Number	Word Mark
Registration Number:	4198751	AVALANCHE TECHNOLOGY
Registration Number:	4237990	AVALANCHE
Registration Number:	4946647	AVA
Serial Number:	88196128	A

OP $115.00 4198751

CORRESPONDENCE DATA

Fax Number: 2123553333

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 2128138800
Email: NY-TM-Admin@goodwinprocter.com
Correspondent Name: GOODWIN PROCTER LLP/Janis Nici
Address Line 1: 620 Eighth Avenue
Address Line 4: New York, NEW YORK 10018

NAME OF SUBMITTER:	Janis Nici
SIGNATURE:	/janis nici/
DATE SIGNED:	02/13/2020

Total Attachments: 23
source=Avalanche IPSA#page1.tif

source=Avalanche IPSA#page2.tif
source=Avalanche IPSA#page3.tif
source=Avalanche IPSA#page4.tif
source=Avalanche IPSA#page5.tif
source=Avalanche IPSA#page6.tif
source=Avalanche IPSA#page7.tif
source=Avalanche IPSA#page8.tif
source=Avalanche IPSA#page9.tif
source=Avalanche IPSA#page10.tif
source=Avalanche IPSA#page11.tif
source=Avalanche IPSA#page12.tif
source=Avalanche IPSA#page13.tif
source=Avalanche IPSA#page14.tif
source=Avalanche IPSA#page15.tif
source=Avalanche IPSA#page16.tif
source=Avalanche IPSA#page17.tif
source=Avalanche IPSA#page18.tif
source=Avalanche IPSA#page19.tif
source=Avalanche IPSA#page20.tif
source=Avalanche IPSA#page21.tif
source=Avalanche IPSA#page22.tif
source=Avalanche IPSA#page23.tif

SECOND AMENDED AND RESTATED
INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Second Amended and Restated Intellectual Property Security Agreement ("Agreement") is entered into as of the February 12, 2020 by and between STRUCTURED ALPHA LP ("Secured Party") and AVALANCHE TECHNOLOGY, INC. ("Grantor").

RECITALS

A. Secured Party and Grantor are parties to that certain Amended and Restated Note and Warrant Purchase Agreement dated as of February 4, 2019 as amended by that certain Omnibus Amendment to Transaction Documents dated as of February 12, 2020, between Secured Party and Grantor (as may be further amended, restated, supplemented, or otherwise modified from time to time, the "Purchase Agreement"; capitalized terms used herein are used as defined in the Purchase Agreement or the Security Agreement (as defined in the Purchase Agreement), as applicable) pursuant to which Secured Party purchased the Note.

B. Pursuant to the terms of the Security Agreement, Grantor has granted to Secured Party a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

C. In connection with the Purchase Agreement and the Security Agreement, Secured Party and Grantor entered into that certain Amended and Restated Intellectual Property Security Agreement dated as of February 4, 2019 (the "Amended and Restated IPSA") which amended and restated the Intellectual Property Security Agreement dated April 13, 2017 by and between Grantor and Secured Party.

D. Secured Party and Grantor desire to amend and restate the Amended and Restated IPSA to update the Exhibits thereto.

E. This Agreement hereby amends, restates and consolidates in their entirety, without novation, the IPSA and Amended and Restated IPSA. This Agreement is not a novation. All security interests granted under the IPSA and Amended and Restated IPSA are hereby confirmed and ratified and shall continue to secure all obligations under the Purchase Agreement and the Note.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its Obligations under the Purchase Agreement and the Note, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

1. Grant of Security Interest. To secure its obligations under the Purchase Agreement, including, without limitation, the Obligations, Grantor grants and pledges to Secured Party a security interest in all of Grantor's right, title and interest in, to and under its intellectual property (all of which shall collectively be called the "Intellectual Property Collateral"), including, without limitation, the following:

(a) Any and all copyright rights, copyright applications, copyright registrations and like protections in each work or authorship and derivative work thereof, whether published or unpublished and whether or not the same also constitutes a trade secret, now or hereafter existing, created, acquired or

TRADEMARK
REEL: 006864 FRAME: 0112

held, including without limitation those set forth on Exhibit A attached hereto (collectively, the "Copyrights");

(b) Any and all trade secrets, and any and all intellectual property rights in computer software and computer software products now or hereafter existing, created, acquired or held;

(c) Any and all design rights that may be available to Grantor now or hereafter existing, created, acquired or held;

(d) All patents, patent applications and like protections including, without limitation, improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the same, including without limitation the patents and patent applications set forth on Exhibit B attached hereto (collectively, the "Patents");

(e) Any trademark and servicemark rights, whether registered or not, applications to register and registrations of the same and like protections, and the entire goodwill of the business of Grantor connected with and symbolized by such trademarks, including without limitation those set forth on Exhibit C attached hereto, but excluding any intent-to-use trademarks at all times prior to the first use thereof, whether by the actual use thereof in commerce, the recording of a statement of use with the United States Patent and Trademark Office or otherwise (collectively, the "Trademarks");

(f) All mask works or similar rights available for the protection of semiconductor chips, now owned or hereafter acquired, including, without limitation those set forth on Exhibit D attached hereto (collectively, the "Mask Works");

(g) Any and all claims for damages by way of past, present and future infringements of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above;

(h) All licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works (other than licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works granted in the ordinary course of Grantor's business);

(i) All license fees and royalties arising from the use of any of the Copyrights, Patents, Trademarks, or Mask Works to the extent permitted by such license or rights;

(j) All amendments, extensions, renewals and extensions of any of the Copyrights, Trademarks, Patents, or Mask Works; and

(k) All proceeds and products of the foregoing, including without limitation all payments under insurance or any indemnity or warranty payable in respect of any of the foregoing.

2. Recordation. Grantor authorizes the Commissioner for Patents, the Commissioner for Trademarks and the Register of Copyrights and any other government officials to record and register this Agreement with the United States Patent and Trademark Office, the United States Copyright Office or any other governmental agency or office providing for the registering or perfection of security interests in any Intellectual Property Collateral, as applicable, upon request by Secured Party.

3. Authorization. Grantor hereby authorizes Secured Party to (a) modify this Agreement unilaterally by amending the exhibits to this Agreement to include any Intellectual Property Collateral

which Grantor obtains subsequent to the date of this Agreement, and (b) file a duplicate original of this Agreement containing amended exhibits reflecting such new Intellectual Property Collateral.

4. Transaction Documents. This Agreement has been entered into pursuant to and in conjunction with the Purchase Agreement and the Security Agreement, which are hereby incorporated by reference. The provisions of the Purchase Agreement and the Security Agreement shall supersede and control over any conflicting or inconsistent provision herein. The rights and remedies of Security Party with respect to the Intellectual Property Collateral are as provided by the Purchase Agreement, the Security Agreement and related documents, and nothing in this Agreement shall be deemed to limit such rights and remedies.

5. Execution in Counterparts. This Agreement may be executed in counterparts (and by different parties hereto in different counterparts), each of which shall constitute an original, but all of which when taken together shall constitute a single contract. Delivery of an executed counterpart of a signature page to this Agreement by facsimile or in electronic (i.e., "pdf" or "tif" format) shall be effective as delivery of a manually executed counterpart of this Agreement. The words "execution," "signed," "signature" and words of like import herein shall be deemed to include electronic signatures or the keeping of records in electronic form, each of which shall be of the same legal effect, validity and enforceability as a manually executed signature or the use of a paper-based recordkeeping systems, as the case may be, to the extent and as provided for in any applicable law, including, without limitation, any state law based on the Uniform Electronic Transactions Act.

6. Successors and Assigns. This Agreement will be binding on and shall inure to the benefit of the parties hereto and their respective successors and assigns.

7. Governing Law. This Agreement and any claim, controversy, dispute or cause of action (whether in contract or tort or otherwise) based upon, arising out of or relating to this Agreement and the transactions contemplated hereby and thereby shall be governed by, and construed in accordance with, the laws of the United States and the State of California, without giving effect to any choice or conflict of law provision or rule (whether of the State of California or any other jurisdiction).

8. Reaffirmation, Amendment, and Restatement. The terms, conditions, agreements, covenants, representations and warranties set forth in and relating to the IPSA and the Amended and Restated IPSA (collectively, the "Existing IP Security Agreement") are hereby amended, restated, replaced and superseded in their entirety by the terms, conditions, agreements, covenants, representations and warranties set forth in this Agreement. Effective as of the date hereof, Grantor hereby acknowledges and reaffirms the security interests and liens granted by it under the Existing IP Security Agreement and acknowledges that such security interests and liens are continuing valid and enforceable first priority liens in favor of Secured Party, under the Existing IP Security Agreement, as modified and restated hereby, in order to secure the Obligations. Grantor hereby confirms and agrees that such liens are hereby ratified and confirmed in all respects in favor of Secured Party. This Agreement does not discharge or release the liens or first priority thereof, which shall continue, as modified and restated hereby, without interruption and in full force and effect.

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

AVALANCHE TECHNOLOGY, INC.

By: Robert Netter
Title: CFO

Address: 3450 West Warren Avenue
Fremont, CA 94538

SECURED PARTY:

STRUCTURED ALPHA LP

By: Thomvest Asset Management Inc.,
its General Partner

By: Stefan V. Clulow
Title: Managing Director and Chief Investment Officer

Address: 65 Queen Street West, Suite 2400
Toronto, Ontario M5H 2M8
Canada

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

AVALANCHE TECHNOLOGY, INC.

By: _____
Title: _____

Address: 3450 West Warren Avenue
Fremont, CA 94538

SECURED PARTY:

STRUCTURED ALPHA LP

By: Thomvest Asset Management Inc.,
its General Partner

By: Stefan V. Clulow
Title: Managing Director and Chief Investment Officer

Address: 65 Queen Street West, Suite 2400
Toronto, Ontario M5H 2M8
Canada

EXHIBIT A

Copyrights

Description	Registration/ Application Number	Registration/ Application Date
None.		

EXHIBIT B

Patents

Patent Applications

Docket No.	Title	App. No.
AVALANCHE-0178CIP	Magnetic Memory Cell I ncluding Two-Terminal selector device	15/863,825
AVALANCHE-0178US	Selector device Incorporating Conductive Cluster for Memory Application	15/438,631
AVALANCHE-0050DIV	MEMORY SYSTEM HAVING THERMALLY STABLE PERPENDICULAR MAGNETO TUNNEL JUNCTION (MTJ) AND A METHOD OF MANUFACTURING SAME	13/737,897
AVALANCHE-0056C-RE	Prependicalar Magnetic Tunnel Juntion(pMTJ) with in-plan Magneto- Statiac Switching- Enhancing Layer	16/100,649
AVALANCHE-0067CIP-C3	MAGNETIC RANDOM ACCESS MEMORY WITH DYNAMIC RANDOM ACCESS MEMORY (DRAM)-LIKE INTERFACE	16/383,361
AVALANCHE-0092C	method of implementing Magnetic Random access memory (MRAM) for Mobile System -on Chip Boot	15/592,575
AVALANCHE-0131CIP5-C3	Magnetic Random Access Memory with Perpendicular Enhancement Layer	16/112,323
AVALANCHE-0157CIP3-C	Multilayered Seed for Magnetic Structure	16/595,120
AVALANCHE-0173CIP	Selector device Incorporating Conductive Cluster for Memory Application	16/251008
AVALANHCE-0182CIP	Magnetic Memory Emulating Dynamic Randomn Access Memoy (DRAM)	16/550,103
AVALANCHE-0184US	Megnetic memory array incoporating selectors and method for manufucting the same	16/024,601
AVALANHE-0185US	Megnetic Memory and method for using the same	16/176,292
AVALANCHE-0186US	Fast Programming of Magnetic Random Access Memory (MRAM)	16/264,279
AVALANCHE-0187US	Three- Dimesional Nonvolatie Memory	16/446,532
AVALANCHE-0183C	Power-Efficient Programming of Magnetic Memory	16/712,814

TRADEMARK
REEL: 006864 FRAME: 0118

Registered Patents

Patent No.	Docket No.	Title	App. No.
7,732,881	AVALANCHE-0006US	CURRENT-CONFINED EFFECT OF MAGNETIC NANO-CURRENT-CHANNEL (NCC) FOR MAGNETIC RANDOM ACCESS MEMORY (MRAM)	11/932,940
7,869,266	AVALANCHE-0011US	LOW CURRENT SWITCHING MAGNETIC TUNNEL JUNCTION DESIGN FOR MAGNETIC MEMORY USING DOMAIN WALL MOTION	12/255,624
7,981,697	AVALANCHE-0006C	CURRENT-CONFINED EFFECT OF MAGNETIC NANO-CURRENT-CHANNEL (NCC) FOR MAGNETIC RANDOM ACCESS MEMORY (MRAM)	12/791,737
8,018,011	AVALANCHE-0008US	LOW COST MULTI-STATE MAGNETIC MEMORY	11/860,467
8,058,696	AVALANCHE-0002US	A HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY	11/678,515
8,063,459	AVALANCHE-0004US	Non-Volatile Magnetic Memory Element with Graded Layer	11/776,692
8,084,835	AVALANCHE-0001US	Non-Uniform Switching Based Non-Volatile Magnetic Based Memory	11/674,124
8,120,949	AVALANCHE-0015US	A LOW-COST NON-VOLATILE FLASHRAM MEMORY	12/182,996
8,148,174	AVALANCHE-0052US	MAGNETIC TUNNEL JUNCTION (MTJ) FORMATION WITH TWO-STEP PROCESS	13/100,048
8,164,947	AVALANCHE-0011DIV	LOW CURRENT SWITCHING MAGNETIC TUNNEL JUNCTION DESIGN FOR MAGNETIC MEMORY USING DOMAIN WALL MOTION	12/985,028
8,169,821	AVALANCHE-0036US	Low-crystallization temperature MTJ for Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM)	12/907,913
8,183,652	AVALANCHE-0003US	NON-VOLATILE MAGNETIC MEMORY WITH LOW SWITCHING CURRENT AND HIGH THERMAL STABILITY	11/739,648
8,238,145	AVALANCHE-0035US	Shared Transistor in a Spin-Torque Transfer Magnetic Random Access Memory (STTMRAM) Cell	12/756,081
8,289,757	AVALANCHE-0018US	EMBEDDED MAGNETIC RANDOM ACCESS MEMORY (MRAM)	12/778,725
8,295,083	AVALANCHE-0043US	METHOD AND APPARATUS FOR INCREASING THE RELIABILITY OF AN ACCESS TRANSITOR COUPLED TO A MAGNETIC TUNNEL JUNCTION (MTJ)	12/860,793
8,310,020	AVALANCHE-0003DIV2	NON-VOLATILE MAGNETIC MEMORY WITH LOW SWITCHING CURRENT AND HIGH THERMAL STABILITY	13/455,888
8,313,960	AVALANCHE-0052CIP	MAGNETIC TUNNEL JUNCTION (MTJ) FORMATION WITH TWO-STEP PROCESS	13/371,380
8,330,240	AVALANCHE-0008DIV	LOW COST MULTI-STATE MAGNETIC MEMORY	13/213,026
8,363,457	AVALANCHE-0013US	Memory Sensing Circuit	12/125,866

8,363,460	AVALANCHE-0037US	METHOD AND APPARATUS FOR PROGRAMMING A MAGNETIC TUNNEL JUNCTION (MTJ)	12/826,546
8,374,025	AVALANCHE-0031US	A Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) With Laminated Free Layer	12/779,881
8,385,108	AVALANCHE-0075US	DIFFERENTIAL MAGNETIC RANDOM ACCESS MEMORY (MRAM)	13/429,293
8,389,301	AVALANCHE-0001DIV	Non-Uniform Switching Based Non-Volatile Magnetic Based Memory	13/305,668
8,391,054	AVALANCHE-0002DIV	A HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY	13/235,232
8,391,058	AVALANCHE-0015C	A LOW-COST NON-VOLATILE FLASHRAM MEMORY	13/345,600
8,399,942	AVALANCHE-0004C	Non-Volatile Magnetic Memory Element with Graded Layer	13/253,916
8,399,943	AVALANCHE-0004DIV	Non-Volatile Magnetic Memory Element with Graded Layer	13/253,918
8,405,174	AVALANCHE-0003DIV	NON-VOLATILE MAGNETIC MEMORY WITH LOW SWITCHING CURRENT AND HIGH THERMAL STABILITY	13/453,928
8,422,286	AVALANCHE-0036C	Low-crystallization temperature MTJ for Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM)	13/437,908
8,427,863	AVALANCHE-0011C	LOW CURRENT SWITCHING MAGNETIC TUNNEL JUNCTION DESIGN FOR MAGNETIC MEMORY USING DOMAIN WALL MOTION	12/986,802
8,440,471	AVALANCHE-0015DIV	A LOW-COST NON-VOLATILE FLASHRAM MEMORY	13/345,608
8,456,897	AVALANCHE-0008C	LOW COST MULTI-STATE MAGNETIC MEMORY	13/216,997
8,477,529	AVALANCHE-0018DIV	EMBEDDED MAGNETIC RANDOM ACCESS MEMORY (MRAM)	13/623,054
8,477,530	AVALANCHE-0001C	Non-Uniform Switching Based Non-Volatile Magnetic Based Memory	13/305,646
8,488,376	AVALANCHE-0004DIV5	Non-Volatile Magnetic Memory Element with Graded Layer	13/476,879
8,492,860	AVALANCHE-0059US	MAGNETIC LATCH MAGNETIC RANDOM ACCESS MEMORY (MRAM)	13/289,372
8,493,777	AVALANCHE-0003C	NON-VOLATILE MAGNETIC MEMORY WITH LOW SWITCHING CURRENT AND HIGH THERMAL STABILITY	13/453,940
8,493,778	AVALANCHE-0004DIV2	Non-Volatile Magnetic Memory Element with Graded Layer	13/475,489
8,493,779	AVALANCHE-0004DIV3	Non-Volatile Magnetic Memory Element with Graded Layer	13/475,800

8,493,780	AVALANCHE-0004DIV6	Non-Volatile Magnetic Memory Element with Graded Layer	13/476,904
8,498,148	AVALANCHE-0004DIV4	Non-Volatile Magnetic Memory Element with Graded Layer	13/475,814
8,498,149	AVALANCHE-0004DIV7	Non-Volatile Magnetic Memory Element with Graded Layer	13/476,930
8,498,150	AVALANCHE-0004DIV8	Non-Volatile Magnetic Memory Element with Graded Layer	13/476,944
8,508,984	AVALANCHE-0009US	Low resistance high-TMR magnetic tunnel junction and process for fabrication therof	12/040,801
8,519,496	AVALANCHE-0046US	Spin-transfer torque magnetic random access memory with multlayered storage layer	13/035,857
8,526,234	AVALANCHE-0096US	CONTROLLER MANAGEMENT OF MEMORY ARRAY OF STORAGE DEVICE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)	13/708,582
8,535,952	AVALANCHE-0010US	METHOD FOR MANUFACTURING NON-VOLATILE MAGNETIC MEMORY	12/040,827
8,536,063	AVALANCHE-0060	MRAM ETCHING PROCESSES	13/199490
8,542,524	AVALANCHE-0017US	Magnetic Random Access Memory (MRAM) Manufacturing Process for a Small Magnetic Tunnel Junction (MTJ) Design with a Low Programming Current Requirement	12/975,304
8,542,526	AVALANCHE-0017DIV	Magnetic Random Access Memory (MRAM) Manufacturing Process for a Small Magnetic Tunnel Junction (MTJ) Design with a Low Programming Current Requirement	13/763,512
8,547,734	AVALANCHE-0075C	Method of reading logical mass storage device using magnetic random access memory (MRAM)	13/752,192
8,547,745	AVALANCHE-0095US	HOST-MANAGED LOGICAL MASS STORAGE DEVICE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)	13/679,739
8,553,452	AVALANCHE-0072	METHOD FOR MAGNETIC SCREENING OF ARRAYS OF MAGNETIC MEMORIES	13/314,470
8,559,215	AVALANCHE-0069US1	PERPENDICULAR MRAM DEVICE AND ITS INITIALIZATION METHOD	13/360,524
8,565,010	AVALANCHE-0032CIP	MAGNETIC RANDOM ACCESS MEMORY WITH FIELD COMPENSATING LAYER AND MULTI-LEVEL CELL	13/099,321
8,574,928	AVALANCHE-0080	MRAM Fabrication Method with Sidewall Cleaning	13/443818
8,575,584	AVALANCHE-0057	RESISTIVE MEMORY DEVICE HAVING VERTICAL TRANSISTORS AND METHOD FOR MAKING THE SAME	13/225431
8,593,862	AVALANCHE-0029US	SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY HAVING MAGNETIC TUNNEL JUNCTION WITH PERPENDICULAR MAGNETIC ANISOTROPY	12/641,244
8,595,427	AVALANCHE-0101US	NON-VOLATILE BLOCK STORAGE MODULE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)	13/791,452

8,598,576	AVALANCHE-0032US	MAGNETIC RANDOM ACCESS MEMORY WITH FIELD COMPENSATING LAYER AND MULTI-LEVEL CELL	13/029,054
8,611,145	AVALANCHE-0035CIP	Spin-Torque Transfer Magnetic Random Access Memory (STTMRAM) Device with Shared Transistor and Minimal Written Data Disturbance	13/719,142
8,611,147	AVALANCHE-0036DIV	A SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY (STTMRAM) USING A SYNTHETIC FREE LAYER	13/849,062
8,623,452	AVALANCHE-0047US	MAGNETIC RANDOM ACCESS MEMORY (MRAM) WITH ENHANCED MAGNETIC STIFFNESS AND METHOD OF MAKING SAME	12/965,733
8,633,720	AVALANCHE-0053	Method and apparatus fo rmeasuring magnetic parameters of magnetic thin film structures	13/134,925
8,634,234	AVALANCHE-0018DIV3	EMBEDDED MAGNETIC RANDOM ACCESS MEMORY (MRAM)	13/931,614
8,644,060	AVALANCHE-0082US	METHOD OF SENSING DATA OF A MAGNETIC RANDOM ACCESS MEMORIES (MRAM)	13/491,159
8,656,255	AVALANCHE-0108US	Method for reducing Effective Raw Bit Error Rate in Multi-Level Cell NAND Flash Memory	13/840,327
8,670,264	AVALANCHE-0064US	MULTI-PORT MAGNETIC RANDOM ACCESS MEMORY (MRAM)	13/585,774
8,670,276	AVALANCHE-0095C	HOST-MANAGED LOGICAL MASS STORAGE DEVICE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)	13/945,362
8,677,097	AVALANCHE-0087US	PERISTENT BLOCK STORAGE ATTACHED TO MEMORY BUS	13/654,361
8,687,418	AVALANCHE-0026US	Flash Memory With Nano-Pillar Charge Trap	12/623,369
8,693,240	AVALANCHE-0091US	A METHOD AND APPARATUS FOR READING A MAGNETIC TUNNEL JUNCTION USING A SEQUENCE OF SHORT PULSES	13/688,066
8,704,206	AVALANCHE-0074	MEMORY DEVICE INCLUDING TRANSISTOR ARRAY WITH SHARED PLATE CHANNEL AND METHOD FOR MAKING THE SAME	13/356633
8,709,956	AVALANCHE-0058CIP	MRAM with sidewall protection and method of fabrication	13/317564
8,711,613	AVALANCHE-0015C2	NON-VOLATILE FLASH-RAM MEMORY WITH MAGNETIC MEMORY	13/892,077
8,711,631	AVALANCHE-0096C	MANAGEMENT OF MEMORY ARRAY WITH MAGNETIC RANDOM ACCESS MEMORY (MRAM)	13/902,650
8,719,492	AVALANCHE-0101C	NON-VOLATILE BLOCK STORAGE MODULE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)	13/958,207
8,723,281	AVALANCHE-0048US	ACCESS TRANSISTOR WITH A BURIED GATE	13/070,355
8,724,378	AVALANCHE-0035C	Shared Transistor in a Spin-Torque Transfer Magnetic Random Access Memory (STTMRAM) Cell	13/546,408

8,724,379	AVALANCHE-0011C2	A MAGNETIC MEMORY WITH A DOMAIN WALL	13/857,857
8,724,380	AVALANCHE-0125US	METHOD FOR READING AND WRITING MULTI-LEVEL CELLS	14/079,518
8,724,392	AVALANCHE-0096CIP	CONTROLLER MANAGEMENT OF MEMORY ARRAY OF STORAGE DEVICE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)	13/952,435
8,724,413	AVALANCHE-0002C	A HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY	13/235,224
8,730,716	AVALANCHE-0018DIV2	EMBEDDED MAGNETIC RANDOM ACCESS MEMORY (MRAM)	13/931,596
8,751,905	AVALANCHE-0062US	Memory with on-chip error correction	13/351,179
8,755,221	AVALANCHE-0042US	EMULATION OF STATIC RANDOM ACCESS MEMORY (SPAM) BY MAGNETIC RANDOM ACCESS MEMORY (MRAM)	13/187,402
8,758,850	AVALANCHE-0047CIP	SST-MRAM MTJ manufacturing method with in-situ annealing	13/238,972
8,760,914	AVALANCHE-0013DIV	Magnetic memory write circuitry	13/720,327
8,772,886	AVALANCHE-0039	SPIN TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY (STTMRAM) HAVING GRADED SYNTHETIC FREE LAYER	13/099,308
8,772,888	AVALANCHE-0077	MTJ MRAM WITH STUDPATTERNING	13/572,197
8,779,537	AVALANCHE-0039C	SPIN TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY (STTMRAM) HAVING GRADED SYNTHETIC FREE LAYER	14/028,448
8,792,269	AVALANCHE-0076US	Fast Programming of Magnetic Random Access Memory (MRAM)	13/842,747
8,796,795	AVALANCHE-0058US	MRAM WITH SIDEWALL PROTECTION AND METHOD OF FABRICATION	13/136,454
8,802,451	AVALANCHE-0016CIP	METHOD FOR MANUFACTURING HIGH DENSITY NON-VOLATILE MAGNETIC MEMORY	13/610,587
8,803,200	AVALANCHE-0048C	ACCESS TRANSISTOR WITH A BURIED GATE	14/0038,582
8,806,098	AVALANCHE-0114US	MULTI ROOT SHARED PERIPHERAL COMPONENT INTERCONNECT EXPRESS (PCIE) END POINT	13/856,395
8,806,284	AVALANCHE-0081US	Method for Bit-Error Rate Testing of Resistance-based RAM Cells Using a Reflected Signal	13/462,708
8,830,736	AVALANCHE-0069US2	INITIALIZATION METHOD OF A PERPENDICULAR MAGNETIC RANDOM ACCESS MEMORY (MRAM) DEVICE WITH A STABLE REFERENCE CELL	13/360,553
8,830,737	AVALANCHE-0090US	A METHOD AND APPARATUS FOR SENSING THE STATE OF A MAGNETIC TUNNEL JUNCTION (MTJ)	13/716,922

8,836,000	AVALANCHE-0116US	A BOTTOM-TYPE PERPENDICULAR MAGNETIC TUNNEL JUNCTION (pMTJ) ELEMENT WITH THERMALLY STABLE AMORPHOUS BLOCKING LAYERS	13/891,833
8,836,061	AVALANCHE-0086US	Magnetic Tunnel Junction With Non-Metallic Layer Adjacent to Free Layer	13/912,107
8,852,676	AVALANCHE-0047C	MAGNETIC RANDOM ACCESS MEMORY (MRAM) WITH ENHANCED MAGNETIC STIFFNESS AND METHOD OF MAKING SAME	14/052,676
8,860,158	AVALANCHE-0059C	High speed SST-MRAM with orthogonal pinned layer	13/921,481
8,861,260	AVALANCHE-0064C	MULTI-PORT MAGNETIC RANDOM ACCESS MEMORY (MRAM)	14/204,274
8,878,156	AVALANCHE-0085	MEMORY DEVICE HAVING STITCHED ARRAYS OF 4 F2 MEMORY CELLS	13/680,037
8,879,309	AVALANCHE-0035CIP-C	Method and Apparatus for Programming a Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) Array	13/914,396
8,883,520	AVALANCHE-0079	Redeposition Control in MRAM Fabrication Process	13/530381
8,885,395	AVALANCHE-0078	MAGNETORESIST-IVE LOGIC CELL AND METHOD OF USE	13/402123
8,887,013	AVALANCHE-0055US	MAPPING OF RANDOM DEFECTS IN A MEMORY DEVICE	13/175,801
8,890,108	AVALANCHE-0074CIP	MEMORY DEVICE HAVING VERTICAL SELECTION TRANSISTORS WITH SHARED CHANNEL STRUCTURE AND METHOD FOR MAKING THE SAME	13/438845
8,891,291	AVALANCHE-0078CIP	MAGNETORESIST-IVE LOGIC CELL AND METHOD OF USE	13/774801
8,891,292	AVALANCHE-0102US	Magnetoressistive layer structure with voltage-inucted switching and lotic cell application	14//011484
8,891,326	AVALANCHE-0120US	METHOD OF SENSING DATA IN MAGNETIC RANDOM ACCESS MEMORY WITH OVERLAP OF HIGH AND LOW RESISTANCE DISTRIBUTIONS	14/024,580
8,909,855	AVALANCHE-0066CIP2	Storage System Employing MRAM and Physically Addressed Solid State Disk	13/769,710
8,917,543	AVALANCHE-0028C	A MULTI-STATE SPIN-TORQUE TRANSFER MAGNETIC RANDOM ACCESS MEMORY	13/893,311
8,917,546	AVALANCHE-0043C	METHOD AND APPARATUS FOR INCREASING THE RELIABILITY OF AN ACCESS TRANSITOR COUPLED TO A MAGNETIC TUNNEL JUNCTION (MTJ)	13/625,586
8,929,146	AVALANCHE-0096CIP-C	CONTROLLER MANAGEMENT OF MEMORY ARRAY OF STORAGE DEVICE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)	14/192,444
8,935,599	AVALANCHE-0108C	Method for reducing Effective Raw Bit Error Rate in Multi-Level Cell NAND Flash Memory	14/180,286
8,942,032	AVALANCHE-0072C	METHOD FOR MAGNETIC SCREENING OF ARRAYS OF MAGNETIC MEMORIES	13/959413

8,947,919	AVALANCHE-0005C	HIGH CAPACITY LOW COST MULTI-STACKED CROSS-LINE MAGNETIC MEMORY	14/017,255
8,947,922	AVALANCHE-0091C	A METHOD AND APPARATUS FOR READING A MAGNETIC TUNNEL JUNCTION USING A SEQUENCE OF SHORT PULSES	14/245,821
8,947,937	AVALANCHE-0095C2	HOST-MANAGED LOGICAL MASS STORAGE DEVICE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)	14/193,814
8,954,657	AVALANCHE-0122US	STORAGE PROCESSOR MANAGING SOLID STATE DISK ARRAY	14/040,280
8,954,658	AVALANCHE-0133US	Method of LUN management in a sold state disk array	14/090,910
8,954,759	AVALANCHE-0073US	SECURE SPIN TORQUE TRANSFER MAGNETIC RANDOM ACCESS MEMORY (STTMRAM)	13/619,114
8,962,349	AVALANCHE-0124US	METHOD OF MANUFACTURING MAGNETIC TUNNEL JUNCTION MEMORY ELEMENT	14/089,209
8,966,164	AVALANCHE-0129US	STORAGE PROCESSOR MANAGING NVME LOGICALLY ADDRESSED SOLID STATE DISK ARRAY	14/050,274
8,971,100	AVALANCHE-0069CIP	INITIALIZATION METHOD OF A PERPENDICULAR MAGNETIC RANDOM ACCESS MEMORY (MRAM) DEVICE	13/546,169
8,971,107	AVALANCHE-0042DIV	EMULATION OF STATIC RANDOM ACCESS MEMORY (SPAM) BY MAGNETIC RANDOM ACCESS MEMORY (MRAM)	14/281,873
8,975,088	AVALANCHE-0060DIV1	MRAM ETCHING PROCESSES	13/954,673
8,975,089	AVALANCHE-0142US	METHOD FOR FORMING MTJ MEMORY ELEMENT	14/082,400
8,980,649	AVALANCHE-0010C	METHOD FOR MANUFACTURING NON-VOLATILE MAGNETIC MEMORY	14/028,216
8,981,506	AVALANCHE-0059CIP	MAGNETIC RANDOM ACCESS MEMORY WITH SWITCHABLE SWITCHING ASSIST LAYER	13/921,549
8,982,616	AVALANCHE-0031C	Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) with Perpendicular Laminated Free layer	13/685,650
8,996,888	AVALANCHE-0073CIP	Mobile device using secure spin torque transfer magnetic random access memory (SSTMRAM)	13/630,731
9,009,396	AVALANCHE-0066CIP3	PHYSICALLY ADDRESSED SOLID STATE DISK EMPLOYING FLASH AND MAGNETIC RANDOM ACCESS MEMORY (MRAM)	13/745,686
9,009,397	AVALANCHE-0132US	STORAGE PROCESSOR MANAGING SOLID STATE DISK ARRAY	14/073,669
9,013,045	AVALANCHE-0058CIP_Div1	MRAM with sidewall protection and method of fabrication	14/242562
9,019,758	AVALANCHE-0045	SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR MAGNETIC ANISOTROPY MULTILAYERS	13/225,338

9,024,398	AVALANCHE-0130US	PERPENDICULAR STTMRAM DEVICE WITH BALANCED REFERENCE LAYER	14/026,163
9,025,371	AVALANCHE-0031C2	A Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) with Perpendicular Laminated Free layer	14/611,125
9,028,910	AVALANCHE-0047CIP5	MTJ MANUFACTURING METHOD UTILIZING IN-SITU ANNEALING AND ETCH BACK	14/273,436
9,029,822	AVALANCHE-0085CIP	HIGH DENSITY RESISTIVE MEMORY HAVING A VERTICAL DUAL CHANNEL TRANSISTOR	13/843,644
9,029,824	AVALANCHE-0085C	Memroy deive having stitiched arrays of 4 F.sup.2 memory cells	14/449,044
9,030,866	AVALANCHE-0069CIP-C	INITIALIZATION METHOD OF A PERPENDICULAR MAGNETIC RANDOM ACCESS MEMORY (MRAM) DEVICE	14/595,059
9,037,786	AVALANCHE-0107US	STORAGE SYSTEM EMPLOYING MRAM AND ARRAY OF SOLID STATE DISKS WITH INTEGRATED SWITCH	13/970,536
9,037,787	AVALANCHE-0066CIP2-C	A COMPUTER SYSTEM WITH PHYSICALLY-ADDRESSABLE SOLID STATE DISK (SSD) AND A METHOD OF ADDRESSING THE SAME	14/542,516
9,047,968	AVALANCHE-0002C2	A HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY	14/212,970
9,054,298	AVALANCHE-0047CIP3	MAGNETIC RANDOM ACCESS MEMORY (MRAM) WITH ENHANCED MAGNETIC STIFFNESS AND METHOD OF MAKING SAME	13/439,817
9,058,257	AVALANCHE-0087C	PERISTENT BLOCK STORAGE ATTACHED TO MEMORY BUS	14/213,575
9,070,458	AVALANCHE-0037C	METHOD AND APPARATUS FOR PROGRAMMING A MAGNETIC TUNNEL JUNCTION (MTJ)	13/481,097
9,070,464	AVALANCHE-0047CIP2	MAGNETIC RANDOM ACCESS MEMORY (MRAM) WITH ENHANCED MAGNETIC STIFFNESS AND METHOD OF MAKING SAME	13/341,826
9,070,692	AVALANCHE-0089	SHIELDS FOR MAGNETIC MEMORY CHIP PACKAGES	13/740180
9,070,855	AVALANCHE-0131US	MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER	14/053,231
9,070,869	AVALANCHE-0100	FABRICATION METHOD USING THINNER HARD MASK FOR HIGH-DENSITY MRAM	14/051327
9,081,669	AVALANCHE-0015CIP	A HYBRID NON-VOLATILE MEMORY DEVICE	14/264,010
9,082,695	AVALANCHE-0049	VIALESS MEMORY STRUCTURE AND MEHTOD OF MANUFACTURING SAME	13/154,346
9,082,951	AVALANCHE-0131CIP4	MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR ENHANCEMENT LAYER	14/560,740
9,083,382	AVALANCHE-0062C	MEMORY WITH ON-CHIP ERROR CORRECTION	14/281,843

9,087,562	AVALANCHE-0101C2	NON-VOLATILE BLOCK STORAGE MODULE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)	14/270,248
9,105,343	AVALANCHE-0125CIP	MULTI-LEVEL CELLS AND METHOD FOR USING THE SAME	14/229,647
9,112,051	AVALANCHE-0160US	THREE-DIMENSIONAL FLASH MEMORY DEVICE	14/451,252
9,117,532	AVALANCHE-0151US	APPARATUS FOR INITIALIZING PERPENDICULAR MRAM DEVICE	14/219,990
9,123,575	AVALANCHE-0159US	SEMICONDUCTOR MEMORY DEVICE HAVING INCREASED SEPARATION BETWEEN MEMORY ELEMENTS	14/336,640
9,142,755	AVALANCHE-0069US1-C	PERPENDICULAR MAGNETIC RANDOM ACCESS MEMORY (MRAM) DEVICE WITH A STABLE REFERENCE CELL	13/938,891
9,158,623	AVALANCHE-0108C2	Flash subsystem organized into pairs of upper and lower page location	14/538,659
9,166,143	AVALANCHE-0158US	MAGNETIC RANDOM ACCESS MEMORY WITH MULTIPLE FREE LAYERS	14/304,775
9,166,146	AVALANCHE-0099	ELECTRIC FIELD ASSISTED MRAM AND METHOD FOR USING THE SAME	14/166,813
9,166,154	AVALANCHE-0098	MTJ STACK AND BOTTOM ELECTRODE PATTERNING PROCESS WITH ION BEAM ETCHING USING A SINGLE MASK	14/096016
9,196,332	AVALANCHE-0056US	ERPENDICULAR MAGNETIC TUNNEL JUNCTION (pMTJ) WITH IN-PLANE MAGNETO-STATIC SWITCHING-ENHANCING LAYER	13/161,412
9,209,390	AVALANCHE-0085C2	MEMORY DEVICE HAVING STITCHED ARRAYS OF 4 F^2 MEMORY CELLS	14/685,196
9,213,495	AVALANCHE-0096CIP-C2	CONTROLLER MANAGEMENT OF MEMORY ARRAY OF STORAGE DEVICE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)	14/498,717
9,218,866	AVALANCHE-0007C	High capacity low cost muliti state magnetic memory	13/893,303
9,224,504	AVALANCHE-0055DIV	MAPPING OF RANDOM DEFECTS IN A MEMORY DEVICE	14/497,091
9,229,892	AVALANCHE-0114DIV	A SHARED PERIPHERAL COMPONENT INTERCONNECT EXPRESS (PCIE) END POINT SYSTEM WITH A PCIe SWITCH AND METHOD FOR INITIALIZING THE SAME	14/253,453
9,231,027	AVALANCHE-0131C	MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER AND INTERFACIAL ANISOTROPIC FREE LAYER	14/198,405
9,251,059	AVALANCHE-0110US	Storage System Employing MRAM and Redundant Array of Solid State Disk	13/858,875
9,251,879	AVALANCHE-0069US2-C	INITIALIZATION METHOD OF A PERPENDICULAR MAGNETIC RANDOM ACCESS MEMORY (MRAM) DEVICE WITH A STABLE REFERENCE CELL	14/333,308
9,251,882	AVALANCHE-0067US	MAGNETIC RANDOM ACCESS MEMORY WITH DYNAMIC RANDOM ACCESS MEMORY (DRAM)-LIKE INTERFACE	13/303,947

9,252,187	AVALANCHE-0088US	DEVICES AND METHODS FOR MEASUREMENT OF MAGNETIC CHARACTERISTICS OF MRAM WAFERS USING MAGNETORESISTIVE TEST STRIPS	14/195473
9,305,626	AVALANCHE-0091C2	A METHOD AND APPARATUS FOR READING A MAGNETIC TUNNEL JUNCTION USING A SEQUENCE OF SHORT PULSES	14/599,450
9,306,154	AVALANCHE-0131CIP4-C	MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR ENHANCEMENT LAYER	14/745,785
9,311,232	AVALANCHE-0096C2-TRK1	MANAGEMENT OF MEMORY ARRAY WITH MAGNETIC RANDOM ACCESS MEMORY (MRAM)	14/109,914
9,317,206	AVALANCHE-0095C3	HOST-MANAGED LOGICAL MASS STORAGE DEVICE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)	14/593,896
9,318,179	AVALANCHE-0045C2	SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR MAGNETIC ANISOTROPY MULTILAYERS	14/657,608
9,319,387	AVALANCHE-0073DIV-C	SECURE SPIN TORQUE TRANSFER MAGNETIC RANDOM ACCESS MEMORY (STTMRAM)	14/867,881
9,337,413	AVALANCHE-0007C-DIV	AN IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY	14/927,412
9,337,417	AVALANCHE-0131CIP2	MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR INTERFACIAL ANISOTROPY	14/195,427
9,343,134	AVALANCHE-0043C2	METHOD AND APPARATUS FOR INCREASING THE RELIABILITY OF AN ACCESS TRANSITOR COUPLED TO A MAGNETIC TUNNEL JUNCTION (MTJ)	14/552,447
9,349,427	AVALANCHE-0072CIP	METHOD FOR SCREENING ARRAYS OF MAGNETIC MEMORIES	13/969,250
9,349,941	AVALANCHE-0007C2	SSTRAM element having multiple perpendicular MTJS Coupled in series	14/944,117
9,373,663	AVALANCHE-0121US	LANDING PAD IN PERIPHERAL CIRCUIT FOR MAGNETIC RANDOM ACCESS MEMORY (MRAM)	14/033,374
9,396,781	AVALANCHE-0131CIP	MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER	14/173,145
9,396,783	AVALANCHE-0067C	MAGNETIC RANDOM ACCESS MEMORY WITH DYNAMIC RANDOM ACCESS MEMORY (DRAM)-LIKE INTERFACE	15/009,367
9,401,194	AVALANCHE-0076C	Fast Programming of Magnetic Random Access Memory (MRAM)	14/253,192
9,419,207	AVALANCHE-0157C	MAGNETIC RANDOM ACCESS MEMORY WITH MULTILAYERED SEED STRUCTURE	14/701,955
9,419,210	AVALANCHE-0045C3	SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR MAGNETIC ANISOTROPY MULTILAYERS	15/072,254
9,443,577	AVALANCHE-0153US	VOLTAGE-SWITCHED MAGNETIC RANDOM ACCESS MEMORY (MRAM) AND METHOD FOR USING THE SAME	14/281,673
9,444,038	AVALANCHE-0157C2	MAGNETIC RANDOM ACCESS MEMORY WITH MULTILAYERED SEED STRUCTURE	14/727,642

9,444,039	AVALANCHE-0045C1	SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR MAGNETIC ANISOTROPY MULTILAYERS	14/657,556
9,472,595	AVALANCHE-0166US	Perpendicular MRAM with Magnet	14/667,590
9,478,279	AVALANCHE-0007C3	AN IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY	15/148,694
9,496,489	AVALANCHE-0157US	MAGNETIC RANDOM ACCESS MEMORY WITH MULTILAYERED SEED STRUCTURE	14/687,161
9,502,092	AVALANCHE-0164US	Unipolar-Switching Perpendicular MRAM And Method for Using Same	14/754,419
9,520,174	AVALANCHE-0037C2	METHOD AND APPARATUS FOR PROGRAMMING A MAGNETIC TUNNEL JUNCTION (MTJ)	14/754,635
9,530,479	AVALANCHE-0043C3	Method and Apparatus of increase the reliablity of an Access Transistor Coupled to a Magnetic Tunnel Junction (MTJ)	15/147,084
9,543,506	AVALANCHE-0131CIP4-C2	MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER	15/054,561
9,548,334	AVALANCHE-0131C2	MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER AND THIN REFERENCE LAYER	14/255,884
9,548,448	AVALANCHE-0167US	MEMORY DEVICE WITH INCREASED SEPARATION BETWEEN MEMORY ELEMENTS	14/939,229
9,558,802	AVALANCHE-0076C-DIV	Fast Programming of Magnetic Random Access Memory (MRAM)	15/203,455
9,559,144	AVALANCHE-0131C3	MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER	14/730,117
9,607,676	AVALANCHE-0500	METHOD AND APPARATUS FOR ADJUSTMENT OF CURRENT THROUGH A MAGNETORESISTIVE TUNNEL JUNCTION (MTJ) BASED ON TEMPERATURE FLUCTUATIONS	14/824,982
9,608,038	AVALANCHE-0131CIP-C	MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER AND THIN REFERENCE LAYER	15/174,754
9,627,438	AVALANCHE-0169US	Three Dimensional Memory Arrays and stitching there of	15/141,726
9,634,244	AVALANCHE-0131CIP2-DIV	MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER AND THIN REFERENCE LAYER	15/080,208
9,646,668	AVALANCHE-0035CIP2	Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) With Enhanced Write Current	14/524,848
9,647,032	AVALANCHE-0161US	SPIN-ORBITRONICS DEVICE AND APPLICATIONS THEREOF	14/831,546
9,647,202	AVALANCHE-0131CIP3	MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR ENHANCEMENT LAYER	14/256,192
9,652,386	AVALANCHE-0096C3	MANAGEMENT OF MEMORY ARRAY WITH MAGNETIC RANDOM ACCESS MEMORY (MRAM)	15/094,844

TRADEMARK
REEL: 006864 FRAME: 0129

9,658,780	AVALANCHE-0067CIP	MAGNETIC RANDOM ACCESS MEMORY WITH DYNAMIC RANDOM ACCESS MEMORY (DRAM)-LIKE INTERFACE	15/132,278
9,658,859	AVALANCHE-0092US	METHOD OF IMPLEMENTING MAGNETIC RANDOM ACCESS MEMORY (MRAM) FOR SYSTEM BOOT	14/091,318
9,679,625	AVALANCHE-0056C	PERPENDICULAR MAGNETIC TUNNEL JUNCTION (pMTJ) WITH IN-PLANE MAGNETO-STATIC SWITCHING-ENHANCING LAYER	14/930,523
9,691,464	AVALANCHE-0076CIP	Fast Programming of Magnetic Random Access Memory (MRAM)	15/417,135
9,727,245	AVALANCHE-0128US	A METHOD AND APPARATUS FOR DE-DUPLICATION FOR SOLID STATE DISKs (SSDs)	14/722,038
9,728,240	AVALANCHE-0115US	Pulse programming techniques ofr voltage-controlled magnetroesistive tunnel junction (MTJ)	14/214,064
9,748,471	AVALANCHE-0131CIP-C2	MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR ENHANCEMENT LAYER	15/440,948
9,780,300	AVALANCHE-0131CIP4-C3	MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR ENHANCEMENT LAYER	15/365,371
9,786,344	AVALANCHE-0076CIP-C	Programming of Magnetic Random Access Memory (MRAM) By Boosting gate voltage	15/614,450
9,792,047	AVALANCHE-0122C	STORAGE PROCESSOR MANAGING SOLID STATE DISK ARRAY	14/595,170
9,792,073	AVALANCHE-0133C	A METHOD OF LUN MANAGEMENT IN A SOLID STATE DISK ARRAY	14/617,868
9,793,003	AVALANCHE-0176US	Programming of Non-Volatile Memory Subjected to High Temperature Exposure	15/265,774
9,793,318	AVALANCHE-0121C	LANDING PAD IN PERIPHERAL CIRCUIT FOR MAGNETIC RANDOM ACCESS MEMORY (MRAM)	15/158,872
9,793,319	AVALANCHE-0157C3	Multilayered Seed Structure for Perpendicular MTJ Memory Element	15/295,002
9,812,499	AVALANCHE-0168US	Memory Device Incorporating selector element with mulitple thresholds	15/221,505
9,824,050	AVALANCHE-0114DIV-C	A SHARED PERIPHERAL COMPONENT INTERCONNECT EXPRESS (PCIE) END POINT SYSTEM WITH A PCIe SWITCH AND METHOD FOR INITIALIZING THE SAME	14/948,187
9,830,106	AVALANCHE-0172US	Management of Memory Array with Magnetic Random Access Memory (MRAM)	15/411,913
9,831,421	AVALANCHE-0131CIP5	MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR ENHANCEMENT LAYER	14/797,458
9,858,977	AVALANCHE-0076CIP-C2	Fast Programming of Magnetic Random Access Memory (MRAM)	15/688,746
9,871,190	AVALANCHE-0152US	MAGNETIC RANDOM ACCESS MEMORY WITH ULTRATHIN REFERENCE LAYER	14/263,046
9,871,191	AVALANCHE-0152C	MAGNETIC RANDOM ACCESS MEMORY WITH ULTRATHIN REFERENCE LAYER	14/730,073

9,898,204	AVALANCHE-0067CIP-C	MAGNETIC RANDOM ACCESS MEMORY WITH DYNAMIC RANDOM ACCESS MEMORY (DRAM)-LIKE INTERFACE	15/599,731
9,911,482	AVALANCHE-0500C	METHOD AND APPARATUS FOR ADJUSTMENT OF CURRENT THROUGH A MAGNETORESISTIVE TUNNEL JUNCTION (MTJ) BASED ON TEMPERATURE FLUCTUATIONS	15/434.966
9,921,782	AVALANCHE-0170US	Memory Device for Emulating Dynamic Random Access Memory (DRAM)	15/011,344
10,008,540	AVALANCHE-0161DIV	SPIN-ORBITRONICS DEVICE AND APPLICATIONS THEREOF	15/586,638
10,008,663	AVALANCHE-0180US	Perpendicular Magnetic Fixed layer with high Anisotropy	15/491,220
10,032,979	AVALANCHE-0131CIP5-C2	Magnetic Random Access Memory with Perpenduicluar Enhancement layer	15/816,160
10,037,272	AVALANCHE-0106US	STORAGE SYSTEM EMPLOYING MRAM AND ARRAY OF SOLID STATE DISKS WITH INTEGRATED SWITCH	13/831,921
10,042,758	AVALANCHE-0107C	STORAGE SYSTEM EMPLOYING MRAM AND ARRAY OF SOLID STATE DISKS WITH INTEGRATED SWITCH	14/688,996
10,050,083	AVALANCHE-0157CIP	Magnetic Random Access Memory with Mulitilayered seed structure	15/687,258
10,079,338	AVALANCHE-0131CIP5-C	Megnetic Random Access memory having perpendicluar Enhancement layer	15/794,983
10,090,456	AVALANCHE-0131CIP-C3	Megnetic Random Access memory having perpendicluar Enhancement layer	15/662,114
10,101,924	AVALANCHE-0129C	STORAGE PROCESSOR MANAGING NVME LOGICALLY ADDRESSED SOLID STATE DISK ARRAY	14/629,404
10,108,542	AVALANCHE-0171US	Serial Link Storage Interface (SLSI) Hybrid Block Storage	15/383,899
10,127,960	AVALANCHE-0181US	Transient Sensing of Memory Cells	15/594,387
10,153,017	AVALANCHE-0174US	Method for Sensing Memory Element Coupled to Selector Device	15/264,847
10,177,308	AVALANCHE-0179US	Method for Manufacturing Magntic Memory Cells	15/618,510
10,217,934	AVALANCHE-0179DIV	Method for manufacuring Magnetic Memory Cells	16/112,173
10,224,367	AVALANCHE-0173	Selector device Incorporating Conductive Cluster for Memory Application	15/157,607
10,268,393	AVALANCHE-0067CIP-C2	Magentic random access memory with dynamic random access memory (DRAM)like interface	15/816,887
10,347,691	AVALANCHE-0157CIP2	Megnetic Memory Element with Multilayred seed strucsture	16/101,325

10,361,362	AVALANCHE-0152C2	MAGNETIC RANDOM ACCESS MEMORY WITH ULTRATHIN REFERENCE LAYER	15/815,516
10,395,710	AVALANCHE-0182US	Magnetic Memory Emulting dynamic Random Access Memory (DRAM)	15/985,268
10,438,997	AVALANCHE-0157CIP3	Multilayered Seed for Magnetic Structure	16/287,987
10,490,737	AVALANCHE-0131CIP5-C4	Magnetic Random Access Memory with Perpendicular Enhancement Layer	16/287,974
10,515,681	AVALANCHE-0183US	Power-Efficient Programming of Magnetic Memory	16/002,828
10,522,590	AVALANCHE-0175US	Magnetic Memory Incorporating Dual Selectors	15/921,552

EXHIBIT C

Trademarks

Title or Mark	Country	Application	Filing Date	Trademark Number
AVALANCHE TECHNOLOGY	US	77/555,366	8/25/2008	4,198,751
AVALANCHE	US	77/664,140	2/5/2009	4,237,990
AVA	US	86/120,452	11/15/2013	4,946,647

Avalanche Pending Trademarks

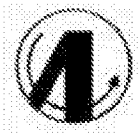
Title or Mark	Country	Application	Filing Date	Trademark Number
	US	88/196,128	11/15/2018	pending

EXHIBIT D

Mask Works

Description	Registration/ Application Number	Registration/ Application Date
None.		