TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

ETAS ID: TM567192

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
ACHRONIX SEMICONDUCTOR CORPORATION		03/16/2020	Corporation: DELAWARE

RECEIVING PARTY DATA

Name:	HERCULES CAPITAL, INC., AS AGENT
Street Address:	400 Hamilton Avenue, Suite 310
City:	Palo Alto
State/Country:	CALIFORNIA
Postal Code:	94301
Entity Type:	Corporation: MARYLAND

PROPERTY NUMBERS Total: 3

Property Type	Number	Word Mark
Registration Number:	3949658	ACHRONIX
Registration Number:	3623430	SPEEDSTER
Serial Number:	88668938	VECTORPATH

OP $90.00 3949658

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 6506483802
Email: PATTY@PATTYCHENG.COM
Correspondent Name: PATTY CHENG
Address Line 1: 2625 MIDDLEFIELD RD., #215
Address Line 4: PALO ALTO, CALIFORNIA 94306

NAME OF SUBMITTER:	Patty Cheng
SIGNATURE:	/s/ Patty Cheng
DATE SIGNED:	03/16/2020

Total Attachments: 8
source=Achronix - IPSA#page1.tif
source=Achronix - IPSA#page2.tif

source=Achronix - IPSA#page3.tif
source=Achronix - IPSA#page4.tif
source=Achronix - IPSA#page5.tif
source=Achronix - IPSA#page6.tif
source=Achronix - IPSA#page7.tif
source=Achronix - IPSA#page8.tif

INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement (as amended, restated, supplemented or otherwise modified from time to time, the "Agreement") is entered into as of March 16, 2020, by and between ACHRONIX SEMICONDUCTOR CORPORATION, a Delaware corporation and ACHRONIX SEMICONDUCTOR INTERNATIONAL CORPORATION, a Delaware corporation (individually, and collectively, "Grantor") and HERCULES CAPITAL, INC., a Maryland corporation, as agent ("Agent").

RECITALS

A. Pursuant to the terms set forth in that certain Loan and Security Agreement dated as of the date hereof and as amended, modified, supplemented or otherwise modified from time to time, by and among the several entities from time to time parties as lenders thereto (collectively, referred to as "Lender"), Agent, Grantor, and any other parties thereto from time to time (the "Loan Agreement"), Lender has agreed to make certain advances of money and to extend certain financial accommodation (the "Loans") to Grantor in the amounts and manner set forth in the Loan Agreement. All capitalized terms used but not defined herein have the meanings given to them in the Loan Agreement.

B. As a condition to the Loan Agreement, Grantor is required to enter into this Agreement to further evidence the grant to Agent of the security interest in its Copyrights, Trademarks and Patents to secure the Secured Obligations.

AGREEMENT

NOW, THEREFORE, Grantor agrees as follows:

1. To secure the Secured Obligations and any other obligations pursuant to the Loan Documents, Grantor grants and pledges to Agent a security interest in all of Grantor's Intellectual Property now or hereafter existing, created, owned, acquired or held (including without limitation those Copyrights, Patents and Trademarks listed on Exhibits A, B and C hereto) and all proceeds and products of the foregoing, including without limitation all payments under insurance or any indemnity or warranty payable in respect of the Intellectual Property.

2. This security interest is granted in conjunction with the security interest granted to Agent under the Loan Agreement. The rights and remedies of Agent with respect to the security interest are as set forth in the Loan Agreement and the other Loan Documents or as are now or hereafter available to Agent as a matter of law or equity, and shall be cumulative and concurrent.

3. Grantor represents and warrants that Exhibits A, B, and C attached hereto set forth any and all Copyrights, Patents and Trademarks in connection with which such Grantor have registered or filed an application with the United States Patent and Trademark Office or the United States Copyright Office, as applicable.

4. Grantor hereby authorizes Agent to (a) modify this Agreement unilaterally by amending the exhibits to this Agreement to include any Intellectual Property which Grantor obtains subsequent to the date of this Agreement, and (b) file a duplicate original of this Agreement containing amended exhibits reflecting such new Intellectual Property.

5. This Agreement has been entered into pursuant to and in conjunction with the Loan Agreement, which is hereby incorporated by reference. The provisions of the Loan Agreement shall supersede and control over any conflicting or inconsistent provision herein.

6. This Agreement may be executed in two or more counterparts, each of which shall be deemed an original but all of which together shall constitute the same instrument. In the event that any signature to this Agreement is delivered by facsimile transmission or by e-mail delivery of a ".pdf" format data file, such signature shall create a valid and binding obligation of the party executing (or on whose behalf such signature is executed) with the same force and effect as if such facsimile or ".pdf" signature page were an original thereof.

[REMAINDER OF PAGE INTENTIONALLY LEFT BLANK]

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed effective as of the date set forth above.

Address of Grantor:

Achronix Semiconductor Corporation Attention: Chief Financial Officer 2903 Bunker Hill Lane, Suite 200 Santa Clara, CA 94054

GRANTOR:

Achronix Semiconductor Corporation

By:_____

Name: Howard S. Brodsky

Title: VP of Business Operations, CFO and Secretary

Achronix Semiconductor International Corporation

By:_____

Name: Howard S. Brodsky

Title: Chief Financial Officer and Secretary

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed effective as of the date set forth above.

Address of Agent:

Legal Department
400 Hamilton Avenue, Suite 310
Palo Alto, CA 94301
Attn: Loan Documentation

AGENT:

HERCULES CAPITAL, INC.

By: _____

Name: Zhuo Huang

Title: Associate General Counsel

EXHIBIT A

Copyrights

Please Check Box if No Copyrights Exist ☑

Registered Owner	Title	Registration Number	Registration Date

EXHIBIT B

Patents

(all owned and registered to Achronix Semiconductor Corporation)

SLW FILE NUMBER	TITLE	COUNTRY	SERIAL NUMBER	FILING DATE	STATUS	ISSUE DATE	PATENT NUMBER
2695.001EP1	SYSTEMS AND METHODS FOR PERFORMING AUTOMATED CONVERSION OF REPRESENTATIONS OF SYNCHRONOUS CIRCUIT DESIGNS TO AND FROM REPRESENTATIONS OF ASYNCHRONOUS CIRCUIT DESIGNS	European Patent Office	077614436	Apr 27, 2007	Issued	Jul 24, 2019	2024884
2695.001HK1	SYSTEMS AND METHODS FOR PERFORMING AUTOMATED CONVERSION OF REPRESENTATIONS OF SYNCHRONOUS CIRCUIT DESIGNS TO AND FROM REPRESENTATIONS OF ASYNCHRONOUS CIRCUIT DESIGNS	Hong Kong	091072262	Apr 27, 2007	Pending		
2695.001JP1	SYSTEMS AND METHODS FOR PERFORMING AUTOMATED CONVERSION OF REPRESENTATIONS OF SYNCHRONOUS CIRCUIT DESIGNS TO AND FROM REPRESENTATIONS OF ASYNCHRONOUS CIRCUIT DESIGNS	Japan	2009507982	Apr 27, 2007	Issued	Jul 27, 2012	5045961
2695.001KR1	SYSTEMS AND METHODS FOR PERFORMING AUTOMATED CONVERSION OF REPRESENTATIONS OF SYNCHRONOUS CIRCUIT DESIGNS TO AND FROM REPRESENTATIONS OF ASYNCHRONOUS CIRCUIT DESIGNS	Republic of Korea	1020087029013	Apr 27, 2007	Issued	Aug 29, 2011	10-1061864
2695.001US1	SYSTEMS AND METHODS FOR PERFORMING AUTOMATED CONVERSION OF REPRESENTATIONS OF SYNCHRONOUS CIRCUIT DESIGNS TO AND FROM REPRESENTATIONS OF ASYNCHRONOUS CIRCUIT DESIGNS	United States of America	11740184	Apr 25, 2007	Issued	Oct 27, 2009	7610567
2695.001US2	AUTOMATED CONVERSION OF SYNCHRONOUS TO ASYNCHRONOUS CIRCUIT DESIGN REPRESENTATIONS	United States of America	12550582	Aug 31, 2009	Issued	May 28, 2013	8453079
2695.002DE1	FAULT TOLERANT ASYNCHRONOUS CIRCUITS	Germany	077614477	Apr 27, 2007	Issued	Nov 8, 2017	602007052969.7
2695.002EP1	FAULT TOLERANT ASYNCHRONOUS CIRCUITS	European Patent Office	077614477	Apr 27, 2007	Issued	Nov 8, 2017	2020085
2695.002FR1	FAULT TOLERANT ASYNCHRONOUS CIRCUITS	France	077614477	Apr 27, 2007	Issued	Nov 8, 2017	2020085
2695.002GB1	FAULT TOLERANT ASYNCHRONOUS CIRCUITS	United Kingdom	077614477	Apr 27, 2007	Issued	Nov 8, 2017	2020085
2695.002HK1	FAULT TOLERANT ASYNCHRONOUS CIRCUITS	Hong Kong	091070371	Apr 27, 2007	Issued	Jul 27, 2018	HK1129778
2695.002JP1	FAULT TOLERANT ASYNCHRONOUS CIRCUITS	Japan	2009507984	Apr 27, 2007	Issued	Dec 21, 2012	5158607
2695.002KR1	FAULT TOLERANT ASYNCHRONOUS CIRCUITS	Republic of Korea	1020087029014	Apr 27, 2007	Issued	Aug 23, 2011	10-1060270
2695.002US1	FAULT TOLERANT ASYNCHRONOUS CIRCUITS	United States of America	11740180	Apr 25, 2007	Issued	Mar 17, 2009	7504851
2695.002US2	FAULT TOLERANT ASYNCHRONOUS CIRCUITS	United States of America	12240430	Sep 29, 2008	Issued	Jun 22, 2010	7741864
2695.002US3	FAULT TOLERANT ASYNCHRONOUS CIRCUITS	United States of America	12768045	Apr 27, 2010	Issued	Jul 17, 2012	8222915
2695.003DE1	RECONFIGURABLE LOGIC FABRICS FOR INTEGRATED CIRCUITS AND SYSTEMS AND METHODS FOR CONFIGURING RECONFIGURABLE LOGIC FABRICS	Germany	078403037	Jun 27, 2007	Issued	Mar 14, 2018	60 2007 054 240.5
2695.003EP1	RECONFIGURABLE LOGIC FABRICS FOR INTEGRATED CIRCUITS AND SYSTEMS AND METHODS FOR CONFIGURING RECONFIGURABLE LOGIC FABRICS	European Patent Office	078403037	Jun 27, 2007	Issued	Mar 14, 2018	2041872
2695.003FR1	RECONFIGURABLE LOGIC FABRICS FOR INTEGRATED CIRCUITS AND SYSTEMS AND METHODS FOR CONFIGURING RECONFIGURABLE LOGIC FABRICS	France	078403037	Jun 27, 2007	Issued	Mar 14, 2018	2041872
2695.003GB1	RECONFIGURABLE LOGIC FABRICS FOR INTEGRATED CIRCUITS AND SYSTEMS AND METHODS FOR CONFIGURING RECONFIGURABLE LOGIC FABRICS	United Kingdom	078403037	Jun 27, 2007	Issued	Mar 14, 2018	2041872
2695.003HK1	RECONFIGURABLE LOGIC FABRICS FOR INTEGRATED CIRCUITS AND SYSTEMS AND METHODS FOR CONFIGURING RECONFIGURABLE LOGIC FABRICS	Hong Kong	091090359	Sep 29, 2009	Issued	Dec 28, 2018	HK1131269
2695.003JP1	RECONFIGURABLE LOGIC FABRICS FOR INTEGRATED CIRCUITS AND SYSTEMS AND METHODS FOR CONFIGURING RECONFIGURABLE LOGIC FABRICS	Japan	2009518547	Jun 27, 2007	Issued	Sep 6, 2013	5354427
2695.003KR1	RECONFIGURABLE LOGIC FABRICS FOR INTEGRATED CIRCUITS AND SYSTEMS AND METHODS FOR CONFIGURING RECONFIGURABLE LOGIC FABRICS	Republic of Korea	1020087031271	Jun 27, 2007	Issued	Aug 16, 2011	10-1058468
2695.003US1	RECONFIGURABLE LOGIC FABRICS FOR INTEGRATED CIRCUITS AND SYSTEMS AND METHODS FOR CONFIGURING RECONFIGURABLE LOGIC FABRICS	United States of America	12304694	Dec 12, 2008	Issued	Feb 1, 2011	7880499
2695.003US2	RECONFIGURABLE LOGIC FABRICS FOR INTEGRATED CIRCUITS AND SYSTEMS AND METHODS FOR CONFIGURING RECONFIGURABLE LOGIC FABRICS	United States of America	13007933	Jan 17, 2011	Issued	Feb 28, 2012	8125242
2695.003US3	RECONFIGURABLE LOGIC FABRICS FOR INTEGRATED CIRCUITS AND SYSTEMS AND METHODS FOR CONFIGURING RECONFIGURABLE LOGIC FABRICS	United States of America	13354117	Jan 19, 2012	Issued	Nov 5, 2013	8575959
2695.003US4	RECONFIGURABLE LOGIC FABRICS FOR INTEGRATED CIRCUITS AND SYSTEMS AND METHODS FOR CONFIGURING RECONFIGURABLE LOGIC FABRICS	United States of America	14071159	Nov 4, 2013	Issued	Feb 3, 2015	8949759
2695.004US1	FAULT TOLERANT ASYNCHRONOUS CIRCUITS	United States of America	11740168	Apr 25, 2007	Issued	Mar 17, 2009	7505304
2695.004US2	FAULT TOLERANT ASYNCHRONOUS CIRCUITS	United States of America	12405746	Mar 17, 2009	Issued	Aug 23, 2011	8004877
2695.007DE1	CONVERSION OF A SYNCHRONOUS FPGA DESIGN INTO AN ASYNCHRONOUS FPGA DESIGN	Germany	078701257	Dec 31, 2007	Issued	Nov 22, 2017	60 2007 053 161.6
2695.007EP1	CONVERSION OF A SYNCHRONOUS FPGA DESIGN INTO AN ASYNCHRONOUS FPGA DESIGN	European Patent Office	078701257	Dec 31, 2007	Issued	Nov 22, 2017	2100242
2695.007FR1	CONVERSION OF A SYNCHRONOUS FPGA DESIGN INTO AN ASYNCHRONOUS FPGA DESIGN	France	078701257	Dec 31, 2007	Issued	Nov 22, 2017	2100242
2695.007GB1	CONVERSION OF A SYNCHRONOUS FPGA DESIGN INTO AN ASYNCHRONOUS FPGA DESIGN	United Kingdom	078701257	Dec 31, 2007	Issued	Nov 22, 2017	2100242
2695.007HK1	CONVERSION OF A SYNCHRONOUS FPGA DESIGN INTO AN ASYNCHRONOUS FPGA DESIGN	Hong Kong	101026667	Mar 15, 2010	Issued	Aug 3, 2018	HK1137829

EXHIBIT B

Patents - continued

(all owned and registered to Achronix Semiconductor Corporation)

SLW FILE NUMBER	TITLE	COUNTRY	SERIAL NUMBER	FILING DATE	STATUS	ISSUE DATE	PATENT NUMBER
2695.007JP1	CONVERSION OF A SYNCHRONOUS FPGA DESIGN INTO AN ASYNCHRONOUS FPGA DESIGN	Japan	2009544906	Dec 31, 2007	Issued	Aug 3, 2012	5055378
2695.007KR1	CONVERSION OF A SYNCHRONOUS FPGA DESIGN INTO AN ASYNCHRONOUS FPGA DESIGN	Republic of Korea	1020097016402	Dec 31, 2007	Issued	Sep 4, 2015	10-1552181
2695.007US1	METHODS AND SYSTEMS FOR CONVERTING A SYNCHRONOUS CIRCUIT FABRIC INTO AN ASYNCHRONOUS DATAFLOW CIRCUIT FABRIC	United States of America	11650238	Jan 5, 2007	Issued	Nov 3, 2009	7614029
2695.007US2	CONVERTING A SYNCHRONOUS CIRCUIT DESIGN INTO AN ASYNCHRONOUS DESIGN	United States of America	12555903	Sep 9, 2009	Issued	Feb 12, 2013	8375339
2695.008TW1	IMPROVING LOGIC PERFORMANCE IN CYCLIC STRUCTURES	Taiwan R.O.C.	098104591	Feb 12, 2009	Issued	Sep 1, 2014	I451280
2695.008US1	LOGIC PERFORMANCE IN CYCLIC STRUCTURES	United States of America	12030531	Feb 13, 2008	Issued	Jan 24, 2012	8104004
2695.012US1	ASYNCHRONOUS PIPELINED INTERCONNECT ARCHITECTURE WITH FANOUT SUPPORT	United States of America	12475744	Jun 1, 2009	Issued	Feb 24, 2015	8964795
2695.012US2	ASYNCHRONOUS PIPELINED INTERCONNECT ARCHITECTURE WITH FANOUT SUPPORT	United States of America	14629192	Feb 23, 2015	Issued	May 17, 2016	9344385
2695.014HK1	SYNCHRONOUS TO ASYNCHRONOUS LOGIC CONVERSION	Hong Kong	111058300	Feb 6, 2009	Pending		
2695.014KR1	SYNCHRONOUS TO ASYNCHRONOUS LOGIC CONVERSION	Republic of Korea	1020107020673	Feb 6, 2009	Issued	Jan 28, 2016	10-1591376
2695.014TW1	SYNCHRONOUS TO ASYNCHRONOUS DESIGN CONVERSION	Taiwan R.O.C.	098104592	Feb 12, 2009	Issued	Feb 11, 2016	I521367
2695.014US1	SYNCHRONOUS TO ASYNCHRONOUS LOGIC CONVERSION	United States of America	12031992	Feb 15, 2008	Issued	Jun 15, 2010	7739628
2695.014US2	SYNCHRONOUS TO ASYNCHRONOUS LOGIC CONVERSION	United States of America	12768129	Apr 27, 2010	Issued	Oct 16, 2012	8291358
2695.015US1	RESET MECHANISM CONVERSION	United States of America	12505653	Jul 20, 2009	Issued	Apr 17, 2012	8161435
2695.015US2	RESET MECHANISM CONVERSION	United States of America	13427041	Mar 22, 2012	Issued	May 14, 2013	8443315
2695.016US1	NON-PREDICATED TO PREDICATED CONVERSION OF ASYNCHRONOUS REPRESENTATIONS	United States of America	12505296	Jul 17, 2009	Issued	May 29, 2012	8191019
2695.017US1	PROGRAMMABLE CROSSBAR STRUCTURES IN ASYNCHRONOUS SYSTEMS	United States of America	12557287	Sep 10, 2009	Issued	Oct 30, 2012	8300635
2695.018US1	ASYNCHRONOUS CONVERSION CIRCUITRYAPPARATUS, SYSTEMS, AND METHODS	United States of America	12559069	Sep 14, 2009	Issued	Mar 1, 2011	7900078
2695.018US2	ASYNCHRONOUS CONVERSION CIRCUITRYAPPARATUS, SYSTEMS, AND METHODS	United States of America	13022843	Feb 8, 2011	Issued	Dec 13, 2011	8078899
2695.019US1	HIERARCHICAL GLOBAL CLOCK TREE	United States of America	12559040	Sep 14, 2009	Issued	Jan 28, 2014	8638138
2695.019US2	HIERARCHICAL GLOBAL CLOCK TREE	United States of America	14159869	Jan 21, 2014	Issued	Jan 13, 2015	8933734
2695.020US1	SOURCE-SYNCHRONOUS CLOCKING	United States of America	12558985	Sep 14, 2009	Issued	Jul 24, 2012	8228101
2695.021US1	RESET SIGNAL DISTRIBUTION	United States of America	12559009	Sep 14, 2009	Issued	Dec 6, 2011	8072250
2695.021US2	RESET SIGNAL DISTRIBUTION	United States of America	13310382	Dec 2, 2011	Issued	Nov 6, 2012	8305124
2695.022US1	MULTI-CLOCK ASYNCHRONOUS LOGIC CIRCUITS	United States of America	12559102	Sep 14, 2009	Issued	Oct 30, 2012	8301933
2695.023US1	ASYCHRONOUS SYSTEM ANALYSIS	United States of America	12570629	Sep 30, 2009	Issued	Feb 25, 2014	8661378
2695.024US1	ASYNCHRONOUS CIRCUIT REPRESENTATION OF SYNCHRONOUS CIRCUIT WITH ASYNCHRONOUS INPUTS	United States of America	12559573	Sep 15, 2009	Issued	Jul 19, 2011	7982502
2695.025US1	TOKEN ENHANCED ASYNCHRONOUS CONVERSION OF SYNCHONOUS CIRCUITS	United States of America	12559612	Sep 15, 2009	Issued	Jul 31, 2012	8234607
2695.026TW1	ONE PHASE LOGIC	Taiwan R.O.C.	100119702	Jun 3, 2011	Issued	Apr 21, 2016	I531165
2695.026US1	ONE PHASE LOGIC	United States of America	12793756	Jun 4, 2010	Issued	Apr 26, 2011	7932746
2695.026US2	ONE PHASE LOGIC	United States of America	13043858	Mar 9, 2011	Issued	Jan 31, 2012	8106683
2695.026US3	ONE PHASE LOGIC	United States of America	13350342	Jan 13, 2012	Issued	Nov 26, 2013	8593176
2695.028US1	EFFICIENT FPGA MULTIPLIERS	United States of America	16134576	Sep 18, 2018	Allowed		
2695.028WO1	EFFICIENT FPGA MULTIPLIERS	PCT	PCTUS2019038100	Jun 20, 2019	Pending		
2695.030US1	EMBEDDED FPGA TIMING SIGN-OFF	United States of America	16363434	Mar 25, 2019	Pending		
2695.031US1	FUSED MEMORY AND ARITHMETIC CIRCUIT	United States of America	16417152	May 20, 2019	Pending		
2695.032US1	Multiple Mode Arithmetic Circuit	United States of America	16535878	Aug 8, 2019	Pending		
2695.033US1	ON-CHIP NETWORK IN PROGRAMMABLE INTEGRATED CIRCUIT	United States of America	16409146	May 10, 2019	Allowed		
2695.034US1	Ethernet Implementation in Field-Programmable Gate Array	United States of America			Unfiled		
2695.036US1	RECONFIGURABLE PROGRAMMABLE INTEGRATED CIRCUIT WITH ON-CHIP NETWORK	United States of America	16409191	May 10, 2019	Pending		
2695.037US1	CASCADE COMMUNICATIONS BETWEEN FPGA TILES	United States of America	16656685	Oct 18, 2019	Pending		
2695.038US1	NOISE-INDEPENDENT LOSS CHARACTERIZATION OF NETWORKS	United States of America	16695743	Nov 26, 2019	Pending		
2695.039US1	Ethernet Packet Processing in Field-Programmable Gate Array	United States of America			Unfiled		
2695.040US1	Wide Elastic Buffer	United States of America			Unfiled		

EXHIBIT C

Trademarks

(all owned and registered to Achronix Semiconductor Corporation)

MARK	COUNTRY	APPLICATION/ REGISTRATION NO.	GOODS/SERVICES	HISTORY AND STATUS
ACHRONIX	United States	Application No. 77085708 Registration No. 3949658	Class 40: Custom manufacture of semiconductor chips and field programmable gate arrays First Use: Aug-01-2004 / First Use in Commerce: Aug-01-2004 Class 42: Product development, namely development, and design of semiconductor chips and field programmable gate arrays First Use: Aug-01-2004 / First Use in Commerce: Aug-01-2004	Filed Jan-18-2007 Registered Apr-26-2011 Affidavit of Use Mar-10-2017
SPEEDSTER	United States	Application No. 77074157 Registration No. 3823430	Class 09: Semiconductor chips First Use: Jan-31-2007 / First Use in Commerce: Aug-15-2008	Filed Jan-02-2007 Registered May-19-2009 Affidavit of Use Apr-28-2015
VECTORPATH	United States	Application No. 88668938	Class 09: Computer hardware	Filed Oct-25-2019
ACHRONIX	Australia (via Madrid Protocol)	Application No. 1506060	Class 40: Custom manufacture of semiconductor chips and field programmable gate arrays Class 42: Product development, namely development, and design of semiconductor chips and field programmable gate arrays	Filed Nov-27-2019
ACHRONIX	Canada	Application No. 1404796 Registration No. TMA895392	Product development, namely development and design of semiconductor chips and field programmable gate arrays (FPGA)	Filed Jul-22-2008 Registered Jan-29-2015
ACHRONIX	Canada	Application No. 1711950 Registration No. TMA988345	Custom manufacture of semiconductor chips and field programmable gate arrays	Filed Jan-22-2015 Registered Jan-12-2018
ACHRONIX	China	Application No. 6974621 Registration No. 6974621	Class 42: Technical research of semiconductor chips and field programmable gate arrays; research and development for others in relation to semiconductor chips and field programmable gate arrays design of computer software in relation to semiconductor chips and field programmable gate arrays; computer system design in relation to semiconductor chips and field programmable gate arrays; materials testing; quality control	Filed Sep-26-2008 Registered Oct-07-2010
SPEEDSTER	China	Application No. 6974624 Registration No. 6974624	Class 09: Transistors and carbons used in electrical equipment; components of electron and electricity	Filed Sep-26-2008 Registered Aug-28-2010
ACHRONIX	European Union	Application No. 006519921 Registration No. 006519921	Class 40: Custom manufacture of semiconductor chips and field programmable gate arrays Class 42: Product development, namely development, design and manufacture of semiconductor chips and field programmable gate arrays	Filed Dec-03-2007 Registered Oct-30-2008
SPEEDSTER	European Union	Application No. 006519953 Registration No. 006519953	Class 09: Semiconductors	Filed Dec-03-2007 Registered Oct-30-2008
ACHRONIX	Hong Kong	Application No. 305127473	Class 40: Custom manufacture of semiconductor chips and field programmable gate arrays Class 42: Product development, namely, development, and design of semiconductor chips and field programmable gate arrays.	Filed Nov-29-2019
VECTORPATH	Hong Kong	Application No. 305127480	Class 09: Computer hardware	Filed Nov-29-2019
ACHRONIX	India (via Madrid Protocol)	Application No. 1506060	Class 40: Custom manufacture of semiconductor chips and field programmable gate arrays Class 42: Product development, namely development, and design of semiconductor chips and field programmable gate arrays	Filed Nov-27-2019
ACHRONIX	Israel (via Madrid Protocol)	Application No. 1506060	Class 40: Custom manufacture of semiconductor chips and field programmable gate arrays Class 42: Product development, namely development, and design of semiconductor chips and field programmable gate arrays	Filed Nov-27-2019
ACHRONIX	Japan	Application No. 2008078851 Registration No. 5273813	Class 40: Manufacture of semiconductor chips and field programmable gate arrays for others Class 42: Development, designing of semiconductor chips and field programmable gate arrays; designing, development of machines, apparatus, instruments [including their parts] or systems composed of such machines,	Filed Sep-26-2008 Registered Oct-16-2009

EXHIBIT C

Trademarks - continued

(all owned and registered to Achronix Semiconductor Corporation)

			apparatus and instruments	
SPEEDSTER	Japan	Application No. 2008078249 Registration No. 5218217	Class 09: Semiconductor chips; other electronic machines, apparatus and their parts	Filed Sep-26-2008 Registered Mar-27-2009
ACHRONIX	Madrid Protocol Designated Jurisdictions Australia, India, Israel, Norway, Singapore, South Korea	Application No. 1506060 Registration No. 1506060	Class 40: Custom manufacture of semiconductor chips and field programmable gate arrays Class 42: Product development, namely development, and design of semiconductor chips and field programmable gate arrays	Filed Nov-27-2019 Registered Dec-26-2019
ACHRONIX	Norway (via Madrid Protocol)	Application No. 1506060	Class 40: Custom manufacture of semiconductor chips and field programmable gate arrays Class 42: Product development, namely development, and design of semiconductor chips and field programmable gate arrays	Filed Nov-27-2019
ACHRONIX	Singapore (via Madrid Protocol)	Application No. 40201923314W Registration No. 1506060	Class 40: Custom manufacture of semiconductor chips and field programmable gate arrays Class 42: Product development, namely development, and design of semiconductor chips and field programmable gate arrays	Filed Nov-27-2019
ACHRONIX	South Korea (via Madrid Protocol)	Application No. 1506060	Class 40: Custom manufacture of semiconductor chips and field programmable gate arrays Class 42: Product development, namely development, and design of semiconductor chips and field programmable gate arrays	Filed Nov-27-2019
ACHRONIX	Taiwan	Application No. 108078313	Class 40: Custom manufacture of semiconductor chips and field programmable gate arrays Class 42: Product development, namely, development, and design of semiconductor chips and field programmable gate arrays	Filed Nov-28-2019
VECTORPATH	Taiwan	Application No. 108078312	Class 09: Computer hardware	Filed Nov-28-2019