TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

ETAS ID: TM585352

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
AVALANCHE TECHNOLOGY, INC.		02/12/2020	Corporation: DELAWARE

RECEIVING PARTY DATA

Name:	SILICON VALLEY BANK
Street Address:	3003 TASMAN DRIVE
City:	SANTA CLARA
State/Country:	CALIFORNIA
Postal Code:	95054
Entity Type:	Corporation: CALIFORNIA

PROPERTY NUMBERS Total: 4

Property Type	Number	Word Mark
Serial Number:	88196128	A
Registration Number:	4946647	AVA
Registration Number:	4237990	AVALANCHE
Registration Number:	4198751	AVALANCHE TECHNOLOGY

CH $115.00 88196128

CORRESPONDENCE DATA

Fax Number: 4048853900

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 4048853868
Email: rusty.close@troutman.com
Correspondent Name: CHRISTOPHER CLOSE
Address Line 1: TROUTMAN PEPPER LLP
Address Line 2: 600 PEACHTREE STREET NE, SUITE 3000
Address Line 4: ATLANTA, GEORGIA 30308-2216

ATTORNEY DOCKET NUMBER:	220763.003057
NAME OF SUBMITTER:	Christopher C Close, Jr.
SIGNATURE:	/Christopher C. Close Jr./
DATE SIGNED:	07/08/2020

Total Attachments: 25

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INTELLECTUAL PROPERTY SECURITY AGREEMENT

THIS INTELLECTUAL PROPERTY SECURITY AGREEMENT ("**Agreement**") is entered into as of February 12, 2020 by and between **SILICON VALLEY BANK**, a California corporation ("**Bank**") and **AVALANCHE TECHNOLOGY, INC.**, a Delaware corporation ("**Grantor**").

RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodation to Grantor (the "**Loans**") in the amounts and manner set forth in that certain Loan and Security Agreement by and between Bank and Grantor dated as of even date herewith (as the same may be amended, modified or supplemented from time to time, the "**Loan Agreement**"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in certain Copyrights, Trademarks, Patents, and Mask Works (as each term is described below) to secure the obligations of Grantor under the Loan Agreement.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

1. Grant of Security Interest. To secure its obligations under the Loan Agreement, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its intellectual property (all of which shall collectively be called the "**Intellectual Property Collateral**"), including, without limitation, the following:

(a) Any and all copyright rights, copyright applications, copyright registrations and like protections in each work or authorship and derivative work thereof, whether published or unpublished and whether or not the same also constitutes a trade secret, now or hereafter existing, created, acquired or held, including without limitation those set forth on Exhibit A attached hereto (collectively, the "**Copyrights**");

(b) Any and all trade secrets, and any and all intellectual property rights in computer software and computer software products now or hereafter existing, created, acquired or held;

(c) Any and all design rights that may be available to Grantor now or hereafter existing, created, acquired or held;

(d) All patents, patent applications and like protections including, without limitation, improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the same, including without limitation the patents and patent applications set forth on Exhibit B attached hereto and any patents and patent applications claiming the priority benefit of the patents and patent applications set forth on Exhibit B attached hereto (collectively, the "**Patents**");

(e) Any trademark and servicemark rights, whether registered or not, applications to register and registrations of the same and like protections, and the entire goodwill of the business of Grantor connected with and symbolized by such trademarks, including without limitation those set forth on Exhibit C attached hereto (collectively, the "**Trademarks**");

(f) All mask works or similar rights available for the protection of semiconductor chips, now owned or hereafter acquired, including, without limitation those set forth on Exhibit D attached hereto (collectively, the "**Mask Works**");

(g) Any and all claims for damages by way of past, present and future infringements of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above;

(h) All licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works and all license fees and royalties arising from such use to the extent permitted by such license or rights;

(i) All amendments, extensions, renewals and extensions of any of the Copyrights, Trademarks, Patents, or Mask Works; and

(j) All proceeds and products of the foregoing, including without limitation all payments under insurance or any indemnity or warranty payable in respect of any of the foregoing.

2. Recordation. Grantor authorizes the Commissioner for Patents, the Commissioner for Trademarks and the Register of Copyrights and any other government officials to record and register this Agreement upon request by Bank.

3. Authorization. Grantor hereby authorizes Bank to (a) modify this Agreement unilaterally by amending the exhibits to this Agreement to include any Intellectual Property Collateral which Grantor obtains subsequent to the date of this Agreement, and (b) file a duplicate original of this Agreement containing amended exhibits reflecting such new Intellectual Property Collateral.

4. Loan Documents. This Agreement has been entered into pursuant to and in conjunction with the Loan Agreement, which is hereby incorporated by reference. The provisions of the Loan Agreement shall supersede and control over any conflicting or inconsistent provision herein. The rights and remedies of Bank with respect to the Intellectual Property Collateral are as provided by the Loan Agreement and related documents, and nothing in this Agreement shall be deemed to limit such rights and remedies.

5. Execution in Counterparts. This Agreement may be executed in counterparts (and by different parties hereto in different counterparts), each of which shall constitute an original, but all of which when taken together shall constitute a single contract. Delivery of an executed counterpart of a signature page to this Agreement by facsimile or in electronic (i.e., "pdf" or "tif" format) shall be effective as delivery of a manually executed counterpart of this Agreement.

6. Successors and Assigns. This Agreement will be binding on and shall inure to the benefit of the parties hereto and their respective successors and assigns.

7. Governing Law. This Agreement and any claim, controversy, dispute or cause of action (whether in contract or tort or otherwise) based upon, arising out of or relating to this Agreement and the transactions contemplated hereby and thereby shall be governed by, and construed in accordance with, the laws of the United States and the State of California, without giving effect to any choice or conflict of law provision or rule (whether of the State of California or any other jurisdiction).

[Signature page follows.]

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

AVALANCHE TECHNOLOGY, INC.

DocuSigned by:
By: Robert Netter
130B73EF8BA2455...
Name: Robert Netter
Title: Chief Financial Officer

BANK:

SILICON VALLEY BANK

DocuSigned by:
By: Tom Graziani
C3323C8A3B8E4B5...
Name: Tom Graziani
Title: Vice President

EXHIBIT A

Copyrights

Description	Registration/ Application Number	Registration/ Application Date
None identified.		

EXHIBIT B

Patents

Description	Registration/ Application Number	Registration/ Application Date
Method for manufacturing Magnetic Memory Cells	16/112,173	8/24/2018
Magnetic random access memory with dynamic random access memory (DRAM) like interface	15/816,887	11/17/2017
Selector Device Incorporating Conductive Cluster for Memory Applications	15/157,607	5/18/2016
Magnetic Memory and method for using the same	16/251,008	1/17/2019
Transient Sensing of Memory Cells	16/176,292	10/31/2018
Magnetic Random Access Memory with Perpendicular Enhancement Layer	16/131,430	9/14/2018
Method for Manufacturing Magnetic Memory Cells	16/112,323	8/24/2018
Perpendicular Magnetic Tunnel Junction (pMTJ) with in-plan Magneto-Static Switching-Enhancing Layer	16/112,173	8/24/2018
Magnetic Memory Element with Multilayered seed structure	16/100,649	8/10/2018
Magnetic memory array incorporating selectors and method for manufacturing the same	16/101,325	8/10/2018
Magnetic Memory Emulating Dynamic Random Access Memory (DRAM)	16/024,601	6/29/2018
Power-Efficient Programming of Magnetic Memory	15/985,268	5/21/2018
Magnetic Memory Incorporating Dual Selectors	16/002,828	5/6/2018
Magnetic Memory Cell Including Two-Terminal selector device	15/921,552	3/14/2018
Magnetic Random Access Memory With Ultrathin Reference Layer	15/863,825	1/5/2018
Method of implementing Magnetic Random Access memory (MRAM) for Mobile System-on Chip Boot	15/815,516	11/16/2017

Selector device Incorporating Conductive Cluster for Memory Application	15/592,575	5/11/2017
Memory System Having Thermally Stable Perpendicular Magneto Tunnel Junction (MTJ) And A Method Of Manufacturing Same	15/438,637	2/21/2017
Magnetic Memory and method for using the same	13/737,897	1/9/2013
Method for Manufacturing Magnetic Memory Cells	10,177,308	1/8/2019
Method for Sensing Memory Element Coupled to Selector Device	10,153,017	12/11/2018
Transient Sensing of Memory Cells	10,127,960	11/13/2018
Serial Link Storage Interface (SLSI) Hybrid Block Storage	10,108,542	10/23/2018
Storage Processor Managing NVME Logically Addressed Solid State Disk Array	10,101,924	10/16/2018
Magnetic Random Access memory having perpendicular Enhancement layer	10,090,456	10/2/2018
Magnetic Random Access memory having perpendicular Enhancement layer	10,079,338	9/18/2018
Magnetic Random Access Memory with Multilayered seed structure	10,050,083	8/14/2018
Storage System Employing MRAM and Array Of Solid State Disks With Integrated Switch	10,042,758	8/7/2018
Storage System Employing MRAM and Array Of Solid State Disks With Integrated Switch	10,037,272	7/31/2018
Magnetic Random Access Memory with Perpendicular Enhancement layer	10,032,979	7/24/2018
Perpendicular Magnetic Fixed layer with high Anisotropy	10,008,663	6/26/2018
Spin-Orbitronics Device And Applications Thereof	10,008,540	6/26/2018
Memory Device for Emulating Dynamic Random Access Memory (DRAM)	9,921,782	3/20/2018
Method And Apparatus For Adjustment Of Current Through A Magnetoresistive Tunnel Junction (MTJ) Based	9,911,482	3/6/2018

On Temperature Fluctuations		
Magnetic Random Access Memory With Dynamic Random Access Memory (DRAM)-Like Interface	9,898,204	2/20/2018
Magnetic Random Access Memory With Ultrathin Reference Layer	9,871,191	1/16/2018
Magnetic Random Access Memory With Ultrathin Reference Layer	9,871,190	1/16/2018
Fast Programming of Magnetic Random Access Memory (MRAM)	9,858,977	1/2/2018
Magnetic Random Access Memory With Perpendicular Enhancement Layer	9,831,421	11/28/2017
Management of Memory Array with Magnetic Random Access Memory (MRAM)	9,830,106	11/28/2017
A Shared Peripheral Component Interconnect Express (PCIE) End Point System with a PCIE Switch And Method For Initializing The Same	9,824,050	11/21/2017
Memory Device Incorporating selector element with multiple thresholds	9,812,499	11/7/2017
Multilayered Seed Structure for Perpendicular MTJ Memory Element	9,793,319	10/17/2017
Landing Pad in Peripheral Circuit For Magnetic Random Access Memory (MRAM)	9,793,318	10/17/2017
Programming of Non-Volatile Memory Subjected to High Temperature Exposure	9,793,003	10/17/2017
A Method of LUN Management In A Solid State Disk Array	9,792,073	10/17/2017
Storage Processor Managing Solid State Disk Array	9,792,047	10/17/2017
Programming of Magnetic Random Access Memory (MRAM) By Boosting gate voltage	9,786,344	10/10/2017
Magnetic Random Access Memory With Perpendicular Enhancement Layer	9,780,300	10/3/2017
Magnetic Random Access Memory With Perpendicular	9,748,471	8/29/2017

Enhancement Layer		
Pulse programming techniques of voltage-controlled magnetroesistive tunnel junction (MTJ)	9,728,240	8/8/2017
A Method and Apparatus For De-Duplication For Solid State Disks (SSDs)	9,727,245	8/8/2017
Fast Programming of Magnetic Random Access Memory (MRAM)	9,691,464	6/27/2017
Perpendicular Magnetic Tunnel Junction (pMTJ) with In-Plane Magneto-Static Switching-Enhancing Layer	9,679,625	6/13/2017
Method Of Implementing Magnetic Random Access Memory (MRAM) For System Boot	9,658,859	5/23/2017
Magnetic Random Access Memory With Dynamic Random Access Memory (DRAM)-Like Interface	9,658,780	5/23/2017
Management Of Memory Array With Magnetic Random Access Memory (MRAM)	9,652,386	5/16/2017
Magnetic Random Access Memory With Perpendicular Enhancement Layer	9,647,202	5/9/2017
Spin-Orbitronics Device And Applications Thereof	9,647,032	5/9/2017
Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) With Enhanced Write Current	9,646,668	5/9/2017
Magnetic Random Access Memory Having Perpendicular Enhancement Layer And Thin Reference Layer	9,634,244	4/25/2017
Three Dimensional Memory Arrays and stitching there of	9,627,438	4/18//17
Magnetic Random Access Memory Having Perpendicular Enhancement Layer And Thin Reference Layer	9,608,038	3/28/2017
Method And Apparatus For Adjustment Of Current Through A Magnetoresistive Tunnel Junction (MTJ) Based On Temperature Fluctuations	9,607,676	3/28/2017
Magnetic Random Access Memory Having Perpendicular Enhancement Layer	9,559,144	1/31/2017
Fast Programming of Magnetic Random Access Memory (MRAM)	9,558,802	1/31/2017

Memory Device With Increased Separation Between Memory Elements	9,548,448	1/17/2017
Magnetic Random Access Memory Having Perpendicular Enhancement Layer And Thin Reference Layer	9,548,334	1/17/2017
Magnetic Random Access Memory Having Perpendicular Enhancement Layer	9,543,506	1/10/2017
Method and Apparatus of increase the reliability of an Access Transistor Coupled to a Magnetic Tunnel Junction (MTJ)	9,530,479	12/27/2016
Method And Apparatus For Programming A Magnetic Tunnel Junction (MTJ)	9,520,174	12/13/2016
Unipolar-Switching Perpendicular MRAM And Method for Using Same	9,502,092	11/22/2016
Magnetic Random Access Memory With Multilayered Seed Structure	9,496,489	11/15/2016
An Improved High Capacity Low Cost Multi-State Magnetic Memory	9,478,279	10/25/2016
Perpendicular MRAM with Magnet	9,472,595	10/18/2016
Spin-Transfer Torque Magnetic Random Access Memory With Perpendicular Magnetic Anisotropy Multilayers	9,444,039	9/13/2016
Magnetic Random Access Memory With Multilayered Seed Structure	9,444,038	9/13/2016
Voltage-Switched Magnetic Random Access Memory (MRAM) And Method For Using The Same	9,443,577	9/13/2016
Spin-Transfer Torque Magnetic Random Access Memory With Perpendicular Magnetic Anisotropy Multilayers	9,419,210	8/16/2016
Magnetic Random Access Memory With Multilayered Seed Structure	9,419,207	8/16/2016
Fast Programming of Magnetic Random Access Memory (MRAM)	9,401,194	7/26/2016
Magnetic Random Access Memory With Dynamic Random Access Memory (DRAM)-Like Interface	9,396,783	7/19/2016

Magnetic Random Access Memory Having Perpendicular Enhancement Layer	9,396,781	7/19/2016
Landing Pad In Peripheral Circuit For Magnetic Random Access Memory (MRAM)	9,373,663	6/21/2016
SSTRAM element having multiple perpendicular MTJS Coupled in series	9,349,941	5/24/2016
Method for Screening Arrays of Magnetic Memories	9,349,427	5/24/2016
Method and Apparatus for Increasing the Reliability of an Access Transistor Coupled To A Magnetic Tunnel Junction (MTJ)	9,343,134	5/17/2016
Magnetic Random Access Memory With Perpendicular Interfacial Anisotropy	9,337,417	5/10/2016
An Improved High Capacity Low Cost Multi-State Magnetic Memory	9,337,413	5/10/2016
Secure Spin Torque Transfer Magnetic Random Access Memory (STTMRAM)	9,319,387	4/19/2016
Spin-Transfer Torque Magnetic Random Access Memory With Perpendicular Magnetic Anisotropy Multilayers	9,318,179	04/192016
Host-Managed Logical Mass Storage Device Using Magnetic Random Access Memory (MRAM)	9,317,206	4/19/2016
Management Of Memory Array With Magnetic Random Access Memory (MRAM)	9,311,232	4/12/2016
Magnetic Random Access Memory With Perpendicular Enhancement Layer	9,306,154	4/5/2016
A Method and Apparatus For Reading A Magnetic Tunnel Junction Using A Sequence Of Short Pulses	9,305,626	4/5/2016
Devices And Methods For Measurement Of Magnetic Characteristics Of MRAM Wafers Using Magnetoresistive Test Strips	9,252,187	2/2/2016
Magnetic Random Access Memory With Dynamic Random Access Memory (DRAM)-Like Interface	9,251,882	2/2/2016
Initialization Method Of A Perpendicular Magnetic Random Access Memory (MRAM) Device With A Stable	9,251,879	2/2/2016

Reference Cell		
Storage System Employing MRAM and Redundant Array of Solid State Disk	9,251,059	2/2/2016
Magnetic Random Access Memory Having Perpendicular Enhancement Layer And Interfacial Anisotropic Free Layer	9,231,027	1/5/2016
A Shared Peripheral Component Interconnect Express (PCIE) End Point System With A PCIe Switch And Method For Initializing The Same	9,229,892	1/5/2016
Mapping Of Random Defects In A Memory Device	9,224,504	12/29/2015
High capacity low cost multi-state magnetic memory	9,218,866	12/22/2015
Controller Management Of Memory Array Of Storage Device Using Magnetic Random Access Memory (MRAM)	9,213,495	12/15/2015
Memory Device Having Stitched Arrays Of 4 F Memory Cells	9,209,390	12/8/2015
Perpendicular Magnetic Tunnel Junction (pMTJ) WITH In-Plane Magneto-Static Switching-Enhancing Layer	9,196,332	11/24/2015
MTJ Stack And Bottom Electrode Patterning Process With Ion Beam Etching Using A Single Mask	9,166,154	10/20/2015
Electric Field Assisted MRAM And Method For Using The Same	9,166,146	10/20/2015
Magnetic Random Access Memory With Multiple Free Layers	9,166,143	10/20/2015
Flash subsystem organized into pairs of upper and lower page location	9,158,623	10/13/2015
Perpendicular Magnetic Random Access Memory (MRAM) Device With A Stable Reference Cell	9,142,755	9/22/2015
Semiconductor Memory Device Having Increased Separation Between Memory Elements	9,123,575	9/1/2015
Apparatus For Initializing Perpendicular MRAM Device	9,117,532	8/25/2015
Three-Dimensional Flash Memory Device	9,112,051	8/18/2015

Multi-Level Cells And Method For Using The Same	9,105,343	8/11/2015
Non-Volatile Block Storage Module Using Magnetic Random Access Memory (MRAM)	9,087,562	7/21/2015
Memory With On-Chip Error Correction	9,083,382	7/14/2015
Magnetic Random Access Memory With Perpendicular Enhancement Layer	9,082,951	7/14/2015
Vialess Memory Structure And Method Of Manufacturing Same	9,082,695	7/14/2015
A Hybrid Non-Volatile Memory Device	9,081,669	7/14/2015
Fabrication Method Using Thinner Hard Mask For High-Density MRAM	9,070,869	6/30/2015
Magnetic Random Access Memory Having Perpendicular Enhancement Layer	9,070,855	6/30/2015
Shields For Magnetic Memory Chip Packages	9,070,692	6/30/2015
Magnetic Random Access Memory (MRAM) With Enhanced Magnetic Stiffness And Method Of Making Same	9,070,464	6/30/2015
Method And Apparatus For Programming A Magnetic Tunnel Junction (MTJ)	9,070,458	6/30/2015
Persistent Block Storage Attached To Memory Bus	9,058,257	6/16/2015
Magnetic Random Access Memory (MRAM) With Enhanced Magnetic Stiffness And Method Of Making Same	9,054,298	6/9/2015
A High Capacity Low Cost Multi-State Magnetic Memory	9,047,968	6/2/2015
A Computer System With Physically-Addressable Solid State Disk (SSD) And A Method Of Addressing The Same	9,037,787	5/19/2015
Storage System Employing MRAM And Array Of Solid State Disks With Integrated Switch	9,037,786	5/19/2015
Initialization Method Of A Perpendicular Magnetic Random Access Memory (MRAM) Device	9,030,866	5/12/2015
Memory device having stitched arrays of 4 F.sup.2 memory	9,029,824	5/12/2015

cells		
High Density Resistive Memory Having A Vertical Dual Channel Transistor	9,029,822	5/12/2015
MTJ Manufacturing Method Utilizing In-Situ Annealing And Etch Back	9,028,910	5/12/2015
A Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) with Perpendicular Laminated Free layer	9,025,371	5/5/2015
Perpendicular STTMRAM Device With Balanced Reference Layer	9,024,398	05//05/15
Spin-Transfer Torque Magnetic Random Access Memory With Perpendicular Magnetic Anisotropy Multilayers	9,019,758	4/28/2015
MRAM with sidewall protection and method of fabrication	9,013,045	4/21/2015
Storage Processor Managing Solid State Disk Array	9,009,397	4/14/2015
Physically Addressed Solid State Disk Employing Flash And Magnetic Random Access Memory (MRAM)	9,009,396	4/14/2015
Mobile device using secure spin torque transfer magnetic random access memory (SSTMRAM)	8,996,888	3/31/2015
Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) with Perpendicular Laminated Free layer	8,982,616	03-17-15
Magnetic Random Access Memory With Switchable Switching Assist Layer	8,981,506	3/17/2015
Method For Manufacturing Non-Volatile Magnetic Memory	8,980,649	3/17/2015
Method For Forming MTJ Memory Element	8,975,089	3/10/2015
MRAM Etching Processes	8,975,088	3/10/2015
Emulation Of Static Random Access Memory (SPAM) By Magnetic Random Access Memory (MRAM)	8,971,107	3/3/2015
Initialization Method Of A Perpendicular Magnetic Random Access Memory (MRAM) Device	8,971,100	3/3/2015
Storage Processor Managing NVME Logically Addressed	8,966,164	2/24/2015

Solid State Disk Array		
Method Of Manufacturing Magnetic Tunnel Junction Memory Element	8,962,349	2/24/2015
Secure Spin Torque Transfer Magnetic Random Access Memory (STTMRAM)	8,954,759	2/10/2015
Method of LUN management in a solid state disk array	8,954,658	2/10/2015
Storage Processor Managing Solid State Disk Array	8,954,657	2/10/2015
Host-Managed Logical Mass Storage Device Using Magnetic Random Access Memory (MRAM)	8,947,937	2/3/2015
A Method And Apparatus For Reading A Magnetic Tunnel Junction Using A Sequence Of Short Pulses	8,947,922	2/3/2015
High Capacity Low Cost Multi-Stacked Cross-Line Magnetic Memory	8,947,919	2/3/2015
Method For Magnetic Screening Of Arrays Of Magnetic Memories	8,942,032	1/27/2015
Method for reducing Effective Raw Bit Error Rate in Multi-Level Cell NAND Flash Memory	8,935,599	1/13/2015
Controller Management Of Memory Array Of Storage Device Using Magnetic Random Access Memory (MRAM)	8,929,146	1/6/2015
Method And Apparatus For Increasing The Reliability Of An Access Transistor Coupled To A Magnetic Tunnel Junction (MTJ)	8,917,546	12/23/2014
A Multi-State Spin-Torque Transfer Magnetic Random Access Memory	8,917,543	12/23/2014
Storage System Employing MRAM and Physically Addressed Solid State Disk	8,909,855	12/9/2014
Method Of Sensing Data In Magnetic Random Access Memory With Overlap Of High And Low Resistance Distributions	8,891,326	11/18/2014
Magnetoresistive layer structure with voltage-induced switching and lotic cell application	8,891,292	11/18/2014

Magnetoresistive Logic Cell And Method Of Use	8,891,291	11/18/2014
Memory Device Having Vertical Selection Transistors With Shared Channel Structure And Method For Making The Same	8,890,108	11/18/2014
Mapping Of Random Defects In A Memory Device	8,887,013	11/11/2014
Magnetoresistive Logic Cell And Method Of Use	8,885,395	11/11/2014
Redeposition Control in MRAM Fabrication Process	8,883,520	11/11/2014
Method and Apparatus for Programming a Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) Array	8,879,309	11/4/2014
Memory Device Having Stitched Arrays Of 4 F2 Memory Cells	8,878,156	11/4/2014
Multi-Port Magnetic Random Access Memory (MRAM)	8,861,260	10/14/2014
High speed SST-MRAM with orthogonal pinned layer	8,860,158	10/14/2014
Magnetic Random Access Memory (MRAM) With Enhanced Magnetic Stiffness And Method Of Making Same	8,852,676	10/7/2014
Magnetic Tunnel Junction With Non-Metallic Layer Adjacent to Free Layer	8,836,061	9/16/2014
A Bottom-Type Perpendicular Magnetic Tunnel Junction (pMTJ) Element With Thermally Stable Amorphous Blocking Layers	8,836,000	9/16/2014
A Method And Apparatus For Sensing The State Of A Magnetic Tunnel Junction (MTJ)	8,830,737	9/9/2014
Initialization Method Of A Perpendicular Magnetic Random Access Memory (MRAM) Device With A Stable Reference Cell	8,830,736	9/9/2014
Method for Bit-Error Rate Testing of Resistance-based RAM Cells Using a Reflected Signal	8,806,284	8/12/2014
Multi Root Shared Peripheral Component Interconnect Express (PCIE) End Point	8,806,098	8/12/2014
Access Transistor With A Buried Gate	8,803,200	8/12/2014

Method For Manufacturing High Density Non-Volatile Magnetic Memory	8,802,451	8/12/2014
MRAM With Sidewall Protection And Method Of Fabrication	8,796,795	8/5/2014
Fast Programming of Magnetic Random Access Memory (MRAM)	8,792,269	7/29/2014
Spin Transfer Torque Magnetic Random Access Memory (STTMRAM) Having Graded Synthetic Free Layer	8,779,537	7/15/2014
MTJ MRAM With Stud Patterning	8,772,888	7/8/2014
Spin Transfer Torque Magnetic Random Access Memory (STTMRAM) Having Graded Synthetic Free Layer	8,772,886	07/08/2014
Magnetic memory write circuitry	8,760,914	6/24/2014
SST-MRAM MTJ manufacturing method with in-situ annealing	8,758,850	6/24/2014
Emulation Of Static Random Access Memory (SPAM) By Magnetic Random Access Memory (MRAM)	8,755,221	6/17/2014
Memory with on-chip error correction	8,751,905	6/10/2014
Embedded Magnetic Random Access Memory (MRAM)	8,730,716	5/20/2014
A High Capacity Low Cost Multi-State Magnetic Memory	8,724,413	5/13/2014
Controller Management Of Memory Array Of Storage Device Using Magnetic Random Access Memory (MRAM)	8,724,392	5/13/2014
Method For Reading And Writing Multi-Level Cells	8,724,380	5/13/2014
A Magnetic Memory With A Domain Wall	8,724,379	5/13/2014
Shared Transistor in a Spin-Torque Transfer Magnetic Random Access Memory (STTMRAM) Cell	8,724,378	5/13/2014
Access Transistor With A Buried Gate	8,723,281	5/13/2014
Non-Volatile Block Storage Module Using Magnetic Random Access Memory (MRAM)	8,719,492	5/6/2014
Management Of Memory Array With Magnetic Random Access Memory (MRAM)	8,711,631	4/29/2014

Non-Volatile Flash-RAM Memory With Magnetic Memory	8,711,613	4/29/2014
MRAM with sidewall protection and method of fabrication	8,709,956	4/29/2014
Memory Device Including Transistor Array With Shared Plate Channel And Method For Making The Same	8,704,206	4/22/2014
A Method And Apparatus For Reading A Magnetic Tunnel Junction Using A Sequence Of Short Pulses	8,693,240	4/8/2014
Flash Memory With Nano-Pillar Charge Trap	8,687,418	4/1/2014
Persistent Block Storage Attached To Memory Bus	8,677,097	3/18/2014
Host-Managed Logical Mass Storage Device Using Magnetic Random Access Memory (MRAM)	8,670,276	3/11/2014
Multi-Port Magnetic Random Access Memory (MRAM)	8,670,264	3/11/2014
Method for reducing Effective Raw Bit Error Rate in Multi-Level Cell NAND Flash Memory	8,656,255	2/18/2014
Method Of Sensing Data Of A Magnetic Random Access Memories (MRAM)	8,644,060	2/4/2014
Embedded Magnetic Random Access Memory (MRAM)	8,634,234	1/21/2014
Method and apparatus for measuring magnetic parameters of magnetic thin film structures	8,633,720	1/21/2014
Magnetic Random Access Memory (MRAM) With Enhanced Magnetic Stiffness And Method Of Making Same	8,623,452	1/7/2014
A Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) Using A Synthetic Free Layer	8,611,147	12/17/2013
Spin-Torque Transfer Magnetic Random Access Memory (STTMRAM) Device with Shared Transistor and Minimal Written Data Disturbance	8,611,145	12/17/2013
Magnetic Random Access Memory With Field Compensating Layer And Multi-Level Cell	8,598,576	12/3/2013
Non-Volatile Block Storage Module Using Magnetic Random Access Memory (MRAM)	8,595,427	11/26/2013
Spin-Transfer Torque Magnetic Random Access Memory	8,593,862	11/26/2013

Having Magnetic Tunnel Junction With Perpendicular Magnetic Anisotropy		
Resistive Memory Device Having Vertical Transistors And Method For Making The Same	8,575,584	11/5/2013
MRAM Fabrication Method with Sidewall Cleaning	8,574,928	11/5/2013
Magnetic Random Access Memory With Field Compensating Layer And Multi-Level Cell	8,565,010	10/22/2013
Perpendicular MRAM Device And Its Initialization Method	8,559,215	10/15/2013
Method For Magnetic Screening Of Arrays Of Magnetic Memories	8,553,452	10/8/2013
Host-Managed Logical Mass Storage Device Using Magnetic Random Access Memory (MRAM)	8,547,745	10/1/2013
Method of reading logical mass storage device using magnetic random access memory (MRAM)	8,547,734	10/1/2013
Magnetic Random Access Memory (MRAM) Manufacturing Process for a Small Magnetic Tunnel Junction (MTJ) Design with a Low Programming Current Requirement	8,542,526	9/24/2013
Magnetic Random Access Memory (MRAM) Manufacturing Process for a Small Magnetic Tunnel Junction (MTJ) Design with a Low Programming Current Requirement	8,542,524	9/24/2013
MRAM Etching Processes	8,536,063	9/17/2013
Method For Manufacturing Non-Volatile Magnetic Memory	8,535,952	9/17/2013
Controller Management Of Memory Array Of Storage Device Using Magnetic Random Access Memory (MRAM)	8,526,234	9/3/2013
Spin-transfer torque magnetic random access memory with multilayered storage layer	8,519,496	8/27/2013
Low resistance high-TMR magnetic tunnel junction and process for fabrication thereof	8,508,984	8/13/2013

Non-Volatile Magnetic Memory Element with Graded Layer	8,498,150	7/30/2013
Non-Volatile Magnetic Memory Element with Graded Layer	8,498,149	7/30/2013
Non-Volatile Magnetic Memory Element with Graded Layer	8,498,148	7/30/2013
Non-Volatile Magnetic Memory Element with Graded Layer	8,493,780	7/23/2013
Non-Volatile Magnetic Memory Element with Graded Layer	8,493,779	7/23/2013
Non-Volatile Magnetic Memory Element with Graded Layer	8,493,778	7/23/2013
Non-Volatile Magnetic Memory With Low Switching Current And High Thermal Stability	8,493,777	7/23/2013
Magnetic Latch Magnetic Random Access Memory (MRAM)	8,492,860	7/23/2013
Non-Volatile Magnetic Memory Element with Graded Layer	8,488,376	7/16/2013
Non-Uniform Switching Based Non-Volatile Magnetic Based Memory	8,477,530	7/2/2013
Embedded Magnetic Random Access Memory (MRAM)	8,477,529	7/2/2013
Low Cost Multi-State Magnetic Memory	8,456,897	6/4/2013
A Low-Cost Non-Volatile Flash-RAM Memory	8,440,471	5/14/2013
Low Current Switching Magnetic Tunnel Junction Design For Magnetic Memory Using Domain Wall Motion	8,427,863	4/23/2013
Low-crystallization temperature MTJ for Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM)	8,422,286	4/16/2013
Non-Volatile Magnetic Memory With Low Switching Current And High Thermal Stability	8,405,174	3/26/2013
Non-Volatile Magnetic Memory Element with Graded Layer	8,399,943	3/19/2013

Non-Volatile Magnetic Memory Element with Graded Layer	8,399,942	3/19/2013
A Low-Cost Non-Volatile Flash-RAM Memory	8,391,058	3/5/2013
A High Capacity Low Cost Multi-State Magnetic Memory	8,391,054	3/5/2013
Non-Uniform Switching Based Non-Volatile Magnetic Based Memory	8,389,301	3/5/2013
Differential Magnetic Random Access Memory (MRAM)	8,385,108	2/26/2013
A Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) With Laminated Free Layer	8,374,025	2/12/2013
Method And Apparatus For Programming A Magnetic Tunnel Junction (MTJ)	8,363,460	1/29/2013
Memory Sensing Circuit	8,363,457	1/29/2013
Low Cost Multi-State Magnetic Memory	8,330,240	12/11/2012
Magnetic Tunnel Junction (MTJ) Formation With Two-Step Process	8,313,960	11/20/2012
Non-Volatile Magnetic Memory With Low Switching Current And High Thermal Stability	8,310,020	11/13/2012
Method And Apparatus For Increasing The Reliability Of An Access Transistor Coupled To A Magnetic Tunnel Junction (MTJ)	8,295,083	10/23/2012
Embedded Magnetic Random Access Memory (MRAM)	8,289,757	10/16/2012
Shared Transistor in a Spin-Torque Transfer Magnetic Random Access Memory (STTMRAM) Cell	8,238,145	8/7/2012
Non-Volatile Magnetic Memory With Low Switching Current And High Thermal Stability	8,183,652	5/22/2012
Low-crystallization temperature MTJ for Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM)	8,169,821	5/1/2012
Low Current Switching Magnetic Tunnel Junction Design For Magnetic Memory Using Domain Wall Motion	8,164,947	4/24/2012
Magnetic Tunnel Junction (MTJ) Formation With Two-Step Process	8,148,174	4/3/2012

A Low-Cost Non-Volatile Flash-Ram Memory	8,120,949	2/21/2012
Non-Uniform Switching Based Non-Volatile Magnetic Based Memory	8,084,835	12/27/2011
Non-Volatile Magnetic Memory Element with Graded Layer	8,063,459	11/22/2011
A High Capacity Low Cost Multi-State Magnetic Memory	8,058,696	11/15/2011
Low Cost Multi-State Magnetic Memory	8,018,011	9/13/2011
Current-Confined Effect Of Magnetic Nano-Current-Channel (NCC) For Magnetic Random Access Memory (MRAM)	7,981,697	7/19/2011
Low Current Switching Magnetic Tunnel Junction Design For Magnetic Memory Using Domain Wall Motion	7,869,266	1/11/2011
Current-Confined Effect Of Magnetic Nano-Current-Channel (NCC) For Magnetic Random Access Memory (MRAM)	7,732,881	6/8/2010
Physically-Addressable Solid State Disk (SSD) and a Method of Addressing the Same	14/697,544	4/27/2015
Perpendicular MRAM with MTJ Including Laminated Magnetic Layers	13/538,863	06/29/2012
Memory System Having Thermally Stable Perpendicular Magneto Tunnel Junction (MTJ) and a Method of Manufacturing Same	14/021,917	09/09/2013
Multilayered Seed Structure for Magnetic Memory Element Including a CoFeB Seed Layer	10,438,997	10/08/2019
Magnetic Memory Element Including Magnesium Perpendicular Enhancement Layer	10,490,737	11/26/2019
High Capacity Low Cost Multi-Stacked Cross-Line Magnetic Memory	11/740,861	04/26/2007
High Capacity Low Cost Multi-Stacked Cross-Line Magnetic Memory	11/866,830	10/03/2007
Multi-State Spin-Torque Transfer Magnetic Random Access Memory	12/397,255	03/03/2009

Trough Channel Transistor and Methods for Making the Same	13/136,051	07/21/2011
Memory System Having Thermally Stable Perpendicular Magneto Tunnel Junction (MTJ) and a Method of Manufacturing Same	13/277,187	10/19/2011
Magnetic Random Access Memory (MRAM) Device Fabricated by a High Selectivity Hard Mask and Process for Making the Same	13/369,756	02/09/2012
Solid State Disk Employing Flash and Magnetic Random Access Memory (MRAM)	13/570,202	08/08/2012
Field Effect Transistor Having a Through Channel	14/043,477	10/01/2013
Method of Managing Redundant Array of Independent Disks (RAID) Groups in a Solid State Disk Array	14/157,394	01/16/2014
Method of Managing Throughput of Redundant Array of Independent Disks (RAID) Groups in a Solid State Disk	14/168,642	01/30/2014
Method of Thin Provisioning in a Solid State Disk Array	14/171,234	02/03/2014
MTJ Memory Cell with Protection Sleeve and Method for Making Same	14/501,463	09/30/2014
Redeposition Control in MRAM Fabrication Process	14/501,553	09/30/2014
Mapping of Random Defects in a Memory Device	14/505,343	10/02/2014
Secure Spin Torque Transfer Magnetic Random Access Memory (STTMRAM)	14/542,533	11/14/2014
Physically-Addressable Solid State Disk (SSD) and a Method of Addressing the Same	14/697,538	04/27/2015
Method and Apparatus to Reduce Thermal Resistance in a Server Chassis	14/845,191	09/03/2015
Selector Device Having Asymmetric Conductance for Memory Applications	15/438,631	02/21/2017
Magnetic Random Access Memory with Dynamic Random Access Memory (DRAM)-Like Interface	16/383,361	04/12/2019
Magnetic Memory Emulating Dynamic Random Access Memory (DRAM)	16/550,103	08/23/2019

EXHIBIT C

Trademarks

Description	Registration/ Application Number	Registration/ Application Date
A (& design)	88/196,128	11/15/2018
AVA	4,946,647	04/26/2016
AVALANCHE	4,237,990	11/06/2012
AVALANCHE TECHNOLOGY	4,198,751	08/28/2012

EXHIBIT D

Mask Works

Description	Registration/ Application Number	Registration/ Application Date
None identified.		