TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

ETAS ID: TM628646

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
Wave Computing, Inc.		02/26/2021	Corporation: DELAWARE
MIPS TECH, LLC		02/26/2021	Limited Liability Company: DELAWARE
MIPS TECH, INC.		02/26/2021	Corporation: DELAWARE
HELLOSOFT, INC.		02/26/2021	Corporation: DELAWARE
WAVE COMPUTING (UK) LIMITED		02/26/2021	Limited Corporation: UNITED KINGDOM
IMAGINATION TECHNOLOGIES, INC.		02/26/2021	Corporation: DELAWARE
CAUSTIC GRAPHICS, INC.		02/26/2021	Corporation: DELAWARE

RECEIVING PARTY DATA

Name:	WAVE COMPUTING LIQUIDATING TRUST
Street Address:	c/o Castellammare Advisors, LLC
Internal Address:	232 Quadro Vecchio Drive
City:	Pacific Palisades
State/Country:	CALIFORNIA
Postal Code:	90272
Entity Type:	Statutory Trust: DELAWARE

CH $340.00 2107854

PROPERTY NUMBERS Total: 13

Property Type	Number	Word Mark
Registration Number:	2107854	CODESCAPE
Registration Number:	3065000	MEOS
Registration Number:	3928894	MICROMIPS
Registration Number:	3255604	MIPS
Registration Number:	1734429	MIPS
Registration Number:	1493963	MIPS
Registration Number:	2896003	MIPS
Registration Number:	2800581	MIPS32
Registration Number:	2883124	MIPS32
Registration Number:	2968237	MIPS64

Property Type	Number	Word Mark
Registration Number:	2764564	MIPS64
Registration Number:	5402116	WAVE COMPUTING
Registration Number:	4913985	WAVE SEMI

CORRESPONDENCE DATA

Fax Number: 3038997333

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 3038997300
Email: BoxIP@hoganlovells.com
Correspondent Name: David London, Hogan Lovells US LLP
Address Line 1: 1601 Wewatta Street, Suite 900
Address Line 4: Denver, COLORADO 80202

ATTORNEY DOCKET NUMBER:	767747.000001
NAME OF SUBMITTER:	David L London
SIGNATURE:	/ DLL /
DATE SIGNED:	02/26/2021

Total Attachments: 18
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INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement is entered into as of the 26th day of February, 2021 by and among WAVE COMPUTING LIQUIDATING TRUST, a Delaware statutory trust (in such capacity, together with its successors and assigns, the "Lender"), WAVE COMPUTING, INC., a Delaware corporation (the "Borrower"), and MIPS TECH, LLC, a Delaware limited liability company ("MIPS"), MIPS TECH, INC., a Delaware corporation ("MIPS Inc."), HELLOSOFT, INC., a Delaware corporation ("HelloSoft"), WAVE COMPUTING (UK) LIMITED, a United Kingdom limited corporation ("Wave UK"), IMAGINATION TECHNOLOGIES, INC., a Delaware corporation ("Imagination") and CAUSTIC GRAPHICS, INC., a Delaware corporation ("Caustic", together with the Borrower, MIPS, MIPS Inc., HelloSoft, Wave UK, Imagination and any other Person that joins this Intellectual Property Security Agreement as a Grantor, each a "Grantor" and collectively, the "Grantors").

RECITALS

A. The Lender has agreed to make a loan to the Borrower (the "Loan") in the amount and manner set forth in that certain Loan and Security Agreement, by and among the Lender and the Grantors to be dated on or about the date hereof (as the same may be amended, modified or supplemented from time to time, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). The Lender is willing to make the Loan to the Borrower, but only upon the condition, among others, that the Grantors shall grant to the Lender a security interest in certain Copyrights, Trademarks and Patents to secure the obligations of the Grantors under the Loan Agreement.

B. Pursuant to the terms of the Loan Agreement, each Grantor has granted to the Lender a security interest in all of such Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement, each Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

1. To secure its obligations under the Loan Agreement, each Grantor hereby grants and pledges to the Lender a continuing security interest in all of such Grantor's right, title and interest in, to and under all of its now owned, held or existing and hereafter owned, held, acquired or arising intellectual property (all of which shall collectively be called the "Intellectual Property Collateral"), including, without limitation, the following:

(a) Any and all United States copyright applications and copyright registrations including those set forth on Exhibit A attached hereto, as such Exhibit may be amended, modified or supplemented from time to time, and all amendments, extensions and renewals of the foregoing (collectively, the "Copyrights");

(b) Any and all United States issued patents and patent applications including those set forth on Exhibit B attached hereto, as such Exhibit may be amended, modified or supplemented from time to time, and including, without limitation, all improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the foregoing (collectively, the "Patents");

(c) Any and all United States trademark and service mark applications and registrations, and the entire goodwill of the business of such Grantor connected with and symbolized by such trademarks and service marks including those set forth on Exhibit C attached hereto, as such Exhibit may be amended, modified or supplemented from time to time, and all amendments, extensions and renewals of the foregoing (collectively, the "Trademarks");

(d) Any and all claims for damages by way of past, present and future infringements of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above; and

(e) All income, royalties, proceeds and products of the foregoing, including without limitation all payments under insurance or any indemnity or warranty payable in respect of any of the foregoing;

provided that, notwithstanding anything herein to the contrary, in no event shall the Intellectual Property Collateral include and the Grantor shall not be deemed to have granted a Lien in, any of its right, title or interest in any property if, and solely for the duration of any period that, the grant of such Lien shall constitute or result in the abandonment of, invalidation of or rendering unenforceable any of its right, title or interest therein.

2. This security interest is granted in conjunction with the security interest granted to the Lender under the Loan Agreement. The rights and remedies of the Lender with respect to the security interest granted hereby are in addition to those set forth in the Loan Agreement and the other Loan Documents, and those which are now or hereafter available to the Lender as a matter of law or equity. The rights and remedies of the Lender with respect to the security interest granted herein are without prejudice to and are in addition to those set forth in the Security Agreement and the other Loan Documents, all terms and provisions of which are incorporated herein by reference. In the event that any provisions of this Intellectual Property Security Agreement are deemed to conflict with the Loan Agreement, the provisions of the Loan Agreement shall govern.

3. THIS INTELLECTUAL PROPERTY SECURITY AGREEMENT AND ALL DISPUTES AND OTHER MATTERS RELATING HERETO OR THERETO OR ARISING THEREFROM (WHETHER SOUNDING IN CONTRACT LAW, TORT LAW OR OTHERWISE), SHALL BE GOVERNED BY, AND SHALL BE CONSTRUED AND ENFORCED IN ACCORDANCE WITH, THE LAWS OF THE STATE OF CALIFORNIA, WITHOUT REGARD TO CONFLICTS OF LAWS PRINCIPLES.

4. TO THE FULLEST EXTENT PERMITTED BY APPLICABLE LAW, EACH GRANTOR AND THE LENDER WAIVE THEIR RESPECTIVE RIGHT TO A JURY TRIAL OF ANY CLAIM OR CAUSE OF ACTION ARISING OUT OF OR BASED UPON THIS INTELLECTUAL PROPERTY SECURITY AGREEMENT, THE LOAN DOCUMENTS OR ANY CONTEMPLATED TRANSACTION, INCLUDING CONTRACT, TORT, BREACH OF DUTY AND ALL OTHER CLAIMS. THIS WAIVER IS A MATERIAL INDUCEMENT FOR EACH PARTY TO ENTER INTO THIS INTELLECTUAL PROPERTY SECURITY AGREEMENT. EACH PARTY HAS REVIEWED THIS WAIVER WITH ITS COUNSEL.

5. WITHOUT INTENDING IN ANY WAY TO LIMIT THE PARTIES' AGREEMENT TO WAIVE THEIR RESPECTIVE RIGHT TO A TRIAL BY JURY, if the above waiver of the right to a trial by jury is not enforceable, the parties hereto agree that any and all disputes or controversies of any nature between them arising at any time shall be decided by a reference to a private judge, mutually selected by the parties (or, if they cannot agree, by the Presiding Judge of the Santa Clara County, California Superior Court) appointed in accordance with California Code of Civil Procedure Section 638 (or pursuant to comparable provisions of federal law if the dispute falls within the exclusive jurisdiction of the federal courts), sitting without a jury, in Santa Clara County, California; and the parties hereby submit to the jurisdiction of such court. The reference proceedings shall be conducted pursuant to and in accordance with the provisions of California Code of Civil Procedure Sections 638 through 645.1, inclusive. The private judge shall have the power, among others, to grant provisional relief, including without limitation, entering temporary restraining orders, issuing preliminary and permanent injunctions and appointing receivers. All such proceedings shall be closed to the public and confidential and all records relating thereto shall be permanently sealed. If during the course of any dispute, a party desires to seek provisional relief, but a judge has not been appointed at that point pursuant to the judicial reference procedures, then such party may apply to the Santa Clara County, California Superior Court for such relief. The proceeding before the private judge shall be conducted in the same manner as it would be before a court under the rules of evidence applicable to judicial

proceedings. The parties shall be entitled to discovery which shall be conducted in the same manner as it would be before a court under the rules of discovery applicable to judicial proceedings. The private judge shall oversee discovery and may enforce all discovery rules and orders applicable to judicial proceedings in the same manner as a trial court judge. The parties agree that the selected or appointed private judge shall have the power to decide all issues in the action or proceeding, whether of fact or of law, and shall report a statement of decision thereon pursuant to California Code of Civil Procedure Section 644(a). Nothing in this paragraph shall limit the right of any party at any time to exercise self-help remedies, foreclose against collateral, or obtain provisional remedies. The private judge shall also determine all issues relating to the applicability, interpretation, and enforceability of this paragraph. This Section 4 shall survive the termination of this Intellectual Property Security Agreement.

6. The provisions of the Loan Agreement regarding jurisdiction, and venue are incorporated herein and shall govern this Intellectual Property Security Agreement. This Intellectual Property Security Agreement shall inure to the benefit of the Lender and its successors and assigns, and shall be binding upon each Grantor and its successors and assigns.

7. This Intellectual Property Security Agreement may be signed in any number of counterparts, each of which shall be deemed an original and all of which when taken together shall constitute one and the same instrument. Delivery of an executed counterpart of this Intellectual Property Security Agreement by facsimile or by electronic mail delivery of an electronic version (e.g., .pdf or .tif file) of an executed signature page shall be effective as delivery of an original executed counterpart hereof and shall bind the parties hereto.

[Signature page follows]

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by their respective officers thereunto duly authorized as of the first date written above.

GRANTORS:

WAVE COMPUTING, INC., as a Grantor

DocuSigned by:
By: Desi Banatao
8FA88D02E635409...
Name: Desi Banatao
Title: President, Secretary and Treasurer

MIPS TECH, INC., as a Grantor

DocuSigned by:
By: Desi Banatao
8FA88D02E635409...
Name: Desi Banatao
Title: President, Secretary and Treasurer

HELLOSOFT, INC., as a Grantor

DocuSigned by:
By: Desi Banatao
8FA88D02E635409...
Name: Desi Banatao
Title: President, Secretary and Treasurer

IMAGINATION TECHNOLOGIES, INC.,
as a Grantor

DocuSigned by:
By: Desi Banatao
8FA88D02E635409...
Name: Desi Banatao
Title: President, Secretary and Treasurer

CAUSTIC GRAPHICS, INC., as a Grantor

DocuSigned by:
By: Desi Banatao
8FA88D02E635409...
Name: Desi Banatao
Title: President, Secretary and Treasurer

MIPS TECH, LLC, as a Grantor

By: DocuSigned by: Desi Banatao
6FA88D02E633409...
Name: Desi Banatao
Title: President, Secretary and Treasurer

WAVE COMPUTING (UK) LIMITED,
as a Grantor

By: DocuSigned by: Desi Banatao
6FA88D02E633409...
Name: Desi Banatao
Title: Authorized Signatory

LENDER:

WAVE COMPUTING LIQUIDATING TRUST, as the Lender

By: _____
Name: Robert A. Kors
Title: Trust Manager

[Signature Page Intellectual Property Security Agreement]

EXHIBIT A

Copyrights

NONE

EXHIBIT B

Patents

Title	Owner	Application No.	Registration / Application Date	Registration No. or Publication No.
MULTI-THREADED DATA PROCESSING SYSTEM	MIPS TECH, LLC	15/467073	3/23/2017	10,318,296
INDIRECT BRANCH PREDICTION	MIPS TECH, LLC	15/707059	9/18/2017	10,261,798
CONDITIONAL BRANCH PREDICTION USING A LONG HISTORY	MIPS TECH, LLC	14/809187	7/25/2015	10,318,304
CACHE OPERATION IN A MULTI-THREADED PROCESSOR	MIPS TECH, LLC	14/873027	10/1/2015	10,318,172
CONTROL OF PRIORITY AND INSTRUCTION RATES ON A MULTITHREADED PROCESSOR	MIPS TECH, LLC	10/468434	9/11/2007	7269713
CONTROL OF PRIORITY AND INSTRUCTION RATES ON A MULTITHREADED PROCESSOR	MIPS TECH, LLC	11/524822	2/26/2008	7337303
MECHANISM FOR EXTENDING PROPERTIES OF VIRTUAL MEMORY PAGES MAPPED BY A TLB	MIPS TECH, LLC	09/822783	11/18/2003	6651156
EXPANDED FUNCTIONALITY OF PROCESSOR OPERATIONS WITHIN A FIXED WIDTH INSTRUCTION ENCODING	MIPS TECH, LLC	11/725631	6/26/2012	8209520
MECHANISM FOR PROGRAMMABLE MODIFICATION OF MEMORY MAPPING GRANULARITY	MIPS TECH, LLC	09/905180	2/18/2003	6523104
ATOMIC UPDATE OF CPO STATE	MIPS TECH, LLC	09/921400	2/27/2007	7185183
READ-ONLY ACCESS TO CPO REGISTERS	MIPS TECH, LLC	09/921377	2/20/2007	7181600
CONFIGURABLE PRIORITIZATION OF CORE GENERATED INTERRUPTS	MIPS TECH, LLC	09/977089	6/23/2009	7552261
METHOD AND APPARATUS FOR CLEARING HAZARDS USING JUMP INSTRUCTIONS	MIPS TECH, LLC	10/238993	2/14/2006	7000095
METHOD AND APPARATUS FOR CLEARING HAZARDS USING JUMP INSTRUCTIONS	MIPS TECH, LLC	11/284069	5/1/2012	8171262
INSTRUCTION ENCODING FOR SYSTEM REGISTER BIT SET AND CLEAR	MIPS TECH, LLC	10/279210	12/15/2009	7634638
INSTRUCTION ENCODING FOR SYSTEM REGISTER BIT SET AND CLEAR	MIPS TECH LLC	11/567290	10/6/2009	7600100
INSTRUCTION ENCODING FOR SYSTEM REGISTER BIT SET AND CLEAR	MIPS TECH LLC	12/576942	5/29/2012	8190865
LATENCY INDEPENDENT COHERENCE PROTOCOL	MIPS TECH LLC	10/783960	1/5/2010	7644237
METHOD AND APPARATUS FOR GLOBAL ORDERING TO INSURE LATENCY INDEPENDENT COHERENCE	MIPS TECH LLC	12/557421	10/11/2011	8037253

MECHANISM FOR ASSURING QUALITY OF SERVICE FOR PROGRAMS EXECUTING ON A MULTITHREAD PROCESSOR	MIPS TECH LLC	10/684350	5/20/2008	7376954
INTEGRATED MECHANISM FOR SUSPENSION AND DEALLOCATION OF COMPUTATIONAL THREADS OF EXECUTION IN A PROCESSOR	MIPS TECH LLC	10/929342	1/22/2008	7321965
SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR CONDITIONALLY SUSPENDING ISSUING INSTRUCTION OF A THREAD	MIPS TECH LLC	11/949603	3/9/2010	7676660
METHOD AND APPARATUS FOR DYNAMIC ALLOCATION OF RESOURCES TO EXECUTING THREADS IN A MULTI-THREADED PROCESSOR	MIPS TECH LLC	10/949958	5/4/2010	7712101
MICROPROCESSOR OUTPUT PORTS AND CONTROL OF INSTRUCTIONS PROVIDED THEREFROM	MIPS TECH LLC	11/632567	9/22/2009	7594097
APPARATUS, METHOD AND INSTRUCTION FOR INITIATION OF CONCURRENT INSTRUCTION STREAMS IN A MULTITHREADING MICROPROCESSOR	MIPS TECH LLC	10/928746	10/27/2009	7610473
APPARATUS, METHOD AND INSTRUCTION FOR INITIATION OF CONCURRENT INSTRUCTION STREAMS IN A MULTITHREADING MICROPROCESSOR	MIPS TECH LLC	12/605201	3/27/2012	8145884
MECHANISMS FOR DYNAMIC CONFIGURATION OF VIRTUAL PROCESSOR RESOURCES	MIPS TECH LLC	10/929102	4/6/2010	7694304
APPARATUS, METHOD AND INSTRUCTION FOR SOFTWARE MANAGEMENT OF MULTIPLE COMPUTATIONAL CONTEXTS IN A MULTITHREADED MICROPROCESSOR	MIPS TECH LLC	10/929097	9/9/2008	7424599
SYNCHRONIZED STORAGE PROVIDING MULTIPLE SYNCHRONIZATION SEMANTICS	MIPS TECH LLC	10/954988	5/4/2010	7711931
SMART MEMORY BASED SYNCHRONIZATION CONTROLLER FOR A MULTITHREADED MICROPROCESSOR SOC	MIPS TECH LLC	10/955231	9/22/2009	7594089
INTERFACING EXTERNAL THREAD PRIORITIZING POLICY ENFORCING LOGIC WITH CUSTOMER MODIFIABLE REGISTER TO PROCESSOR INTERNAL SCHEDULER	MIPS TECH LLC	11/051997	11/3/2009	7613904
MULTITHREADING MICROPROCESSOR WITH OPTIMIZED THREAD SCHEDULER FOR INCREASING PIPELINE UTILIZATION EFFICIENCY	MIPS TECH LLC	11/051979	2/2/2010	7657891
MULTITHREADING MICROPROCESSOR WITH OPTIMIZED THREAD SCHEDULER FOR INCREASING PIPELINE UTILIZATION EFFICIENCY	MIPS TECH LLC	12/684564	4/3/2012	8151268

INSTRUCTION/SKID BUFFERS IN A MULTITHREADING MICROPROCESSOR THAT STORE DISPATCHED INSTRUCTIONS TO AVOID RE-FETCHING FLUSHED INSTRUCTIONS	MIPS TECH LLC	11/051978	12/14/2010	7853777
THREE TIERED TRANSLATION LOOKASIDE BUFFER HIERARCHY IN A MULTITHREADING MICROPROCESSOR	MIPS TECH LLC	11/075041	7/7/2009	7558939
THREE-TIERED TRANSLATION LOOKASIDE BUFFER HIERARCHY IN A MULTITHREADING MICROPROCESSOR	MIPS TECH LLC	12/495375	4/12/2011	7925859
SOFTWARE EMULATION OF DIRECTED EXCEPTIONS IN A MULTITHREADING PROCESSOR	MIPS TECH LLC	11/313272	12/7/2010	7849297
SYMMETRIC MULTIPROCESSOR OPERATING SYSTEM FOR EXECUTION ON NON-INDEPENDENT LIGHTWEIGHT THREAD CONTEXTS	MIPS TECH LLC	12/911901	9/11/2012	8266620
PREEMPTIVE MULTITASKING EMPLOYING SOFTWARE EMULATION OF DIRECTED EXCEPTIONS IN A MULTITHREADING PROCESSOR	MIPS TECH LLC	11/313296	5/12/2015	9032404
SYMMETRIC MULTIPROCESSOR OPERATING SYSTEM FOR EXECUTION ON NON-INDEPENDENT LIGHTWEIGHT THREAD CONTEXTS	MIPS TECH LLC	11/330914	8/26/2008	7418585
SYMMETRIC MULTIPROCESSOR OPERATING SYSTEM FOR EXECUTION ON NON-INDEPENDENT LIGHTWEIGHT THREAD CONTEXTS	MIPS TECH LLC	11/330916	1/11/2011	7870553
SYMMETRIC MULTIPROCESSOR OPERATING SYSTEM FOR EXECUTION ON NON-INDEPENDENT LIGHTWEIGHT THREAD CONTEXTS	MIPS TECH LLC	11/330915	11/16/2010	7836450
SYMMETRIC MULTIPROCESSOR OPERATING SYSTEM FOR EXECUTION ON NON-INDEPENDENT LIGHTWEIGHT THREAD CONTEXTS	MIPS TECH LLC	11/615960	5/25/2010	7725689
SYMMETRIC MULTIPROCESSOR OPERATING SYSTEM FOR EXECUTION ON NON-INDEPENDENT LIGHTWEIGHT THREAD CONTEXTS	MIPS TECH LLC	11/615963	5/25/2010	7725697
SYMMETRIC MULTIPROCESSOR OPERATING SYSTEM FOR EXECUTION ON NON-INDEPENDENT LIGHTWEIGHT THREAD CONTEXTS	MIPS TECH LLC	11/615964	6/1/2010	7730291
SYMMETRIC MULTIPROCESSOR OPERATING SYSTEM FOR EXECUTION ON NON-INDEPENDENT LIGHTWEIGHT THREAD CONTEXTS	MIPS TECH LLC	11/615965	3/9/2010	7676664
USER INTERFACE FOR FACILITATION OF HIGH LEVEL GENERATION OF PROCESSOR EXTENSIONS	MIPS TECH LLC	11/388484	6/23/2015	9064076
HORIZONTALLY-SHARED CACHE VICTIMS IN MULTIPLE CORE PROCESSORS	MIPS TECH LLC	11/681610	8/10/2010	7774549

HORIZONTALLY-SHARED CACHE VICTIMS IN MULTIPLE CORE PROCESSORS	MIPS TECH LLC	12/828056	5/13/2014	8725950
AVOIDING LIVELOCK USING A CACHE MANAGER IN MULTIPLE CORE PROCESSORS	MIPS TECH LLC	11/767247	6/15/2010	7739455
PRIORITISING OF INSTRUCTION FETCHING IN MICROPROCESSOR SYSTEMS	MIPS TECH LLC	12/322942	5/24/2016	9348600
PRIORITISING OF INSTRUCTION FETCHING IN MICROPROCESSOR SYSTEMS	MIPS TECH LLC	15/134510	1/16/2018	9870228
PIPELINE PROCESSORS	MIPS TECH LLC	12/383118	10/15/2013	8560813
SYSTEM FOR PROVIDING TRACE DATA IN A DATA PROCESSOR HAVING A PIPELINED ARCHITECTURE	MIPS TECH LLC	12/387152	7/8/2014	8775875
SYSTEM FOR PROVIDING TRACE DATA IN A DATA PROCESSOR HAVING A PIPELINED ARCHITECTURE	MIPS TECH LLC	14/271886	8/1/2017	9720695
MULTI-THREADED DATA PROCESSING SYSTEM	MIPS TECH LLC	13/138176	4/4/2017	9612844
METHOD AND APPARATUS FOR ENSURING DATA CACHE COHERENCY	MIPS TECH LLC	12/586649	7/31/2012	8234455
METHOD AND APPARATUS FOR ENSURING DATA CACHE COHERENCY	MIPS TECH LLC	13/555894	7/7/2015	9075724
METHOD AND APPARATUS FOR ENSURING DATA CACHE COHERENCY	MIPS TECH LLC	14/791699	7/11/2017	9703709
METHOD AND APPARATUS FOR SCHEDULING THE ISSUE OF INSTRUCTIONS IN A MULTITHREADED MICROPROCESSOR	MIPS TECH LLC	12/584759	11/17/2015	9189241
MICROPROCESSOR SYSTEM FOR VIRTUAL MACHINE EXECUTION	MIPS TECH LLC	12/891530	7/22/2014	8789042
MICROPROCESSOR WITH DUAL-LEVEL ADDRESS TRANSLATION	MIPS TECH LLC	12/891503	8/7/2012	8239620
PROCESSOR WITH KERNEL-MODE ACCESS TO USER SPACE VIRTUAL ADDRESSES	MIPS TECH LLC	13/683875	1/12/2016	9235510
RESTORING A REGISTER RENAMING MAP	MIPS TECH LLC	13/563025	9/8/2015	9128700
RESTORING A REGISTER RENAMING MAP	MIPS TECH LLC	14/816651	9/6/2016	9436470
APPARATUS AND METHOD FOR GUEST AND ROOT REGISTER SHARING IN A VIRTUAL MACHINE	MIPS TECH LLC	13/436654	7/21/2015	9086906
GLOBAL REGISTER PROTECTION IN A MULTI-THREADED PROCESSOR	MIPS TECH LLC	13/780115	3/31/2015	8996847
GLOBAL REGISTER PROTECTION IN A MULTI-THREADED PROCESSOR	MIPS TECH LLC	14/625895	8/8/2017	9727380
DYNAMICALLY RESIZABLE CIRCULAR BUFFERS	MIPS TECH LLC	13/964257	11/21/2017	9824003
UNAMBIGUOUS PREFIX INSTRUCTIONS	MIPS TECH LLC	14/722292	2/20/2018	9898293
IMPROVED CONTROL OF PRE-FETCH TRAFFIC	MIPS TECH LLC	14/153223	5/23/2017	9658962

IMPROVED MECHANISM FOR COPYING DATA IN MEMORY	MIPS TECH LLC	14/169886	2/6/2018	9886212
FILL PARTITIONING OF A SHARED CACHE	MIPS TECH LLC	14/153240	5/9/2017	9645945
REGISTER FILE HAVING A PLURALITY OF SUB-REGISTER FILES	MIPS TECH LLC	14/153240	4/5/2016	9304934
REGISTER FILE HAVING A PLURALITY OF SUB-REGISTER FILES	MIPS TECH LLC	14/157805	6/6/2017	9672039
ALLOCATING RESOURCES TO THREADS BASED ON SPECULATION METRIC	MIPS TECH LLC	14/842983	7/21/2015	9086721
ALLOCATING RESOURCES TO THREADS BASED ON SPECULATION METRIC	MIPS TECH LLC	14/157764	3/28/2017	9606834
INDIRECT BRANCH PREDICTION	MIPS TECH LLC	14/754436	3/29/2016	9298467
SPECULATIVE LOAD ISSUE	MIPS TECH LLC	14/153188	7/19/2016	9395991
SPECULATIVE LOAD ISSUE	MIPS TECH LLC	14/169601	3/6/2018	9910672
MIGRATION OF DATA TO REGISTER FILE CACHE	MIPS TECH LLC	14/189719	3/22/2016	9292450
MIGRATION OF DATA TO REGISTER FILE CACHE	MIPS TECH LLC	15/019132	4/4/2017	9612968
MIGRATION OF DATA TO REGISTER FILE CACHE	MIPS TECH LLC	15/438000	1/2/2018	9858194
INDIRECT BRANCH PREDICTION	MIPS TECH LLC	14/169771	10/17/2017	9792123
PRIORITIZING INSTRUCTIONS BASED ON TYPE	MIPS TECH LLC	14/340932	1/31/2017	9558001
STACK POINTER VALUE PREDICTION	MIPS TECH LLC	14/596407	5/16/2017	9652240
STACK SAVED VARIABLE VALUE PREDICTION	MIPS TECH LLC	14/598415	4/3/2018	9934039
AN IMPROVED RETURN STACK BUFFER	MIPS TECH LLC	14/608745	8/23/2016	9424203
AN IMPROVED RETURN STACK BUFFER	MIPS TECH LLC	14/608630	6/7/2016	9361242
WAY LOOKAHEAD	MIPS TECH LLC	13/781319	8/1/2017	9720840
RESOURCE SHARING USING PROCESS DELAY	MIPS TECH LLC	13/780197	9/15/2015	9135067
RESOURCE SHARING USING PROCESS DELAY	MIPS TECH LLC	14/837109	2/7/2017	9563476
RESOURCE SHARING USING PROCESS DELAY	MIPS TECH LLC	15/404743	4/10/2018	9940168
APPARATUS AND METHOD FOR OPERATING A PROCESSOR WITH AN OPERATION CACHE	MIPS TECH LLC	13/789443	11/17/2015	9189412
CROSSING PIPELINED DATA BETWEEN CIRCUITRY IN DIFFERENT CLOCK DOMAINS	MIPS TECH LLC	14/451279	6/14/2016	9367286
CROSSING PIPELINED DATA BETWEEN CIRCUITRY IN DIFFERENT CLOCK DOMAINS	MIPS TECH LLC	15/150177	8/22/2017	9740454
PROCESSOR WITH VIRTUALIZED INSTRUCTION SET ARCHITECTURE & METHODS	MIPS TECH LLC	14/572186	1/16/2018	9870225

PIPELINED ECC-PROTECTED MEMORY ACCESS	MIPS TECH LLC	14/612084	8/22/2017	9740557
FAULT TOLERANT PROCESSOR FOR REAL-TIME SYSTEMS	MIPS TECH LLC	14/741738	9/24/2019	10423417
CHECK POINTING A SHIFT REGISTER	MIPS TECH LLC	15/205555	7/17/2018	10025527
TRANSLATION LOOKASIDE BUFFER	MIPS TECH LLC	14/715117	11/28/2017	9830275
FAULT DETECTING AND FAULT TOLERANT MULTI-THREADED PROCESSORS	MIPS TECH, LLC	PCT/US2018/046246	8/10/2018	WO 2019/032980
INSTRUCTION SETS FOR MICROPROCESSORS	MIPS TECH, LLC	11/704725	2/9/2007	10,437,598
METHOD AND APPARATUS FOR SCHEDULING THE ISSUE OF INSTRUCTIONS IN A MULTITHREADED MICROPROCESSOR	MIPS TECH, LLC	14/930,913	11/3/2015	10,360,038
SHARED REGISTER POOL FOR A MULTITHREADED MICROPROCESSOR	MIPS TECH, LLC	13/491,781	6/8/2012	10,534,614
DECODING INSTRUCTIONS THAT ARE MODIFIED BY ONE OR MORE OTHER INSTRUCTIONS	MIPS TECH, LLC	15/874,724	1/18/2018	10379861
IMPROVED CONTROL OF PRE-FETCH TRAFFIC	MIPS TECH, LLC	15/488,649	4/17/2017	10754778
MIGRATION OF DATA TO REGISTER FILE CACHE	MIPS TECH, LLC	15/833,555	12/6/2017	10678695
PRIORITIZING INSTRUCTIONS BASED ON TYPE	MIPS TECH, LLC	15/387,394	12/21/2016	10001997
APPARATUS AND METHOD FOR BRANCH INSTRUCTION BONDING	MIPS TECH, LLC	13/789,467	3/7/2013	10,540,179
HARDWARE VIRTUALIZED INPUT OUTPUT MEMORY MANAGEMENT UNIT	MIPS TECH, LLC	14/589,693	1/5/2015	10,642,501
RUNNING A 32-BIT OPERATING SYSTEM ON A 64-BIT MACHINE	MIPS TECH, LLC	14/798,841	7/14/2015	10,048,967
PROCESSOR SUPPORTING ARITHMETIC INSTRUCTIONS WITH BRANCH ON OVERFLOW & METHODS	MIPS TECH, LLC	14/612,104	2/2/2015	10,768,930
MODELESS INSTRUCTION EXECUTION WITH 64/32-BIT ADDRESSING	MIPS TECH, LLC	14/612,090	2/2/2015	10,671,391
PROCESSORS AND METHODS FOR CACHE SPARING STORES	MIPS TECH, LLC	14/829,458	8/18/2015	10,108,548
TRANSLATION LOOKASIDE BUFFER	MIPS TECH, LLC	15/824,613	11/28/2017	10185665
VIRTUALIZED-IN-HARDWARE INPUT OUTPUT MEMORY MANAGEMENT	MIPS TECH, LLC	16/865,851	5/4/2020	2020-0264783
CHECK POINTING A SHIFT REGISTER WITH A CIRCULAR BUFFER	MIPS TECH, LLC	16/036104	5/5/2020	10,642,527
PROCESSORS SUPPORTING ATOMIC WRITES TO MULTIWORD MEMORY LOCATIONS & METHODS	MIPS TECH, LLC	15/092915	5/12/2020	10,073,773
FETCH AHEAD BRANCH TARGET BUFFER	MIPS TECH, LLC	14/935579	5/26/2020	10,664,280
FETCH UNIT FOR PREDICTING TARGET FOR SUBROUTINE RETURN INSTRUCTIONS	MIPS TECH, LLC	15/281661	7/23/2019	10,360,037
EXECUTION OF LOAD INSTRUCTIONS IN A PROCESSOR	MIPS TECH, LLC	15/001628	10/29/2019	10,459,725

FETCHING INSTRUCTIONS IN AN INSTRUCTION FETCH UNIT	MIPS TECH, LLC	15/624121	8/6/2019	10,372,453
FAULT DETECTING AND FAULT TOLERANT MULTI-THREADED PROCESSORS	MIPS TECH, LLC	16/100,706	9/22/2020	10,782,977
IMPLICIT GLOBAL POINTER RELATIVE ADDRESSING FOR GLOBAL MEMORY ACCESS	MIPS TECH, LLC	16/119,291	8/31/2018	2019-0065201
UNIFIED LOGIC FOR ALIASED PROCESSOR INSTRUCTIONS	MIPS TECH, LLC	16/119,487	11/24/2020	10,846,089
PROCESSOR ARRAY REDUNDANCY	MIPS TECH, LLC	16/522,429	7/25/2019	2020-0034262
NEURAL NETWORK PROCESSING USING SPECIALIZED DATA REPRESENTATION	MIPS TECH, LLC	16/704,263	12/5/2019	2020-0184309
NEURAL NETWORK PROCESSING USING SPECIALIZED DATA REPRESENTATION	MIPS TECH, LLC	PCT/US19/64677	12/5/2019	WO 2020/118051 published
ADDRESS MANIPULATION USING INDICES AND TAGS	MIPS TECH, LLC	16/739,540	1/10/2020	2020-0225955
ADDRESS MANIPULATION USING INDICES AND TAGS	MIPS TECH, LLC	PCT/US20/13075	1/10/2020	WO 2020/146724 published
NEURAL NETWORK PROCESSING USING MIXED-PRECISION DATA REPRESENTATION	MIPS TECH, LLC	16/778,258	1/31/2020	2020-0202195
NEURAL NETWORK DATA COMPUTATION USING MIXED-PRECISION	MIPS TECH, LLC	16/985,307	8/5/2020	2021-0034979
SAVING AND RESTORING NON-CONTIGUOUS BLOCKS OF PRESERVED REGISTERS	MIPS Tech, LLC	PCT/US18/49128	8/31/2018	WO 2019/046742
MULTI-THRESHOLD FLASH NCL CIRCUITRY	Wave Computing, Inc.	13/772,759	5/5/2015	9024655
MULTI-THRESHOLD FLASH NCL LOGIC CIRCUITRY WITH FLASH RESET	Wave Computing, Inc.	14/703,483	7/5/2016	9385715
SELF-READY FLASH NULL CONVENTION LOGIC	Wave Computing, Inc.	13/827,902	3/17/2015	8981812
IMPLEMENTATION METHOD FOR FAST NCL DATA PATH	Wave Computing, Inc.	13/894,072	12/1/2015	9203406
HUM GENERATION CIRCUITRY	Wave Computing, Inc.	13/969,675	2/10/2015	8952727
EXTENSIBLE ITERATIVE MULTIPLIER	Wave Computing, Inc.	14/099,949	2/7/2017	9563401
SELECTIVELY COMBINABLE SHIFTERS	Wave Computing, Inc.	14/136,754	4/3/2018	9933996
SELECTIVELY COMBINABLE DIRECTIONAL SHIFTERS	Wave Computing, Inc.	15/941,826	5/14/2019	10,289,382
COMPUTING RESOURCE ALLOCATION BASED ON FLOW GRAPH TRANSLATION	Wave Computing, Inc.	14/928,314	8/7/2018	10,042,966
MULTI-THRESHOLD CIRCUITRY BASED ON SILICON-ON-INSULATOR TECHNOLOGY	Wave Computing, Inc.	14/487,678	9/16/2014	9257984
LOGICAL ELEMENTS WITH SWITCHABLE CONNECTIONS	Wave Computing, Inc.	14/530,624	3/7/2017	9590629

LOGICAL ELEMENTS WITH SWITCHABLE CONNECTIONS FOR MULTIFUNCTION OPERATION	Wave Computing, Inc.	15/443,612	2/26/2019	10218357
LOGICAL ELEMENTS WITH SWITCHABLE CONNECTIONS IN A RECONFIGURABLE FABRIC	Wave Computing, Inc.	16/176,922	10/31/2018	10,374,605
COMPACT LOGIC EVALUATION GATES USING NULL CONVENTION	Wave Computing, Inc.	14/941,554	6/27/2017	9692419
INSTRUCTION PAGING IN RECONFIGURABLE FABRIC	Wave Computing, Inc.	15/048,983	9/11/2018	10073773
BRANCHLESS INSTRUCTION PAGING IN RECONFIGURABLE FABRIC	Wave Computing, Inc.	16/126,107	9/10/2018	10437728
DATA EN-QUEUING USING CIRCULAR BUFFER CONTROL	Wave Computing, Inc.	15/202,721	7/6/2016	
HUM GENERATION USING REPRESENTATIVE CIRCUITRY	Wave Computing, Inc.	15/475,411	5/1/2018	9960771
DATA UPLOADING TO ASYNCHRONOUS CIRCUITRY USING CIRCULAR BUFFER CONTROL	Wave Computing, Inc.	15/225,768	8/1/2016	10,505,704
DYNAMIC CONFIGURATION OF A RECONFIGURABLE HUM FABRIC	Wave Computing, Inc.	15/941,741	3/30/2018	2018-0225403
TIMING ANALYSIS AND OPTIMIZATION OF ASYNCHRONOUS CIRCUIT DESIGNS	Wave Computing, Inc.	15/628,307	6/11/2019	10318691
SOFTWARE BASED APPLICATION SPECIFIC INTEGRATED CIRCUIT	Wave Computing, Inc.	14/149,009	3/7/2017	9588773
POWER CONTROL WITHIN A DATAFLOW PROCESSOR	Wave Computing, Inc.	15/667,338	2/12/2019	10203935
POWER CONTROL FOR A DATAFLOW PROCESSOR	Wave Computing, Inc.	16/272,039	2/11/2019	10656911
COMMUNICATION BETWEEN DATAFLOW PROCESSING UNITS AND MEMORIES	Wave Computing, Inc.	15/665,631	8/1/2017	10564929
DATA TRANSFER CIRCUITRY GIVEN MULTIPLE SOURCE ELEMENTS	Wave Computing, Inc.	15/226,472	8/2/2016	10374981
RECONFIGURABLE FABRIC DIRECT MEMORY ACCESS WITH MULTIPLE READ OR WRITE ELEMENTS	Wave Computing, Inc.	15/712,494	9/22/2017	10719470
RECONFIGURABLE INTERCONNECTED PROGRAMMABLE PROCESSORS	Wave Computing, Inc.	15/449,852	3/3/2017	10,592,444
RECONFIGURABLE PROCESSOR FABRIC IMPLEMENTATION USING SATISFIABILITY ANALYSIS	Wave Computing, Inc.	15/953,896	4/16/2018	10452452
JOINING DATA WITHIN A RECONFIGURABLE FABRIC	Wave Computing, Inc.	16/021,840	6/28/2018	10659396
JOINING DATA WITHIN A RECONFIGURABLE FABRIC	Wave Computing, Inc.	PCT/US18/40009	6/28/2018	WO 2019/006119
REMOTE USAGE OF MACHINE LEARNED LAYERS BY A SECOND MACHINE LEARNING CONSTRUCT	Wave Computing, Inc.	16/051,792	8/1/2018	2019-0042918
RECONFIGURABLE FABRIC OPERATION LINKAGE	Wave Computing, Inc.	16/054,225	8/3/2018	2019-0042941
RECONFIGURABLE FABRIC OPERATION LINKAGE	Wave Computing, Inc.	PCT/US18/45150	8/3/2018	WO 2019/032396
RECONFIGURABLE FABRIC DATA ROUTING	Wave Computing, Inc.	16/104,586	8/17/2018	2019-0057060

RECONFIGURABLE FABRIC DATA ROUTING	Wave Computing, Inc.	PCT/US18/46 932	8/17/2018	WO 2019/040339
TENSOR MANIPULATION WITHIN A NEURAL NETWORK	Wave Computing, Inc.	16/170,268	10/25/2018	2019-0130276
PIPELINED TENSOR MANIPULATION WITHIN A RECONFIGURABLE FABRIC	Wave Computing, Inc.	16/208,928	12/4/2018	2019-0130269
PIPELINED TENSOR MANIPULATION WITHIN A RECONFIGURABLE FABRIC	Wave Computing, Inc.	PCT/US18/63 762	12/4/2018	WO 2019/113007
DYNAMIC RECONFIGURATION WITH PARTIALLY RESIDENT AGENTS	Wave Computing, Inc.	16/228,882	12/21/2018	2019-0130291
TENSOR MANIPULATION WITHIN A RECONFIGURABLE FABRIC USING POINTERS	Wave Computing, Inc.	16/208,991	12/4/2018	2019-0130270
TENSOR MANIPULATION WITHIN A RECONFIGURABLE FABRIC USING POINTERS	Wave Computing, Inc.	PCT/US18/63 782	12/4/2018	WO 2019/113021
TENSOR RADIX POINT CALCULATION IN A NEURAL NETWORK	Wave Computing, Inc.	16/174,786	10/30/2018	2019-0130268
TENSOR RADIX POINT CALCULATION IN A NEURAL NETWORK	Wave Computing, Inc.	PCT/US18/58 162	10/30/2018	2019-0130268
MULTITHREADED DATA FLOW PROCESSING WITHIN A RECONFIGURABLE FABRIC	Wave Computing, Inc.	16/234,728	12/28/2018	2019-0138373
MATRIX COMPUTATION WITHIN A RECONFIGURABLE PROCESSOR FABRIC	Wave Computing, Inc.	16/286,891	2/27/2019	2019-0266218
DYNAMIC RECONFIGURATION USING DATA TRANSFER CONTROL	Wave Computing, Inc.	16/289,814	3/1/2019	2019-0197018
DYNAMIC RECONFIGURATION USING DATA TRANSFER CONTROL	Wave Computing, Inc.	PCT/US19/20 231	3/1/2019	WO 2019/169238
DATA FLOW GRAPH COMPUTATION FOR MACHINE LEARNING	Wave Computing, Inc.	16/369,134	3/29/2019	2019-0228340 published
DATA FLOW GRAPH COMPUTATION FOR MACHINE LEARNING	Wave Computing, Inc.	PCT/US19/24 820	3/29/2019	WO 2019/191578 published
CHECKPOINTING DATA FLOW GRAPH COMPUTATION FOR MACHINE LEARNING	Wave Computing, Inc.	16/369,079	3/29/2019	2019-0228037 published
DATA FLOW GRAPH NODE UPDATE FOR MACHINE LEARNING	Wave Computing, Inc.	16/423,051	5/27/2019	2019-0279086 published
NEURAL NETWORK OUTPUT LAYER FOR MACHINE LEARNING	Wave Computing, Inc.	16/459,731	7/2/2019	2019-0325309 published
DATA FLOW GRAPH NODE PARALLEL UPDATE FOR MACHINE LEARNING	Wave Computing, Inc.	16/423,050	5/27/2019	2019-0279038 published
DATA FLOW GRAPH COMPUTATION USING EXCEPTIONS	Wave Computing, Inc.	16/502,110	9/10/2018	2019-0324888
RECONFIGURABLE FABRIC CONFIGURATION USING SPATIAL AND TEMPORAL ROUTING	Wave Computing, Inc.	16/697,571	5/28/2020	2020-0167309
FIFO FILLING LOGIC FOR TENSOR CALCULATION	Wave Computing, Inc.	16/784,363	2/27/2020	2020-0174707

MATRIX MULTIPLICATION ENGINE USING PIPELINING	Wave Computing, Inc.	16/835,812	3/31/2020	2020-0311183
INTEGER MATRIX MULTIPLICATION ENGINE USING PIPELINING	Wave Computing, Inc.	16/943,252	7/30/2020	2020-038756
MULTIDIMENSIONAL ADDRESS GENERATION FOR DIRECT MEMORY ACCESS	Wave Computing, Inc.	16/991,080	8/12/2020	2020-0371978
PROCESSOR CLUSTER ADDRESS GENERATION	Wave Computing, Inc.	17/035,869	9/29/2020	2021-0011849

EXHIBIT C

Trademarks

Title	Owner/Applicant	Registration / Application No.	Registration / Application Date
CODESCAPE	Imagination Technologies Limited	2107854	10/21/1997
MEOS	Imagination Technologies Limited	3065000	3/7/2006
MICROMIPS	MIPS Tech, LLC	3928894	3/8/2011
MIPS	MIPS Tech, LLC	3255604	6/26/2007
MIPS	MIPS Tech, LLC	1734429	11/24/1992
MIPS	MIPS Tech, LLC	1493963	6/28/1988
MIPS	MIPS Tech, LLC	2896003	10/19/2004
MIPS32	MIPS Tech, LLC	2800581	12/30/2003
MIPS32	MIPS Tech, LLC	2883124	9/7/2004
MIPS64	MIPS Tech, LLC	2968237	7/12/2005
MIPS64	MIPS Tech, LLC	2764564	9/16/2003
WARRIOR	Imagination Technologies Ltd	4957744	5/17/2016
WAVE COMPUTING	Wave Computing, Inc.	5402116	2/13/2018
WAVE SEMI (and Design)	Wave Computing, Inc.	4913985	3/8/2016