TRADEMARK ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

ETAS ID: TM641064

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST
SEQUENCE:	1

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
Avalanche Technology, Inc.		04/08/2021	Corporation: DELAWARE

RECEIVING PARTY DATA

Name:	Structured Alpha LP
Street Address:	65 Queen Street West
Internal Address:	Suite 2400
City:	Toronto,Ontario
State/Country:	CANADA
Postal Code:	M5H 2M8
Entity Type:	Corporation: CAYMAN ISLANDS

PROPERTY NUMBERS Total: 4

Property Type	Number	Word Mark
Registration Number:	4198751	AVALANCHE TECHNOLOGY
Registration Number:	4237990	AVALANCHE
Registration Number:	4946647	AVA
Serial Number:	88196128	A

OP $115.00 4198751

CORRESPONDENCE DATA

Fax Number: 2123553333

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 2128138800
Email: NY-TM-Admin@goodwinprocter.com
Correspondent Name: Goodwin Procter LLC/Janis Nici
Address Line 1: 620 Eighth Avenue
Address Line 4: New York, NEW YORK 10018

NAME OF SUBMITTER:	Janis Nici
SIGNATURE:	/janis nici/
DATE SIGNED:	04/21/2021

Total Attachments: 24

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EXECUTION VERSION

INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement ("Agreement") is entered into as of the April 8, 2021 by and between STRUCTURED ALPHA LP, as collateral agent for the Purchasers under the Purchase Agreement referred to below (in such capacity, "Secured Party"), and AVALANCHE TECHNOLOGY, INC. ("Grantor").

RECITALS

A. Secured Party, Grantor and the other purchasers party thereto are parties to that certain Note Purchase Agreement dated as of as of the date hereof, between Secured Party and Grantor (as may be further amended, restated, supplemented, or otherwise modified from time to time, the "Purchase Agreement"; capitalized terms used herein are used as defined in the Purchase Agreement or the Security Agreement (as defined in the Purchase Agreement), as applicable).

B. Pursuant to the terms of the Security Agreement, Grantor has granted to Secured Party a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its Obligations under the Purchase Agreement and the Notes, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

1. Grant of Security Interest. To secure its obligations under the Purchase Agreement, including, without limitation, the Obligations, Grantor grants and pledges to Secured Party a security interest in all of Grantor's right, title and interest in, to and under its intellectual property (all of which shall collectively be called the "Intellectual Property Collateral"), including, without limitation, the following:

(a) Any and all copyright rights, copyright applications, copyright registrations and like protections in each work or authorship and derivative work thereof, whether published or unpublished and whether or not the same also constitutes a trade secret, now or hereafter existing, created, acquired or held, including without limitation those set forth on Exhibit A attached hereto (collectively, the "Copyrights");

(b) Any and all trade secrets, and any and all intellectual property rights in computer software and computer software products now or hereafter existing, created, acquired or held;

(c) Any and all design rights that may be available to Grantor now or hereafter existing, created, acquired or held;

(d) All patents, patent applications and like protections including, without limitation, improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the same, including without limitation the patents and patent applications set forth on Exhibit B attached hereto (collectively, the "Patents");

(e) Any trademark and servicemark rights, whether registered or not, applications to register and registrations of the same and like protections, and the entire goodwill of the business of Grantor connected with and symbolized by such trademarks, including without limitation those set forth on Exhibit C attached hereto, but excluding any intent-to-use trademarks at all times prior to the first use thereof, whether by the actual use thereof in commerce, the recording of a statement of use with the United States Patent and Trademark Office or otherwise (collectively, the "Trademarks");

(f) All mask works or similar rights available for the protection of semiconductor chips, now owned or hereafter acquired, including, without limitation those set forth on Exhibit D attached hereto (collectively, the "Mask Works");

(g) Any and all claims for damages by way of past, present and future infringements of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above;

(h) All licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works (other than licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works granted in the ordinary course of Grantor's business);

(i) All license fees and royalties arising from the use of any of the Copyrights, Patents, Trademarks, or Mask Works to the extent permitted by such license or rights;

(j) All amendments, extensions, renewals and extensions of any of the Copyrights, Trademarks, Patents, or Mask Works; and

(k) All proceeds and products of the foregoing, including without limitation all payments under insurance or any indemnity or warranty payable in respect of any of the foregoing.

2. Recordation. Grantor authorizes the Commissioner for Patents, the Commissioner for Trademarks and the Register of Copyrights and any other government officials to record and register this Agreement with the United States Patent and Trademark Office, the United States Copyright Office or any other governmental agency or office providing for the registering or perfection of security interests in any Intellectual Property Collateral, as applicable, upon request by Secured Party.

3. Authorization. Grantor hereby authorizes Secured Party to (a) modify this Agreement unilaterally by amending the exhibits to this Agreement to include any Intellectual Property Collateral which Grantor obtains subsequent to the date of this Agreement, and (b) file a duplicate original of this Agreement containing amended exhibits reflecting such new Intellectual Property Collateral.

4. Transaction Documents. This Agreement has been entered into pursuant to and in conjunction with the Purchase Agreement and the Security Agreement, which are hereby incorporated by reference. The provisions of the Purchase Agreement and the Security Agreement shall supersede and control over any conflicting or inconsistent provision herein. The rights and remedies of Security Party with respect to the Intellectual Property Collateral are as provided by the Purchase Agreement, the Security Agreement and related documents, and nothing in this Agreement shall be deemed to limit such rights and remedies.

5. Execution in Counterparts. This Agreement may be executed in counterparts (and by different parties hereto in different counterparts), each of which shall constitute an original, but all of which when taken together shall constitute a single contract. Delivery of an executed counterpart of a signature page to this Agreement by facsimile or in electronic (i.e., "pdf" or "tif" format) shall be effective

as delivery of a manually executed counterpart of this Agreement. The words "execution," "signed," "signature" and words of like import herein shall be deemed to include electronic signatures or the keeping of records in electronic form, each of which shall be of the same legal effect, validity and enforceability as a manually executed signature or the use of a paper-based recordkeeping systems, as the case may be, to the extent and as provided for in any applicable law, including, without limitation, any state law based on the Uniform Electronic Transactions Act.

6. Successors and Assigns. This Agreement will be binding on and shall inure to the benefit of the parties hereto and their respective successors and assigns.

7. Governing Law. This Agreement and any claim, controversy, dispute or cause of action (whether in contract or tort or otherwise) based upon, arising out of or relating to this Agreement and the transactions contemplated hereby and thereby shall be governed by, and construed in accordance with, the laws of the United States and the State of California, without giving effect to any choice or conflict of law provision or rule (whether of the State of California or any other jurisdiction).

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

AVALANCHE TECHNOLOGY, INC.

By: _____
Name: Petro Estakhri
Title: President and Chief Executive Officer

Address: 3450 West Warren Avenue
Fremont, CA 94538

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

SECURED PARTY:

STRUCTURED ALPHA LP

By: Thomvest Asset Management, Inc.,
its General Partner

By: _____
Name: Eugene Siklos
Title: Authorized Signatory

EXHIBIT A

Copyrights

Description	Registration/ Application Number	Registration/ Application Date
None.		

EXHIBIT B

Patents

Patent Applications

	Application Number	Filing Date	Title	Status
1	13/737,897	1/9/2013	MEMORY SYSTEM HAVING THERMALLY STABLE PERPENDICULAR MAGNETO TUNNEL JUNCTION (MTJ) AND A METHOD OF MANUFACTURING SAME	Pending
2	16/550,103	8/23/2019	Magnetic Memory Emulating Dynamic Randomn Access Memoy (DRAM)	Pending
3	16/024,601	2/18/2020	Megnetic memory array incoporating selectors and method for manufucting the same	Pending - On Appeal
4	16/793,349	2/18/2020	Magnetic Memory Cell Including Two-Terminal Selector Device	Pending
5	16/836,922		Bidirectional Selector Device for Memory Applications	Unpublished.
6	16/900,470		Locally Timed Sensing of Memory Device	Unpublished.
7	17/031,542		Memory Sensing Circuit and Method for Using the Same	Unpublished
8	17/064,880		Memory Sensing Circuit and Method for Using the Same	Unpublished
9	17/156,562	1/23/2021	Magnetic Memory Element Incorporating Dual Perpendicular Enhancement Layers	Pending
10	17/175,663	2/13/2021	Multilayered Seed for Perpendicular Magnetic Structure	Pending

Registered Patents

	Patent #	Date Issued	Title
1	10,177,308	1/8/2019	Method for Manufacturing Magntic Memory Cells
2	10,153,017	12/11/2018	Method for Sensing Memory Element Coupled to Selector Device
3	10,127,960	11/13/2018	Transient Sensing of Memory Cells
4	10,108,542	10/23/2018	Serial Link Storage Interface (SLSI) Hybrid Block Storage
5	10,101,924	10/16/2018	STORAGE PROCESSOR MANAGING NVME LOGICALLY ADDRESSED SOLID STATE DISK ARRAY
6	10,090,456	10/2/2018	Megnetic Random Access memory having perpendicluar Enhancement layer
7	10,079,338	9/18/2018	Megnetic Random Access memory having perpendicluar Enhancement layer
8	10,050,083	8/14/2018	Magnetic Random Access Memory with Mulitilayered seed structure
9	10,042,758	8/7/2018	STORAGE SYSTEM EMPLOYING MRAM AND ARRAY OF SOLID STATE DISKS WITH INTEGRATED SWITCH
10	10,037,272	7/31/2018	STORAGE SYSTEM EMPLOYING MRAM AND ARRAY OF SOLID STATE DISKS WITH INTEGRATED SWITCH
11	10,032,979	7/24/2018	Magnetic Random Access Memory with Perpenduicluar Enhancement layer
12	10,008,663	6/26/2018	Perpendicular Magnetic Fixed layer with high Anisotropy
13	10,008,540	6/26/2018	SPIN-ORBITRONICS DEVICE AND APPLICATIONS THEREOF
14	9,921,782	3/20/2018	Memory Device for Emulating Dynamic Random Access Memory (DRAM)
15	9,911,482	3/6/2018	METHOD AND APPARATUS FOR ADJUSTMENT OF CURRENT THROUGH AMAGNETORESISTIVE TUNNEL JUNCTION (MTJ) BASED ON TEMPERATURE FLUCTUATIONS
16	9,898,204	2/20/2018	MAGNETIC RANDOM ACCESS MEMORY WITH DYNAMIC RANDOM ACCESS MEMORY (DRAM)-LIKE INTERFACE
17	9,871,191	1/16/2018	MAGNETIC RANDOM ACCESS MEMORY WITH ULTRATHIN REFERENCE LAYER
18	9,871,190	1/16/2018	MAGNETIC RANDOM ACCESS MEMORY WITH ULTRATHIN REFERENCE LAYER
19	9,858,977	1/2/2018	Fast Programming of Magnetic Random Access Memory (MRAM)
20	9,831,421	11/28/2017	MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR ENHANCEMENT LAYER
21	9,830,106	11/28/2017	Management of Memory Array with Magnetic Random Access Memory (MRAM)
22	9,824,050	11/21/2017	A SHARED PERIPHERAL COMPONENT INTERCONNECT EXPRESS (PCIE) END POINT SYSTEM WITH A PCIe SWITCH AND METHOD FOR INITIALIZING THE SAME
23	9,812,499	11/7/2017	Memory Device Incorporating selector element with mulitple thresholds
24	9,793,319	10/17/2017	Multilayered Seed Structure for Perpendicular MTJ Memory Element

	Patent #	Date Issued	Title
25	9,793,318	10/17/2017	LANDING PAD IN PERIPHERAL CIRCUIT FOR MAGNETIC RANDOM ACCESS MEMORY (MRAM)
26	9,793,003	10/17/2017	Programming of Non-Volatile Memory Subjected to High Temperature Exposure
27	9,792,073	10/17/2017	A METHOD OF LUN MANAGEMENT IN A SOLID STATE DISK ARRAY
28	9,792,047	10/17/2017	STORAGE PROCESSOR MANAGING SOLID STATE DISK ARRAY
29	9,786,344	10/10/2017	Programming of Magnetic Random Access Memory (MRAM) By Boosting gate voltage
30	9,780,300	10/3/2017	MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR ENHANCEMENT LAYER
31	9,748,471	8/29/2017	MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR ENHANCEMENT LAYER
32	9,728,240	8/8/2017	Pulse programming techniques ofr voltage-controlled magnetroesistive tunnel junction (MTJ)
33	9,727,245	8/8/2017	A METHOD AND APPARATUS FOR DE-DUPLICATION FOR SOLID STATE DISKs (SSDs)
34	9,691,464	6/27/2017	Fast Programming of Magnetic Random Access Memory (MRAM)
35	9,679,625	6/13/2017	PERPENDICULAR MAGNETIC TUNNEL JUNCTION (pMTJ) WITH IN-PLANE MAGNETO- STATIC SWITCHING-ENHANCING LAYER
36	9,658,859	5/23/2017	METHOD OF IMPLEMENTING MAGNETIC RANDOM ACCESS MEMORY (MRAM) FOR SYSTEM BOOT
37	9,658,780	5/23/2017	MAGNETIC RANDOM ACCESS MEMORY WITH DYNAMIC RANDOM ACCESS MEMORY (DRAM)-LIKE INTERFACE
38	9,652,386	5/16/2017	MANAGEMENT OF MEMORY ARRAY WITH MAGNETIC RANDOM ACCESS MEMORY (MRAM)
39	9,647,202	5/9/2017	MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR ENHANCEMENT LAYER
40	9,647,032	5/9/2017	SPIN-ORBITRONICS DEVICE AND APPLICATIONS THEREOF
41	9,646,668	5/9/2017	Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) With Enhanced Write Current
42	9,634,244	4/25/2017	MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER AND THIN REFERENCE LAYER
43	9,627,438	4/18//17	Three Dimensional Memory Arrays and stitching there of
44	9,608,038	3/28/2017	MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER AND THIN REFERENCE LAYER
45	9,607,676	3/28/2017	METHOD AND APPARATUS FOR ADJUSTMENT OF CURRENT THROUGH AMAGNETORESISTIVE TUNNEL JUNCTION (MTJ) BASED ON TEMPERATURE FLUCTUATIONS
46	9,559,144	1/31/2017	MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER

	Patent #	Date Issued	Title
47	9,558,802	1/31/2017	Fast Programming of Magnetic Random Access Memory (MRAM)
48	9,548,448	1/17/2017	MEMORY DEVICE WITH INCREASED SEPARATION BETWEEN MEMORY ELEMENTS
49	9,548,334	1/17/2017	MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER AND THIN REFERENCE LAYER
50	9,543,506	1/10/2017	MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER
51	9,530,479	12/27/2016	Method and Apparatus of increase the reliablity of an Access Transistor Coupled to a Magnetic Tunnel Junction (MTJ)
52	9,520,174	12/13/2016	METHOD AND APPARATUS FOR PROGRAMMING A MAGNETIC TUNNEL JUNCTION (MTJ)
53	9,502,092	11/22/2016	Unipolar-Switching Perpendicular MRAM And Method for Using Same
54	9,496,489	11/15/2016	MAGNETIC RANDOM ACCESS MEMORY WITH MULTILAYERED SEED STRUCTURE
55	9,478,279	10/25/2016	AN IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY
56	9,472,595	10/18/2016	Perpendicular MRAM with Magnet
57	9,444,039	9/13/2016	SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR MAGNETIC ANISOTROPY MULTILAYERS
58	9,444,038	9/13/2016	MAGNETIC RANDOM ACCESS MEMORY WITH MULTILAYERED SEED STRUCTURE
59	9,443,577	9/13/2016	VOLTAGE-SWITCHED MAGNETIC RANDOM ACCESS MEMORY (MRAM) AND METHOD FOR USING THE SAME
60	9,419,210	8/16/2016	SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR MAGNETIC ANISOTROPY MULTILAYERS
61	9,419,207	8/16/2016	MAGNETIC RANDOM ACCESS MEMORY WITH MULTILAYERED SEED STRUCTURE
62	9,401,194	7/26/2016	Fast Programming of Magnetic Random Access Memory (MRAM)
63	9,396,783	7/19/2016	MAGNETIC RANDOM ACCESS MEMORY WITH DYNAMIC RANDOM ACCESS MEMORY (DRAM)-LIKE INTERFACE
64	9,396,781	7/19/2016	MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER
65	9,373,663	6/21/2016	LANDING PAD IN PERIPHERAL CIRCUIT FOR MAGNETIC RANDOM ACCESS MEMORY (MRAM)
66	9,349,941	5/24/2016	SSTRAM element having multiple perpendicular MTJS Coupled in series
67	9,349,427	5/24/2016	METHOD FOR SCREENING ARRAYS OF MAGNETIC MEMORIES
68	9,343,134	5/17/2016	METHOD AND APPARATUS FOR INCREASING THE RELIABILITY OF AN ACCESS TRANSITOR COUPLED TO A MAGNETIC TUNNEL JUNCTION (MTJ)

	Patent #	Date Issued	Title
69	9,337,417	5/10/2016	MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR INTERFACIAL ANISOTROPY
70	9,337,413	5/10/2016	AN IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY
71	9,319,387	4/19/2016	SECURE SPIN TORQUE TRANSFER MAGNETIC RANDOM ACCESS MEMORY (STTMRAM)
72	9,318,179	04/192016	SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR MAGNETIC ANISOTROPY MULTILAYERS
73	9,317,206	4/19/2016	HOST-MANAGED LOGICAL MASS STORAGE DEVICE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)
74	9,311,232	4/12/2016	MANAGEMENT OF MEMORY ARRAY WITH MAGNETIC RANDOM ACCESS MEMORY (MRAM)
75	9,306,154	4/5/2016	MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR ENHANCEMENT LAYER
76	9,305,626	4/5/2016	A METHOD AND APPARATUS FOR READING A MAGNETIC TUNNEL JUNCTION USING A SEQUENCE OF SHORT PULSES
77	9,252,187	2/2/2016	DEVICES AND METHODS FOR MEASUREMENT OF MAGNETIC CHARACTERISTICS OF MRAM WAFERS USING MAGNETORESISTIVE TEST STRIPS
78	9,251,882	2/2/2016	MAGNETIC RANDOM ACCESS MEMORY WITH DYNAMIC RANDOM ACCESS MEMORY (DRAM)-LIKE INTERFACE
79	9,251,879	2/2/2016	INITIALIZATION METHOD OF A PERPENDICULAR MAGNETIC RANDOM ACCESS MEMORY (MRAM) DEVICE WITH A STABLE REFERENCE CELL
80	9,251,059	2/2/2016	Storage System Employing MRAM and Redundant Array of Solid State Disk
81	9,231,027	1/5/2016	MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER AND INTERFACIAL ANISOTROPIC FREE LAYER
82	9,229,892	1/5/2016	A SHARED PERIPHERAL COMPONENT INTERCONNECT EXPRESS (PCIE) END POINT SYSTEM WITH A PCIe SWITCH AND METHOD FOR INITIALIZING THE SAME
83	9,224,504	12/29/2015	MAPPING OF RANDOM DEFECTS IN A MEMORY DEVICE
84	9,218,866	12/22/2015	High capacity low cost muliti state magnetic memory
85	9,213,495	12/15/2015	CONTROLLER MANAGEMENT OF MEMORY ARRAY OF STORAGE DEVICE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)
86	9,209,390	12/8/2015	MEMORY DEVICE HAVING STITCHED ARRAYS OF 4 F^2 MEMORY CELLS
87	9,196,332	11/24/2015	ERPENDICULAR MAGNETIC TUNNEL JUNCTION (pMTJ) WITH IN-PLANE MAGNETO- STATIC SWITCHING-ENHANCING LAYER
88	9,166,154	10/20/2015	MTJ STACK AND BOTTOM ELECTRODE PATTERNING PROCESS WITH ION BEAM ETCHING USING A SINGLE MASK

	Patent #	Date Issued	Title
89	9,166,146	10/20/2015	ELECTRIC FIELD ASSISTED MRAM AND METHOD FOR USING THE SAME
90	9,166,143	10/20/2015	MAGNETIC RANDOM ACCESS MEMORY WITH MULTIPLE FREE LAYERS
91	9,158,623	10/13/2015	Flash subsystem organized into pairs of upper and lower page location
92	9,142,755	9/22/2015	PERPENDICULAR MAGNETIC RANDOM ACCESS MEMORY (MRAM) DEVICE WITH A STABLE REFERENCE CELL
93	9,123,575	9/1/2015	SEMICONDUCTOR MEMORY DEVICE HAVING INCREASED SEPARATION BETWEEN MEMORY ELEMENTS
94	9,117,532	8/25/2015	APPARATUS FOR INITIALIZING PERPENDICULAR MRAM DEVICE
95	9,112,051	8/18/2015	THREE-DIMENSIONAL FLASH MEMORY DEVICE
96	9,105,343	8/11/2015	MULTI-LEVEL CELLS AND METHOD FOR USING THE SAME
97	9,087,562	7/21/2015	NON-VOLATILE BLOCK STORAGE MODULE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)
98	9,083,382	7/14/2015	MEMORY WITH ON-CHIP ERROR CORRECTION
99	9,082,951	7/14/2015	MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR ENHANCEMENT LAYER
100	9,082,695	7/14/2015	VIALESS MEMORY STRUCTURE AND MEHTOD OF MANUFACTURING SAME
101	9,081,669	7/14/2015	A HYBRID NON-VOLATILE MEMORY DEVICE
102	9,070,869	6/30/2015	FABRICATION METHOD USING THINNER HARD MASK FOR HIGH-DENSITY MRAM
103	9,070,855	6/30/2015	MAGNETIC RANDOM ACCESS MEMORY HAVING PERPENDICULAR ENHANCEMENT LAYER
104	9,070,692	6/30/2015	SHIELDS FOR MAGNETIC MEMORY CHIP PACKAGES
105	9,070,464	6/30/2015	MAGNETIC RANDOM ACCESS MEMORY (MRAM) WITH ENHANCED MAGNETIC STIFFNESS AND METHOD OF MAKING SAME
106	9,070,458	6/30/2015	METHOD AND APPARATUS FOR PROGRAMMING A MAGNETIC TUNNEL JUNCTION (MTJ)
107	9,058,257	6/16/2015	PERISTENT BLOCK STORAGE ATTACHED TO MEMORY BUS
108	9,054,298	6/9/2015	MAGNETIC RANDOM ACCESS MEMORY (MRAM) WITH ENHANCED MAGNETIC STIFFNESS AND METHOD OF MAKING SAME
109	9,047,968	6/2/2015	A HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY
110	9,037,787	5/19/2015	A COMPUTER SYSTEM WITH PHYSICALLY-ADDRESSABLE SOLID STATE DISK (SSD) AND A METHOD OF ADDRESSING THE SAME
111	9,037,786	5/19/2015	STORAGE SYSTEM EMPLOYING MRAM AND ARRAY OF SOLID STATE DISKS WITH INTEGRATED SWITCH

	Patent #	Date Issued	Title
112	9,030,866	5/12/2015	INITIALIZATION METHOD OF A PERPENDICULAR MAGNETIC RANDOM ACCESS MEMORY (MRAM) DEVICE
113	9,029,824	5/12/2015	Memroy deive having stitiched arrays of 4 F.sup.2 memory cells
114	9,029,822	5/12/2015	HIGH DENSITY RESISTIVE MEMORY HAVING A VERTICAL DUAL CHANNEL TRANSISTOR
115	9,028,910	5/12/2015	MTJ MANUFACTURING METHOD UTILIZING IN-SITU ANNEALING AND ETCH BACK
116	9,025,371	5/5/2015	A Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) with Perpendicular Laminated Free layer
117	9,024,398	05//05/15	PERPENDICULAR STTMRAM DEVICE WITH BALANCED REFERENCE LAYER
118	9,019,758	4/28/2015	SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY WITH PERPENDICULAR MAGNETIC ANISOTROPY MULTILAYERS
119	9,013,045	4/21/2015	MRAM with sidewall protection and method of fabrication
120	9,009,397	4/14/2015	STORAGE PROCESSOR MANAGING SOLID STATE DISK ARRAY
121	9,009,396	4/14/2015	PHYSICALLY ADDRESSED SOLID STATE DISK EMPLOYING FLASH AND MAGNETIC RANDOM ACCESS MEMORY (MRAM)
122	8,996,888	3/31/2015	Mobile device using secure spin torque transfer magnetic random access memory (SSTMRAM)
123	8,982,616	03-17-15	Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) with Perpendicular Laminated Free layer
124	8,981,506	3/17/2015	MAGNETIC RANDOM ACCESS MEMORY WITH SWITCHABLE SWITCHING ASSIST LAYER
125	8,980,649	3/17/2015	METHOD FOR MANUFACTURING NON-VOLATILE MAGNETIC MEMORY
126	8,975,089	3/10/2015	METHOD FOR FORMING MTJ MEMORY ELEMENT
127	8,975,088	3/10/2015	MRAM ETCHING PROCESSES
128	8,971,107	3/3/2015	EMULATION OF STATIC RANDOM ACCESS MEMORY (SPAM) BY MAGNETIC RANDOM ACCESS MEMORY (MRAM)
129	8,971,100	3/3/2015	INITIALIZATION METHOD OF A PERPENDICULAR MAGNETIC RANDOM ACCESS MEMORY (MRAM) DEVICE
130	8,966,164	2/24/2015	STORAGE PROCESSOR MANAGING NVME LOGICALLY ADDRESSED SOLID STATE DISK ARRAY
131	8,962,349	2/24/2015	METHOD OF MANUFACTURING MAGNETIC TUNNEL JUNCTION MEMORY ELEMENT
132	8,954,759	2/10/2015	SECURE SPIN TORQUE TRANSFER MAGNETIC RANDOM ACCESS MEMORY (STTMRAM)
133	8,954,658	2/10/2015	Method of LUN management in a sold state disk array
134	8,954,657	2/10/2015	STORAGE PROCESSOR MANAGING SOLID STATE DISK ARRAY
135	8,947,937	2/3/2015	HOST-MANAGED LOGICAL MASS STORAGE DEVICE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)

	Patent #	Date Issued	Title
136	8,947,922	2/3/2015	A METHOD AND APPARATUS FOR READING A MAGNETIC TUNNEL JUNCTION USING A SEQUENCE OF SHORT PULSES
137	8,947,919	2/3/2015	HIGH CAPACITY LOW COST MULTI-STACKED CROSS-LINE MAGNETIC MEMORY
138	8,942,032	1/27/2015	METHOD FOR MAGNETIC SCREENING OF ARRAYS OF MAGNETIC MEMORIES
139	8,935,599	1/13/2015	Method for reducing Effective Raw Bit Error Rate in Multi-Level Cell NAND Flash Memory
140	8,929,146	1/6/2015	CONTROLLER MANAGEMENT OF MEMORY ARRAY OF STORAGE DEVICE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)
141	8,917,546	12/23/2014	METHOD AND APPARATUS FOR INCREASING THE RELIABILITY OF AN ACCESS TRANSITOR COUPLED TO A MAGNETIC TUNNEL JUNCTION (MTJ)
142	8,917,543	12/23/2014	A MULTI-STATE SPIN-TORQUE TRANSFER MAGNETIC RANDOM ACCESS MEMORY
143	8,909,855	12/9/2014	Storage System Employing MRAM and Physically Addressed Solid State Disk
144	8,891,326	11/18/2014	METHOD OF SENSING DATA IN MAGNETIC RANDOM ACCESS MEMORY WITH OVERLAP OF HIGH AND LOW RESISTANCE DISTRIBUTIONS
145	8,891,292	11/18/2014	Magnetoressistive layer structure with voltage-inucted switching and lotic cell application
146	8,891,291	11/18/2014	MAGNETORESIST-IVE LOGIC CELL AND METHOD OF USE
147	8,890,108	11/18/2014	MEMORY DEVICE HAVING VERTICAL SELECTION TRANSISTORS WITH SHARED CHANNEL STRUCTURE AND METHOD FOR MAKING THE SAME
148	8,887,013	11/11/2014	MAPPING OF RANDOM DEFECTS IN A MEMORY DEVICE
149	8,885,395	11/11/2014	MAGNETORESIST-IVE LOGIC CELL AND METHOD OF USE
150	8,883,520	11/11/2014	Redeposition Control in MRAM Fabrication Process
151	8,879,309	11/4/2014	Method and Apparatus for Programming a Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) Array
152	8,878,156	11/4/2014	MEMORY DEVICE HAVING STITCHED ARRAYS OF 4 F2 MEMORY CELLS
153	8,861,260	10/14/2014	MULTI-PORT MAGNETIC RANDOM ACCESS MEMORY (MRAM)
154	8,860,158	10/14/2014	High speed SST-MRAM with orthogonal pinned layer
155	8,852,676	10/7/2014	MAGNETIC RANDOM ACCESS MEMORY (MRAM) WITH ENHANCED MAGNETIC STIFFNESS AND METHOD OF MAKING SAME
156	8,836,061	9/16/2014	Magnetic Tunnel Junction With Non-Metallic Layer Adjacent to Free Layer
157	8,836,000	9/16/2014	A BOTTOM-TYPE PERPENDICULAR MAGNETIC TUNNEL JUNCTION (pMTJ) ELEMENT WITH THERMALLY STABLE

	Patent #	Date Issued	Title
			AMORPHOUS BLOCKING LAYERS
158	8,830,737	9/9/2014	A METHOD AND APPARATUS FOR SENSING THE STATE OF A MAGNETIC TUNNEL JUNCTION (MTJ)
159	8,830,736	9/9/2014	INITIALIZATION METHOD OF A PERPENDICULAR MAGNETIC RANDOM ACCESS MEMORY (MRAM) DEVICE WITH A STABLE REFERENCE CELL
160	8,806,284	8/12/2014	Method for Bit-Error Rate Testing of Resistance-based RAM Cells Using a Reflected Signal
161	8,806,098	8/12/2014	MULTI ROOT SHARED PERIPHERAL COMPONENT INTERCONNECT EXPRESS (PCIE) END POINT
162	8,803,200	8/12/2014	ACCESS TRANSISTOR WITH A BURIED GATE
163	8,802,451	8/12/2014	METHOD FOR MANUFACTURING HIGH DENSITY NON-VOLATILE MAGNETIC MEMORY
164	8,796,795	8/5/2014	MRAM WITH SIDEWALL PROTECTION AND METHOD OF FABRICATION
165	8,792,269	7/29/2014	Fast Programming of Magnetic Random Access Memory (MRAM)
166	8,779,537	7/15/2014	SPIN TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY (STTMRAM) HAVING GRADED SYNTHETIC FREE LAYER
167	8,772,888	7/8/2014	MTJ MRAM WITH STUDPATTERNING
168	8,772,886	07/08/2014	SPIN TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY (STTMRAM) HAVING GRADED SYNTHETIC FREE LAYER
169	8,760,914	6/24/2014	Magnetic memory write circuitry
170	8,758,850	6/24/2014	SST-MRAM MTJ manufacturing method with in-situ annealing
171	8,755,221	6/17/2014	EMULATION OF STATIC RANDOM ACCESS MEMORY (SPAM) BY MAGNETIC RANDOM ACCESS MEMORY (MRAM)
172	8,751,905	6/10/2014	Memory with on-chip error correction
173	8,730,716	5/20/2014	EMBEDDED MAGNETIC RANDOM ACCESS MEMORY (MRAM)
174	8,724,413	5/13/2014	A HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY
175	8,724,392	5/13/2014	CONTROLLER MANAGEMENT OF MEMORY ARRAY OF STORAGE DEVICE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)
176	8,724,380	5/13/2014	METHOD FOR READING AND WRITING MULTI-LEVEL CELLS
177	8,724,379	5/13/2014	A MAGNETIC MEMORY WITH A DOMAIN WALL
178	8,724,378	5/13/2014	Shared Transistor in a Spin-Torque Transfer Magnetic Random Access Memory (STTMRAM) Cell
179	8,723,281	5/13/2014	ACCESS TRANSISTOR WITH A BURIED GATE
180	8,719,492	5/6/2014	NON-VOLATILE BLOCK STORAGE MODULE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)

	Patent #	Date Issued	Title
181	8,711,631	4/29/2014	MANAGEMENT OF MEMORY ARRAY WITH MAGNETIC RANDOM ACCESS MEMORY (MRAM)
182	8,711,613	4/29/2014	NON-VOLATILE FLASH-RAM MEMORY WITH MAGNETIC MEMORY
183	8,709,956	4/29/2014	MRAM with sidewall protection and method of fabrication
184	8,704,206	4/22/2014	MEMORY DEVICE INCLUDING TRANSISTOR ARRAY WITH SHARED PLATE CHANNEL AND METHOD FOR MAKING THE SAME
185	8,693,240	4/8/2014	A METHOD AND APPARATUS FOR READING A MAGNETIC TUNNEL JUNCTION USING A SEQUENCE OF SHORT PULSES
186	8,687,418	4/1/2014	Flash Memory With Nano-Pillar Charge Trap
187	8,677,097	3/18/2014	PERISTENT BLOCK STORAGE ATTACHED TO MEMORY BUS
188	8,670,276	3/11/2014	HOST-MANAGED LOGICAL MASS STORAGE DEVICE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)
189	8,670,264	3/11/2014	MULTI-PORT MAGNETIC RANDOM ACCESS MEMORY (MRAM)
190	8,656,255	2/18/2014	Method for reducing Effective Raw Bit Error Rate in Multi-Level Cell NAND Flash Memory
191	8,644,060	2/4/2014	METHOD OF SENSING DATA OF A MAGNETIC RANDOM ACCESS MEMORIES (MRAM)
192	8,634,234	1/21/2014	EMBEDDED MAGNETIC RANDOM ACCESS MEMORY (MRAM)
193	8,633,720	1/21/2014	Method and apparatus fo rmeasuring magnetic parameters of magnetic thin film structures
194	8,623,452	1/7/2014	MAGNETIC RANDOM ACCESS MEMORY (MRAM) WITH ENHANCED MAGNETIC STIFFNESS AND METHOD OF MAKING SAME
195	8,611,147	12/17/2013	A SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY (STTMRAM) USING A SYNTHETIC FREE LAYER
196	8,611,145	12/17/2013	Spin-Torque Transfer Magnetic Random Access Memory (STTMRAM) Device with Shared Transistor and Minimal Written Data Disturbance
197	8,598,576	12/3/2013	MAGNETIC RANDOM ACCESS MEMORY WITH FIELD COMPENSATING LAYER AND MULTI-LEVEL CELL
198	8,595,427	11/26/2013	NON-VOLATILE BLOCK STORAGE MODULE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)
199	8,593,862	11/26/2013	SPIN-TRANSFER TORQUE MAGNETIC RANDOM ACCESS MEMORY HAVING MAGNETIC TUNNEL JUNCTION WITH PERPENDICULAR MAGNETIC ANISOTROPY
200	8,575,584	11/5/2013	RESISTIVE MEMORY DEVICE HAVING VERTICAL TRANSISTORS AND METHOD FOR MAKING THE SAME
201	8,574,928	11/5/2013	MRAM Fabrication Method with Sidewall Cleaning
202	8,565,010	10/22/2013	MAGNETIC RANDOM ACCESS MEMORY WITH FIELD COMPENSATING LAYER AND MULTI-LEVEL CELL
203	8,559,215	10/15/2013	PERPENDICULAR MRAM DEVICE AND ITS INITIALIZATION

	Patent #	Date Issued	Title
			METHOD
204	8,553,452	10/8/2013	METHOD FOR MAGNETIC SCREENING OF ARRAYS OF MAGNETIC MEMORIES
205	8,547,745	10/1/2013	HOST-MANAGED LOGICAL MASS STORAGE DEVICE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)
206	8,547,734	10/1/2013	Method of reading logical mass storage device using magnetic random access memory (MRAM)
207	8,542,526	9/24/2013	Magnetic Random Access Memory (MRAM) Manufacturing Process for a Small Magnetic Tunnel Junction (MTJ) Design with a Low Programming Current Requirement
208	8,542,524	9/24/2013	Magnetic Random Access Memory (MRAM) Manufacturing Process for a Small Magnetic Tunnel Junction (MTJ) Design with a Low Programming Current Requirement
209	8,536,063	9/17/2013	MRAM ETCHING PROCESSES
210	8,535,952	9/17/2013	METHOD FOR MANUFACTURING NON-VOLATILE MAGNETIC MEMORY
211	8,526,234	9/3/2013	CONTROLLER MANAGEMENT OF MEMORY ARRAY OF STORAGE DEVICE USING MAGNETIC RANDOM ACCESS MEMORY (MRAM)
212	8,519,496	8/27/2013	Spin-transfer torque magnetic random access memory with multlayered storage layer
213	8,508,984	8/13/2013	Low resistance high-TMR magnetic tunnel junction and process for fabrication therof
214	8,498,150	7/30/2013	Non-Volatile Magnetic Memory Element with Graded Layer
215	8,498,149	7/30/2013	Non-Volatile Magnetic Memory Element with Graded Layer
216	8,498,148	7/30/2013	Non-Volatile Magnetic Memory Element with Graded Layer
217	8,493,780	7/23/2013	Non-Volatile Magnetic Memory Element with Graded Layer
218	8,493,779	7/23/2013	Non-Volatile Magnetic Memory Element with Graded Layer
219	8,493,778	7/23/2013	Non-Volatile Magnetic Memory Element with Graded Layer
220	8,493,777	7/23/2013	NON-VOLATILE MAGNETIC MEMORY WITH LOW SWITCHING CURRENT AND HIGH THERMAL STABILITY
221	8,492,860	7/23/2013	MAGNETIC LATCH MAGNETIC RANDOM ACCESS MEMORY (MRAM)
222	8,488,376	7/16/2013	Non-Volatile Magnetic Memory Element with Graded Layer
223	8,477,530	7/2/2013	Non-Uniform Switching Based Non-Volatile Magnetic Based Memory
224	8,477,529	7/2/2013	EMBEDDED MAGNETIC RANDOM ACCESS MEMORY (MRAM)
225	8,456,897	6/4/2013	LOW COST MULTI-STATE MAGNETIC MEMORY
226	8,440,471	5/14/2013	A LOW-COST NON-VOLATILE FLASHRAM MEMORY
227	8,427,863	4/23/2013	LOW CURRENT SWITCHING MAGNETIC TUNNEL JUNCTION DESIGN FOR MAGNETIC MEMORY USING DOMAIN WALL MOTION

	Patent #	Date Issued	Title
228	8,422,286	4/16/2013	Low-crystallization temperature MTJ for Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM)
229	8,405,174	3/26/2013	NON-VOLATILE MAGNETIC MEMORY WITH LOW SWITCHING CURRENT AND HIGH THERMAL STABILITY
230	8,399,943	3/19/2013	Non-Volatile Magnetic Memory Element with Graded Layer
231	8,399,942	3/19/2013	Non-Volatile Magnetic Memory Element with Graded Layer
232	8,391,058	3/5/2013	A LOW-COST NON-VOLATILE FLASHRAM MEMORY
233	8,391,054	3/5/2013	A HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC MEMORY
234	8,389,301	3/5/2013	Non-Uniform Switching Based Non-Volatile Magnetic Based Memory
235	8,385,108	2/26/2013	DIFFERENTIAL MAGNETIC RANDOM ACCESS MEMORY (MRAM)
236	8,374,025	2/12/2013	A Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM) With Laminated Free Layer
237	8,363,460	1/29/2013	METHOD AND APPARATUS FOR PROGRAMMING A MAGNETIC TUNNEL JUNCTION (MTJ)
238	8,363,457	1/29/2013	Memory Sensing Circuit
239	8,330,240	12/11/2012	LOW COST MULTI-STATE MAGNETIC MEMORY
240	8,313,960	11/20/2012	MAGNETIC TUNNEL JUNCTION (MTJ) FORMATION WITH TWO-STEP PROCESS
241	8,310,020	11/13/2012	NON-VOLATILE MAGNETIC MEMORY WITH LOW SWITCHING CURRENT AND HIGH THERMAL STABILITY
242	8,295,083	10/23/2012	METHOD AND APPARATUS FOR INCREASING THE RELIABILITY OF AN ACCESS TRANSITOR COUPLED TO A MAGNETIC TUNNEL JUNCTION (MTJ)
243	8,289,757	10/16/2012	EMBEDDED MAGNETIC RANDOM ACCESS MEMORY (MRAM)
244	8,238,145	8/7/2012	Shared Transistor in a Spin-Torque Transfer Magnetic Random Access Memory (STTMRAM) Cell
245	8,183,652	5/22/2012	NON-VOLATILE MAGNETIC MEMORY WITH LOW SWITCHING CURRENT AND HIGH THERMAL STABILITY
246	8,169,821	5/1/2012	Low-crystallization temperature MTJ for Spin-Transfer Torque Magnetic Random Access Memory (STTMRAM)
247	8,164,947	4/24/2012	LOW CURRENT SWITCHING MAGNETIC TUNNEL JUNCTION DESIGN FOR MAGNETIC MEMORY USING DOMAIN WALL MOTION
248	8,148,174	4/3/2012	MAGNETIC TUNNEL JUNCTION (MTJ) FORMATION WITH TWO-STEP PROCESS
249	8,120,949	2/21/2012	A LOW-COST NON-VOLATILE FLASHRAM MEMORY
250	8,084,835	12/27/2011	Non-Uniform Switching Based Non-Volatile Magnetic Based Memory
251	8,063,459	11/22/2011	Non-Volatile Magnetic Memory Element with Graded Layer
252	8,058,696	11/15/2011	A HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC

	Patent #	Date Issued	Title
			MEMORY
253	8,018,011	9/13/2011	LOW COST MULTI-STATE MAGNETIC MEMORY
254	7,981,697	7/19/2011	CURRENT-CONFINED EFFECT OF MAGNETIC NANO-CURRENT-CHANNEL (NCC) FOR MAGNETIC RANDOM ACCESS MEMORY (MRAM)
255	7,869,266	1/11/2011	LOW CURRENT SWITCHING MAGNETIC TUNNEL JUNCTION DESIGN FOR MAGNETIC MEMORY USING DOMAIN WALL MOTION
256	7,732,881	6/8/2010	CURRENT-CONFINED EFFECT OF MAGNETIC NANO-CURRENT-CHANNEL (NCC) FOR MAGNETIC RANDOM ACCESS MEMORY (MRAM)
257	10,217,934	2/26/2020	Method for manufacturing Magnetic Memory Cells
258	10,224,367	3/5/2019	Selector device Incorporating Conductive Cluster for Memory Application
259	10,268,393	3/17/2020	Magnetic random access memory with dynamic random access memory (DRAM)like interface
260	10,347,691	7/9/2019	Magnetic Memory Element with Multilayred seed structure
261	10,361,362	7/23/2019	MAGNETIC RANDOM ACCESS MEMORY WITH ULTRATHIN REFERENCE LAYER
262	10,395,710	8/27/2019	Magnetic Memory Emulting dynamic Random Access Memory (DRAM)
263	10,438,997	10/08/2019	Multilayered Seed for Magnetic Structure
264	10,490,737	11/26/2019	Magnetic Random Access Memory with Perpendicular Enhancement Layer
265	10,515,681	12/24/2019	Power-Efficient Programming of Magnetic Memory
266	10,522,590	12/31/2019	Magnetic Memory Incorporating Dual Selectors
267	10,559,624	2/11/2020	Selector Device Having Asymmetric Conductance for Memory Applications
268	10,593,727	3/17/2020	Magnetic Memory Cell Including Two-Terminal Selector Device
269	10,628,169	4/21/2020	Method of Implementing Magnetic Random Access Memory (MRAM) for Mobile System -on Chip Boot
270	RE47975	5/5/2020	Perpendicular Magnetic Tunnel Junction (pMTJ) with in-plane Magneto-Static Switching- Enhancing Layer
271	10,720,469	7/21/2020	Multilayered Seed for Magnetic Structure
272	10,727,400	7/28/2020	Magnetic Random Access Memory with Perpendicular Enhancement Layer
273	10/811,072	10/20/2020	Power-Efficient Programming of Magnetic Memory
274	10/818,330	10/27/2020	Fast Programming of Magnetic Random Access Memory (MRAM)
275	10/818,731	10/27/2020	Three- Dimensional Nonvolatile Memory
276	10/832,751	11/10/2020	Magnetic Memory and method for using the same
277	10/838,623	11/17/2020	MAGNETIC RANDOM ACCESS MEMORY WITH DYNAMIC RANDOM ACCESS MEMORY (DRAM)-LIKE INTERFACE

	Patent #	Date Issued	Title
278	10/910,555	2/2/2021	Magnetic Memory Element Incorporating Perpendicular Enhancement Layer
279	10/936,327	3/2/2021	Method of Implementing Magnetic Random Access Memory (MRAM) for Mobile System-on Chip Boot
280	10/950,659	3/16/2021	Multilayered Seed for Perpendicular Magnetic Structure

	Country	Patent Number	Date Issued	Title
1	China	CN101730913B	11/14/2012	Non-Volatile Magnetic Memory Element with Graded Layer
2	Korea	10-1497356	2/24/2015	Non-Volatile Magnetic Memory Element with Graded Layer
3	Germany	EP2118893	5/16/2012	Non-Volatile Magnetic Memory Element with Graded Layer
4	France	EP2118893	5/16/2012	Non-Volatile Magnetic Memory Element with Graded Layer
5	United Kingdom	EP2118893	5/16/2012	Non-Volatile Magnetic Memory Element with Graded Layer
6	Germany	EP2506264	4/16/2014	Non-Volatile Magnetic Memory Element with Graded Layer
7	France	EP2506264	4/16/2014	Non-Volatile Magnetic Memory Element with Graded Layer
8	United Kingdom	EP2506264	4/16/2014	Non-Volatile Magnetic Memory Element with Graded Layer
9	China	CN101711408B	4/10/2013	IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC
10	Korea	10-1414485	6/26/2014	IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC
11	Germany	EP2118894	6/6/2012	IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC
12	France	EP2118894	6/6/2012	IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC
13	United Kingdom	EP2118894	6/6/2012	IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC
14	China	CN103544982B	7/4/2017	IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC
15	Germany	EP2515306	6/2/2014	IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC
16	France	EP2515306	6/2/2014	IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC
17	United Kingdom	EP2515306	6/2/2014	IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC
18	China	CN103544983B	8/29/2017	IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC
19	Germany	EP2515307	7/16/2014	IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC
20	France	EP2515307	7/16/2014	IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC
21	United Kingdom	EP2515307	7/16/2014	IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC
22	China	CN103268774B	9/22/2017	IMPROVED HIGH CAPACITY LOW COST

	Country	Patent Number	Date Issued	Title
				MULTI-STATE MAGNETIC
23	Germany	EP2523193	7/16/2014	IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC
24	France	EP2523193	7/16/2014	IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC
25	United Kingdom	EP2523193	7/16/2014	IMPROVED HIGH CAPACITY LOW COST MULTI-STATE MAGNETIC

EXHIBIT C

Trademarks

Title or Mark	Country	Application	Filing Date	Trademark Number
AVALANCHE TECHNOLOGY	US	77/555,366	8/25/2008	4,198,751
AVALANCHE	US	77/664,140	2/5/2009	4,237,990
AVA	US	86/120,452	11/15/2013	4,946,647

Pending Trademarks

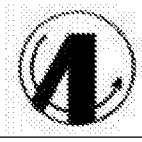
Title or Mark	Country	Application	Filing Date	Trademark Number
	US	88/196,128	11/15/2018	Pending

EXHIBIT D

Mask Works

Description	Registration/ Application Number	Registration/ Application Date
None.		