

REC

05-14-2002

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To the Commissioner, United States P

102089282

ached original documents or copy thereof.

1. Name of conveying party(ies)
Intrinsity, Inc.

2. Name and address of receiving party(ies)

Name: Adams Capital Management III, L.P.

Internal Address: _____

Street Address: 500 Blackburn Avenue

City: Sewickley State: PA ZIP: 15143

- Individual(s)
- General Partnership
- Corporation - State
- Other _____
- Association
- Limited Partnership

- Association
- Individual(s) citizenship _____
- Association
- General Partnership
- Limited Partnership
- Corporation-State
- Other _____

Additional name(s) of conveying party(ies) attached? Yes No

3. Nature of conveyance:

- Assignment
- Security Agreement
- Other _____
- Merger
- Change of Name

Execution Date: April 5, 2002

If assignee is not domiciled in the United States, a domestic representative designation is attached: Yes No
(Designations must be a separate document from assignment)
Additional name(s) & address(es) attached? Yes No

4. Application number(s) or registration number(s):

A. Trademark Application No.(s)

75/666,953

75/666,954

78/062,324

B. Trademark Registration No.(s)

Additional numbers attached? Yes No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: David J. Thibodeau, Jr.

Internal Address: _____

Hamilton, Brook, Smith & Reynolds, P.C.

Street Address: 530 Virginia Road

P.O. Box 9133

City: Concord State: MA ZIP: 01742-9133

6. Total number of applications and registrations involved: [11]

7. Total Fee (37 C.F.R. 3.41)..... \$ 290

- Enclosed
- Authorized to charge any deficiencies or credit any overpayment to deposit account
- Authorized to be charged to deposit account

8. Deposit account number:

08-0380

(Attach duplicate copy of this page if paying by deposit account)

DO NOT USE THIS SPACE

9. Statement and signature.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

David J. Thibodeau, Jr.

Name of Person Signing

[Signature]

Signature

4/30/02

Date

05/13/2002 00000179 75666953

01 FC:481
02 FC:482

Total number of pages including cover sheet, attachments, and document: [14]

40.00 DP
250.00 DP

OFFICE OF PUBLIC RECORDS
7 AM 7:45
TRADEMARK SECTION

Attachment A
RECORDATION FORM COVER SHEET
TRADEMARKS ONLY

4. A. Trademark Application Nos.

78/065,724

78/032,605

75/895,354

78/007,731

78/007,760

78/007,766

78/065,636

78/075,206

ADDENDUM TO THE INTELLECTUAL PROPERTY SECURITY AGREEMENT FOR
PATENTS AND TRADEMARKS

THIS ADDENDUM to the Intellectual Property Security Agreement for Patents and Trademarks ("Agreement") made and entered into on the 26th day of February, 2002, by and between Intrinsicity, Inc. ("Borrower") and Adams Capital Management, III, L.P. ("Lenders' Agent"), is made an entered into as of the 26th day of February, 2002.

WHEREAS, the Lenders' Agent has been granted certain liens and security interests in and to the intellectual property set forth in Schedule 1;

WHEREAS, the Lenders' Agent has requested to perfect the security interest by recording, in the Lenders' name, the intellectual property rights as set forth in Schedule 1 with the U.S. Patent and Trademark Office;

WHEREAS, the U.S. Patent and Trademark Office requires the application and registration numbers for patent applications and trademarks for recordal thereat;

NOW, THEREFORE, the Borrower and the Lenders' Agent covenant and agree to record notice of the Lenders' interest in the intellectual property set forth in Schedule 1 in the name of the Lenders' Agent.

IN WITNESS WHEREOF, and intending to be legally bound, the parties have executed and delivered this Agreement as of the day and year set forth above.

BORROWER:

INTRINSITY, INC.

By: 

Title: president & cco

Date: 4.5.02

LENDERS' AGENT:

ADAMS CAPITAL MANAGEMENT III,
L.P.

By: 

Title: General Partner

Date: 4/5/02

Exhibit A

Pending Patent Applications

Application Number	Filing Date
09/019,278	February 5, 1998
09/181,406	October 28, 1998
09/405,618	September 24, 1999
09/373,840	August 13, 1999
09/406,016	September 24, 1999
09/468,760	December 21, 1999
09/406,017	September 24, 1999
60/302,590	July 2, 2001
09/496,008	February 1, 2000
09/398,618	September 17, 1999
09/374,588	August 13, 1999
09/405,474	September 24, 1999
99951988.7	October 12, 1999
2000-578908	October 12, 1999
09/527,653	March 17, 2000
09/468,759	December 21, 1999
09/546,412	April 10, 2000
60/294,204	May 25, 2001
PCT/US/9929409	December 10, 1999
PCT/US/9930502	December 21, 1999
09/587,729	June 5, 2000

Application Number	Filing Date
60/302,587	July 2, 2001
09/844,686	April 27, 2001
09/901,411	July 9, 2001
60/296,410	June 6, 2001
60/293,869	May 25, 2001
60/302,599	July 2, 2001
60/302,593	July 2, 2001
09/966,049	September 28, 2001
09/965,945	September 28, 2001
60/302,400	July 2, 2001
09/206,905	December 7, 1998
09/373,516	August 12, 1999
09/123,742	July 28, 1998
09/195,758	November 18, 1998
09/210,410	December 11, 1998

Client-Matter/Subcase Case Type	Country Client	Patent Number Issue Date	Status Expiration Date	Attorney(s)
31876-0101/1 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for a N-Nary Logic Circuit Using Capacitance Isolation</i>	6,124,735 26-Sep-2000	Granted 10-Dec-2018	KSW MJB
31876-0102/1 ORD	United States of America Intrinsity, Inc. <i>Title: Operation-Independent Power Consumption</i>	6,107,835 22-Aug-2000	Granted 10-Dec-2018	MJB KSW
31876-0103/1 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for Routing 1 of N Signals</i>	6,202,194 13-Mar-2001	Granted 06-May-2018	MJB
31876-0104/1 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for Routing 1 of 4 Signals</i>	6,211,456 03-Apr-2001	Granted 06-May-2018	MJB
31876-0107/1 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for an N-Nary Logic Circuit Using 1 of N Signals</i>	6,069,497 30-May-2000	Granted 05-Feb-2018	MJB
31876-0108/3 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for Logic Synchronization</i>	6,118,304 12-Sep-2000	Granted 27-Oct-2018	MJB KSW
31876-0111/2 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for Transforming Pseudorandom Binary Patterns into Test Stimulus Patterns Appropriate for Circuits Having 1 of N encoded Inputs</i>	6,295,622 25-Sep-2001	Granted 07-Dec-2018	KSW MJB
31876-0112/1 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for Speed Detection Circuitry</i>	6,088,830 11-Jul-2000	Granted 28-Jul-2018	KSW MJB

Client-Matter/Subcase Case Type	Country Client	Patent Number Issue Date	Status Expiration Date	Attorney(s)
31876-0117/1 ORD	United States of America Intrinsity, Inc.	6,301,600 09-Oct-2001	Granted 18-Nov-2018	MJB
<i>Title: Method and Apparatus for a Dynamic Partitionable Saturating Adder/Subtractor</i>				
31876-0118/1 ORD	United States of America Intrinsity, Inc.	6,260,131 10-Jul-2001	Granted 18-Nov-2018	KSW MJB
<i>Title: Method and Apparatus for TLB Memory Ordering</i>				
31876-0120/1 ORD	United States of America Intrinsity, Inc.	6,334,183 25-Dec-2001	Granted 18-Nov-2018	MJB
<i>Title: Method and Apparatus for Partial Register Write Handling</i>				
31876-0121/1 ORD	United States of America Intrinsity, Inc.	6,209,076 27-Mar-2001	Granted 24-Jul-2018	MJB
<i>Title: Method and Apparatus for Two Stage Address Generation</i>				
31876-0123/1 ORD	United States of America Intrinsity, Inc.	6,272,653 07-Aug-2001	Granted 13-Nov-2018	KSW MJB
<i>Title: Method and Apparatus for Built-In Self-Test of Logic Circuitry</i>				
31876-0125/1 ORD	United States of America Intrinsity, Inc.	6,185,593 06-Feb-2001	Granted 22-Jul-2018	KSW MJB
<i>Title: Method and Apparatus for Parallel Normalization and Rounding Technique for Floating Point Arithmetic Operations</i>				
31876-0126/1 ORD	United States of America Intrinsity, Inc.	6,173,299 09-Jan-2001	Granted 22-Jul-2018	KSW MJB
<i>Title: A Method and Apparatus for Selecting an Intermediate Result for Parallel Normalization and Rounding Technique for Floating Point Arithmetic Operations</i>				
31876-0127/1 ORD	United States of America Intrinsity, Inc.	6,066,965 23-May-2000	Granted 05-Feb-2018	MJB
<i>Title: Method and Apparatus for an N-Nary Logic Circuit Using 1 of 4 Signals</i>				

Client-Matter/Subcase Case Type	Country Client	Patent Number Issue Date	Status Expiration Date	Attorney(s)
31876-0130/1 ORD	United States of America Intrinsity, Inc. <i>Title: Shifting for Parallel Normalization and Rounding Technique for Floating Point Arithmetic Operations</i>	6,175,847 16-Jan-2001	Granted 22-Jul-2018	KSW MJB
31876-0131/1 ORD	United States of America Intrinsity, Inc. <i>Title: Dynamic 3-Level Partial Result Merge Adder</i>	6,334,136 25-Dec-2001	Granted 11-Dec-2018	MJB
31876-0132/1 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for N-nary Incrementor</i>	6,347,327 12-Feb-2002	Granted 07-Dec-2018	KSW MJB
31876-0133/3 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for Generating Clock Signals</i>	6,288,589 11-Sep-2001	Granted 27-Oct-2018	MJB
31876-0134/2 ORD	United States of America Intrinsity, Inc. <i>Title: A Method and Apparatus for an Enhanced Floating Point Unit with Graphics and Integer Capabilities</i>	6,275,838 14-Aug-2001	Granted 28-Oct-2018	MJB
31876-0135/1 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for 1 of 4 Register File Design</i>	6,104,642 15-Aug-2000	Granted 09-Dec-2018	MJB
31876-0136/1 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for N-nary Hardware Description Language</i>	6,289,497 11-Sep-2001	Granted 11-Dec-2018	KSW MJB
31876-0137/1 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for an Address Triggered RAM Circuit</i>	6,118,716 12-Sep-2000	Granted 09-Sep-2018	MJB

Client-Matter/Subcase Case Type	Country Client	Patent Number Issue Date	Status Expiration Date	Attorney(s)
31876-0139/3 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus that Allows the Logic State of a Logic Gate to be Tested when Stopping or Starting the Logic Gate's clock</i>	6,233,707 15-May-2001	Granted 27-Oct-2018	MJB KSW
31876-0144/1 ORD	United States of America Intrinsity, Inc. <i>Title: A Method and Apparatus for Formatting an Intermediate Result for Parallel Normalization and Rounding Technique for Floating Point Arithmetic Operations</i>	6,151,615 21-Nov-2000	Granted 22-Jul-2018	KSW MJB
31876-0145/1 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for a 3-Stage 32-Bit Adder</i>	6,269,387 31-Jul-2001	Granted 07-Dec-2018	MJB
31876-0146/1 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for an N-Nary Sum/HPG Gate</i>	6,219,687 17-Apr-2001	Granted 10-Sep-2018	MJB
31876-0147/1 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for a 1 of 4 Shifter</i>	6,324,239 27-Nov-2001	Granted 07-Dec-2018	MJB
31876-0148/1 ORD	United States of America Intrinsity, Inc. <i>Title: 1 of 4 Multiplier</i>	6,275,841 14-Aug-2001	Granted 05-Nov-2018	KSW MJB
31876-0150/1 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for an N-nary Sum/HPG Adder/Subtractor Gate</i>	6,219,686 17-Apr-2001	Granted 10-Sep-2018	MJB
31876-0151/1 ORD	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for an N-Nary Adder Gate</i>	6,216,146 10-Apr-2001	Granted 10-Sep-2018	MJB

Client-Matter/Subcase Case Type	Country Client	Patent Number Issue Date	Status Expiration Date	Attorney(s)
31876-0152/1 ORD	United States of America Intrinsity, Inc.	6,223,199 24-Apr-2001	Granted 10-Sep-2018	MJB
<i>Title: Method and Apparatus for an N-nary HPG Gate</i>				
31876-0153/1 ORD	United States of America Intrinsity, Inc.	6,069,836 30-May-2000	Granted 09-Sep-2018	MJB
<i>Title: Method and Apparatus for a RAM Circuit having N-NARY Word Line Generation</i>				
31876-0154/1 ORD	United States of America Intrinsity, Inc.	6,046,931 04-Apr-2000	Granted 09-Sep-2018	MJB
<i>Title: Method and Apparatus for a RAM Circuit Having N-Nary Output Interface</i>				
31876-0156/1 ORD	United States of America Intrinsity, Inc.	6,216,147 10-Apr-2001	Granted 07-Dec-2018	MJB
<i>Title: Method and Apparatus for an N-Nary Magnitude Comparator</i>				
31876-0157/1 ORD	United States of America Intrinsity, Inc.	6,154,120 28-Nov-2000	Granted 07-Dec-2018	MJB
<i>Title: Method and Apparatus for an N-nary Equality Comparator</i>				
31876-0159/1 ORD	United States of America Intrinsity, Inc.	6,272,514 07-Aug-2001	Granted 18-Nov-2018	MJB
<i>Title: Method and Apparatus for Interruption of Carry Propagation on Partition Boundaries</i>				
31876-0160/1 ORD	United States of America Intrinsity, Inc.	6,301,597 09-Oct-2001	Granted 18-Nov-2018	KSW MJB
<i>Title: Method and Apparatus for Saturation in an N-nary Adder/Subtractor</i>				
31876-0163/1 ORD	United States of America Intrinsity, Inc.	6,345,381 05-Feb-2002	Granted 11-Dec-2018	KSW MJB
<i>Title: Method and Apparatus for a Logic Circuit Design Tool</i>				

Client-Matter/Subcase Case Type	Country Client	Patent Number Issue Date	Status Expiration Date	Attorney(s)
31876-0167/2 CON	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for Multi-bit Register Cell</i>	6,115,294 05-Sep-2000	Granted 11-Dec-2017	MJB
31876-0174/4 CIP	United States of America Intrinsity, Inc. <i>Title: Dynamic Logic Scan Gate Method and Apparatus</i>	6,271,683 07-Aug-2001	Granted 21-Dec-2019	KSW MJB
31876-0217/2 CON	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for an N-Nary Logic Circuit</i>	6,252,425 26-Jun-2001	Granted 05-Feb-2018	MJB
31876-0219/2 DIV	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for a RAM Circuit Having N-Nary Output Interface</i>	6,181,596 30-Jan-2001	Granted 11-Dec-2017	MJB
31876-0221/2 CON	United States of America Intrinsity, Inc. <i>Title: Dynamic Adjustment of the Clock Rate in Logic Circuits</i>	6,349,387 19-Feb-2002	Granted 28-Jul-2018	KSW MJB
31876-0224/4 CON	United States of America Intrinsity, Inc. <i>Title: Method and Apparatus for Logic Synchronization</i>	6,268,746 31-Jul-2001	Granted 27-Oct-2018	MJB

Trademark	Client-Matter/Subcase Country Name	Application Number/Date	Publication Number/Date	Registration Number/Date	Status Next Renewal
DIT	31876-0169/ United States of America <i>Class(es):</i> 42 <i>Client:</i> Intrinsity, Inc. <i>Agent Name:</i> <i>Owner Name:</i> Intrinsity, Inc. <i>Goods:</i> Engineering design services for semiconductor devices; licensing of intellectual property, namely semiconductor devices, cell libraries, and technology for semiconductor design and manufacturing qualification.	75/666,953 24-Mar-1999	17-Jul-2001 <i>Attorney(s):</i> MJB <i>Client Ref:</i> <i>Agent Ref:</i>		Allowed
DUAL-BIT	31876-0170/ United States of America <i>Class(es):</i> 42 <i>Client:</i> Intrinsity, Inc. <i>Agent Name:</i> <i>Owner Name:</i> Intrinsity, Inc. <i>Goods:</i> Engineering design services for semiconductor devices; licensing of intellectual property, namely semiconductor devices, cell libraries, and technology for semiconductor design and manufacturing qualification.	75/666,954 24-Mar-1999	17-Jul-2001 <i>Attorney(s):</i> MJB <i>Client Ref:</i> <i>Agent Ref:</i>		Allowed
F14	31876-0260/ United States of America <i>Class(es):</i> 009 <i>Client:</i> Intrinsity, Inc. <i>Agent Name:</i> <i>Owner Name:</i> Intrinsity, Inc. <i>Goods:</i> Semiconductor devices	78/062,324 07-May-2001	18-Sep-2001 <i>Attorney(s):</i> MJB <i>Client Ref:</i> <i>Agent Ref:</i>		Allowed
FAST14	31876-0261/ United States of America <i>Class(es):</i> 009 <i>Client:</i> Intrinsity, Inc. <i>Agent Name:</i> <i>Owner Name:</i> <i>Goods:</i> Semiconductor devices	78/065,724 25-May-2001	18-Dec-2001 <i>Attorney(s):</i> MJB <i>Client Ref:</i> <i>Agent Ref:</i>		Published

Trademark	Client-Matter/Subcase Country Name	Application Number/Date	Publication Number/Date	Registration Number/Date	Status Next Renewal
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IN dot logo (or badge logo) and design

31876-0228/
United States of America

Pending

Class(es): 009

Attorney(s): MJB

Client: Intrinsicity, Inc.

Client Ref:

Agent Name:

Agent Ref:

Owner Name: Intrinsicity, Inc.

Goods: Semiconductor devices

Remarks: This page was generated by the TARR system on 02/04/2002 12:19:04 ET

Current Status: Final review prior to publication has been completed, application will be published for opposition.

Date of Status: 2002-01-24

Filing Date: 2000-10-26

The Information will be/was published in the Official Gazette on 2002-03-05

INTRINSITY

31876-0220/
United States of America

Allowed

Class(es): 9

Attorney(s): MJB

Client: Intrinsicity, Inc.

Client Ref:

Agent Name:

Agent Ref:

Owner Name: Intrinsicity, Inc.

Goods: Semiconductor devices

Intrinsicity and Design

31876-0225/
United States of America

Allowed

Class(es): 009

Attorney(s): MJB

Client: Intrinsicity, Inc.

Client Ref:

Agent Name:

Agent Ref:

Owner Name: Intrinsicity, Inc.

Goods: Semiconductor Devices

Remarks: Published for Opposition 12/05/2000

Trademark	Client-Matter/Subcase Country Name	Application Number/Date	Publication Number/Date	Registration Number/Date	Status	Next Renewal
Intrinsity Inverted Logo	31876-0226/ United States of America <i>Class(es):</i> 009 <i>Client:</i> Intrinsity, Inc. <i>Agent Name:</i> <i>Owner Name:</i> Intrinsity, Inc. <i>Goods:</i> Semiconductor devices	78/007,760 11-May-2000	13-Mar-2001		Allowed	
Intrinsity Part Stamp Logo	31876-0227/ United States of America <i>Class(es):</i> 009 <i>Client:</i> Intrinsity, Inc. <i>Agent Name:</i> <i>Owner Name:</i> Intrinsity, Inc. <i>Goods:</i> Semiconductor devices	78/007,766 11-May-2000	27-Feb-2001		Allowed	
NDL	31876-0246/ United States of America <i>Class(es):</i> 009 <i>Client:</i> Intrinsity, Inc. <i>Agent Name:</i> <i>Owner Name:</i> Intrinsity, Inc. <i>Goods:</i> Semiconductor devices	78/065,636 24-May-2001			Pending	
TWIZZLING	31876-0266/ United States of America <i>Class(es):</i> 009 <i>Client:</i> Intrinsity, Inc. <i>Agent Name:</i> <i>Owner Name:</i> Intrinsity, Inc. <i>Goods:</i> semiconductor devices	78/075,206 23-Jul-2001	20-Nov-2001		Published	