04-27-2007

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Form PTO-1594
(Rev. 03/01)
OMB No. 0651-0027 (exp. 5/31/2002)
Tab settings ⇨ ⇨ ⇨

U.S. DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office

To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copy thereof.

424407

1. Name of conveying party(ies):

RAZA MICROELECTRONICS, INC.

☐ Individual(s) ☐ Association
☐ General Partnership ☐ Limited Partnership
☑ Corporation-State
☐ Other

Additional name(s) of conveying party(ies) attached? ☐ Yes ☑ No

2. Name and address of receiving party(ies)

Name: Venture Lending & Leasing IV, Inc.
Internal Address:
Street Address: 2010 North First Street
City: San Jose State: CA Zip: 95131

☐ Individual(s) citizenship
☐ Association
☐ General Partnership
☐ Limited Partnership
☒ Corporation-State Maryland
☐ Other

If assignee is not domiciled in the United States, a domestic representative designation is attached: ☐ Yes ☐ No
(Designations must be a separate document from assignment)
Additional name(s) & address(es) attached? ☐ Yes ☑ No

3. Nature of conveyance:

☐ Assignment ☐ Merger
☒ Security Agreement ☐ Change of Name
☐ Other

Execution Date: 12/26/06

4. Application number(s) or registration number(s):

A. Trademark Application No.(s) 78/592849; 78/592854; 78/614252; 78/626845; 78/626856; 78/626878; 78/756626

B. Trademark Registration No.(s) 2,986086; 3,024284; 2,984009; 3,048934; 2,865549; 2,936552; 2,897576; 2,936657; 2,935385;

Additional number(s) attached ☑ Yes ☐ No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Russell D. Pollock, Esq.
Internal Address:
Street Address: Greene Radovsky Maloney & Share LLP
Four Embarcadero Center, Suite 4000
City: San Francisco State: CA Zip: 94111

6. Total number of applications and registrations involved: 36

7. Total fee (37 CFR 3.41).....$ 915.00

☑ Enclosed
☐ Authorized to be charged to deposit account

8. Deposit account number:

OFFICE OF PUBLIC RECORDS
FINANCE SECTION
2007 APR 24 PM 2:47

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9. Signature.

Jeffrey T. Klugman — Name of Person Signing
Signature
4/20/07 — Date

Total number of pages including cover sheet, attachments, and document: 16

04/26/2007 DBYRNE 00000012 78592849
01 FC:8521 40.00 OP
02 FC:8522 875.00 OP

Mail documents to be recorded with required cover sheet information to:
Commissioner of Patent & Trademarks, Box Assignments
Washington, D.C. 20231

Attachment to Trademark Cover Sheet
Raza Microelectronics, Inc.

2,944421
3,038510
2,917937
76/657092
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45596/0847
4/19/07/MVR/323772.1

INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement (this "Agreement") is made as of December 26, 2006, by and between RAZA MICROELECTRONICS, INC., a Delaware corporation ("Grantor"), and VENTURE LENDING & LEASING IV, INC., in its capacity as agent for itself and Silicon Valley Bank under the Loan Agreement (hereinafter defined) ("Secured Party").

RECITALS

A. Pursuant to a Loan and Security Agreement of even date herewith (the "Loan Agreement") between Grantor, as borrower, and Secured Party, as agent for itself and the other lenders party thereto ("Lenders"), Lenders have agreed to make certain advances of money and to extend certain financial accommodations to Grantor (the "Loans") in the amounts and manner set forth in the Loan Agreement. All capitalized terms used herein without definition shall have the meanings ascribed to them in the Loan Agreement.

B. Lenders are willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Secured Party, for the benefit of Lenders, a security interest in substantially all of Grantor's personal property whether presently existing or hereafter acquired. To that end, Grantor has executed in favor of Secured Party the Loan Agreement granting a security interest in all Collateral, and is executing this Agreement with respect to certain items of Intellectual Property, in particular.

NOW, THEREFORE, THE PARTIES HERETO AGREE AS FOLLOWS:

1. Grant of Security Interest. As collateral security for the prompt and complete payment and performance of all of Grantor's present or future Obligations, Grantor hereby grants a security interest and mortgage to Secured Party, as security, in and to Grantor's entire right, title and interest in, to and under the following Intellectual Property, now owned or hereafter acquired by Grantor or in which Grantor now holds or hereafter acquires any interest (all of which shall collectively be called the "Collateral" for purposes of this Agreement):

(a) Any and all copyrights, whether registered or unregistered, held pursuant to the laws of the United States, any State thereof or of any other country; all registrations, applications and recordings in the United States Copyright Office or in any similar office or agency of the United States, any State thereof or any other country; all continuations, renewals, or extensions thereof; and any registrations to be issued under any pending applications, including without limitation those set forth on Exhibit A attached hereto (collectively, the "Copyrights");

(b) All letters patent of, or rights corresponding thereto in, the United States or any other country, all registrations and recordings thereof, and all applications for letters patent of, or rights corresponding thereto in, the United States or any other country, including, without limitation, registrations, recordings and applications in the United States Patent and Trademark Office or in any similar office or agency of the United States, any State thereof or any other country; all reissues, continuations, continuations-in-part or extensions thereof; all petty patents, divisionals, and patents of addition; and all patents to be issued under any such applications, including without limitation the patents and patent applications set forth on Exhibit B attached hereto (collectively, the "Patents");

(c) All trademarks, trade names, corporate names, business names, trade styles, service marks, logos, other source or business identifiers, prints and labels on which any of the foregoing have appeared or appear, designs and general intangibles of like nature, now existing or hereafter adopted or acquired, all registrations and recordings thereof, and any applications in connection therewith, including, without limitation, registrations, recordings and applications in the United States Patent and Trademark Office or in any similar office or agency of the United States, any State thereof or any other country or any political subdivision thereof, and reissues, extensions or renewals thereof, and the entire goodwill of the business of Grantor connected with and symbolized by such trademarks, including without limitation those set forth on Exhibit C attached hereto (collectively, the "Trademarks");

(d) Any and all claims for damages by way of past, present and future infringement of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above;

(e) All licenses or other rights to use any of the Copyrights, Patents or Trademarks, and all license fees and royalties arising from such use to the extent permitted by such license or rights;

(f) All amendments, renewals and extensions of any of the Copyrights, Trademarks or Patents; and

(g) All proceeds and products of the foregoing, including without limitation all payments under insurance or any indemnity or warranty payable in respect of any of the foregoing.

2. Covenants. Grantor covenants and agrees as follows:

(a) During the term of this Agreement, Grantor will not transfer or otherwise encumber any interest in the Collateral, except for non-exclusive licenses granted by Grantor in the ordinary course of business or as set forth in this Agreement;

(b) Grantor shall deliver to Secured Party within thirty (30) days of the last day of each fiscal year in which there is a change or update to the reported contents from the previous fiscal year, a report signed by Grantor, in form reasonably acceptable to Secured Party, listing any applications or registrations that Grantor has made or filed in respect of any patents, copyrights or trademarks and the status of any outstanding applications or registrations.

(c) Grantor shall use reasonable commercial efforts to (i) protect, defend and maintain the validity and enforceability of the Trademarks, Patents and Copyrights (ii) detect infringements of the Trademarks, Patents and Copyrights and promptly advise Secured Party in writing of material infringements detected and (iii) not allow any material Trademarks, Patents or Copyrights to be abandoned, forfeited or dedicated to the public without the written consent of Secured Party, which consent shall not be unreasonably withheld;

(d) Grantor shall apply for registration (to the extent not already registered) with the United States Patent and Trademark Office or the United States Copyright Office, as applicable, of: (i) those intellectual property rights listed on Exhibits B and C hereto within thirty (30) days of the date of this Agreement; and (ii) those additional intellectual property rights developed or acquired by Grantor from time to time in connection with any product or service, prior to the sale or licensing of such product or the rendering of such service to any third party (including without limitation revisions or additions to the intellectual property rights listed on such Exhibits A, B and C), in each case except with respect to such rights that Grantor determines in its sole commercial judgment need not or should not be registered or maintained to protect its own business interests. Grantor shall, from time to time, execute and file such other instruments, and take such further actions (not inconsistent with Grantor's determinations referenced in the immediately preceding sentence) as Secured Party may reasonably request from time to time to perfect or continue the perfection of Secured Party's interest in the Collateral. Grantor shall give Secured Party notice of all such applications or registrations in accordance with clause (d) above; and

(e) Grantor shall not enter into any agreement that would materially impair or conflict with Grantor's obligations hereunder without Secured Party's prior written consent, which consent shall not be unreasonably withheld. Grantor shall not permit the inclusion in any material contract to which it becomes a party of any provisions that could or might in any way prevent the creation of a security interest in Grantor's rights and interests in any property included within the definition of the Collateral acquired under such contracts.

3. Further Assurances. On a continuing basis, Grantor will make, execute, acknowledge and deliver, and file and record in the proper filing and recording places in the United States, all such instruments, including appropriate financing and continuation statements and collateral agreements and filings with the United States Patent and Trademark Office and the Register of Copyrights, and take all such action as may reasonably be deemed necessary or advisable, or as reasonably requested by Secured Party, to perfect Secured Party's security interest in all

Copyrights, Patents and Trademarks and otherwise to carry out the intent and purposes of this Agreement, or for assuring and confirming to Secured Party the grant or perfection of a security interest in all Collateral.

4. Amendments. This Agreement may be amended only by a written instrument signed by both parties hereto.

5. Counterparts. This Agreement may be executed in two or more counterparts, each of which shall be deemed an original but all of which together shall constitute the same instrument.

Remainder of this page intentionally left blank; signature page follows

IN WITNESS WHEREOF, the parties hereto have executed this Agreement on the day and year first above written.

GRANTOR:

Address of Grantor:

RAZA MICROELECTRONICS, INC.

By: Steven Geiser

18920 Forge Drive
Cupertino, CA 95014
Attn: Chief Financial Officer

Name: Steven Geiser

Its: CFO

SECURED PARTY:

Address of Secured Party:

VENTURE LENDING & LEASING IV, INC., as Agent

2010 North First Street, Suite 310
San Jose, CA 95131
Attn: Chief Financial Officer

By: _____

Name: _____

Its: _____

IN WITNESS WHEREOF, the parties hereto have executed this Agreement on the day and year first above written.

GRANTOR:

Address of Grantor:

RAZA MICROELECTRONICS, INC.

By: _____

18920 Forge Drive
Cupertino, CA 95014
Attn: Chief Financial Officer

Name: _____

Its: _____

SECURED PARTY:

Address of Secured Party:

VENTURE LENDING & LEASING IV, INC., as Agent

2010 North First Street, Suite 310
San Jose, CA 95131
Attn: Chief Financial Officer

By: _____

Name: Brian R. Best

Its: Vice President

EXHIBIT A

Copyrights

As of the date hereof, the Company has common law Copyrights, but no federally-registered Copyrights.

EXHIBIT B

PATENTS

REGISTRATION NUMBER/DESCRIPTION	ISSUE DATE
US Pat. No. 6,035,388 for "Method And Apparatus For Dual Issue Of Program Instructions To Symmetric Multifunctional Execution Units"	March 7, 2000
US Pat. No. 6,055,606 for "Writeback Cache Cell With A Dual Ported Dirty Bit Cell And Method For Operating Such A Cache Cell"	April 25, 2000
US Pat. No. 6,070,229 for "Cache Memory Cell With A Pre-Programmed State"	May 30, 2000
US Pat. No. 6,069,893 for "Asynchronous Transfer Mode Switching Architectures Having Connection Buffers"	May 30, 2000
US Pat. No. 6,085,271 for "System Bus Arbitrator For Facilitating Multiple Transactions In A Computer System"	July 4, 2000
US Pat. No. 6,088,784 for "Processor With Multiple Execution Units And Local And Global Register Bypasses"	July 11, 2000
US Pat. No. 6,092,129 for "Method And Apparatus For Communicating Signals Between Circuits Operating At Different Frequencies"	July 18, 2000
US Pat. No. 6,198,723 for "Asynchronous Transfer Mode Traffic Shapers"	March 6, 2001
US Pat. No. 6,229,812 for "Scheduling Techniques For Data Cells In A Data Switch"	May 8, 2001
US Pat. No. 6,252,818 for "Apparatus And Method For Operating A Dual Port Memory Cell"	June 26, 2001
US Pat. No. 6,252,819 for "Reduced Line Select Decoder For A Memory Array"	June 26, 2001
US Pat. No. 6,255,879 for "Digital Programmable Delay Element"	July 3, 2001
US Pat. No. 6,292,061 for "Low-Voltage CMOS Phase-Locked Loop (PLL) For High-Performance Microprocessor Clock Generation"	September 18, 2001
US Pat. No. 6,311,292 for "Circuit, Architecture And Method For Analyzing The Operation Of A Digital Processing System"	October 30, 2001
US Pat. No. 6,349,098 for "Method and Apparatus for Forming a Virtual Circuit"	February 19, 2002
US Pat. No. 6,388,471 for "Single Phase Edge Trigger Register"	May 14, 2002
US Pat. No. 6,400,599 for "Cache Memory Cell With A Pre-Programmed State"	June 4, 2002
US Pat. No. 6,480,872 for "Floating-Point And Integer Multiply-Add And Multiply-Accumulate"	November 12, 2002
US Pat. No. 6,530,011 for "Method And Apparatus For Vector Register With Scalar Values"	March 4, 2003
US Pat. No. 6,594,753 for "Method And Apparatus For Dual Issue Of Program Instructions To Symmetric Multifunctional Execution Units"	July 15, 2003
US Pat. No. 6,686,774 for "System and Method for a High Speed Bi-Directional, Zero Turnaround	February 3, 2004

Time, Pseudo Differential Bus Capable of Supporting Arbitrary Number of Drivers"	
U.S. Pat. No. 6,694,408 for "Scalable Replacement Method and System in a Cache Memory"	February 17, 2004
U.S. Pat. No. 6,708,282 for "Method for Initiating Computation Upon Unordered Receipt of Data"	March 16, 2004
U.S. Pat. No. 6,735,689 for "Method for Reducing Taken Branch Penalty"	May 11, 2004
U.S. Pat. No. 6,775,788 for "High Performance Method and System for Processing Information on an Integrated Circuit"	August 10, 2004
US Pat. No. 6,963,895 for "Floating Point Pipeline Method and Circuit for Fast Inverse Square Root Calculations"	November 8, 2005
U.S. Pat. No. 7,002,916 for "Asynchronous Transfer Mode Traffic Shapers"	February 21, 2006
U.S. Pat. No. 7,002,978 for "Scheduling Techniques for data cells in a data switch"	February 21, 2006
US Pat. No. 7,028,069 B1 for "Dynamic Circuit Using Exclusive States"	April 26, 2006
US Pat. No. 7,046,681 B2 for "Network Switch for Routing Network Traffic"	May 16, 2006
US Pat. No. 7,062,767 B1 for "Method for Coordination of Information Flow Between Components"	June 13, 2006
US Pat. No. 7,072,345 B2 for "Programmable Integrated Circuit For Use In A Network Switch"	July 4, 2006
U.S. Pat. No. 7,099,584 for "Advanced Error Correcting Optical Transport Network"	August 29, 2006
US Pat. No. 7,164,860 for "Advanced Multi-Protocol Optical Transport Network"	January 16, 2007
U.S. Pat. No. 7,165,102 for "Adaptive Link Quality Management For Wireless Medium"	January 16, 2007
U.S. Pat. No. 7,174,441 B2 for "Method and Apparatus For Providing Internal Table Extensibility Based On Product Configuration"	February 6, 2007
U.S. Pat. No. 7,173,927 for "Hybrid Network To Carry Synchronous And Asynchronous Traffic Over Symmetric and Asymmetric Links"	February 6, 2007

PATENT APPLICATION NUMBER AND DESCRIPTION	**DATE FILED**
Utility Patent Application entitled "Low Power Cache System and Method" bearing Ser. No. 09/562,071	May 1, 2000
Utility Patent Application entitled "Method and Apparatus for Load/Store Exception Processing" bearing Ser. No. 09/564,715	May 3, 2000
Utility Patent Application entitled "Network Switch With A Parallel Shared Memory" bearing Ser. No. 09/939,454	August 24, 2001
Patent Cooperation Treaty Patent Application entitled "Network Switch With A Parallel Shared Memory" bearing Ser. No. PCT/US01/44499	November 28, 2001
Utility Patent Application entitled "Integration Of Network, Data, Link And Physical Layer To Adapt Network Traffic" Ser. No. 10/023,972	December 17, 2001
Utility Patent Application entitled "Network Mode With Multi-Medium Interfaces" Ser. No.	December 17, 2001

10/023,633	
Utility Patent Application entitled "Dynamic Mixing TDM Data with Data Packets" Ser. No. 10/023,974	December 17, 2001
Utility Patent Application entitled "Interfacing a 622.08 MHz LVDS Line Interface to a 77.76 MHz SONET Framer" bearing Ser. No. 10/093,324	March 6, 2002
Taiwan Patent Application entitled "Advanced Telecommunications Router And Crossbar Switch Controller"	November 20, 2002
Utility Patent Application entitled "Advanced Telecommunications Router And Crossbar Switch Controller" bearing Ser. No. 10/302,015	November 21, 2002
Utility Patent Application entitled "Multi-Protocol Serializer-Deserializer" bearing Ser. No. 10/452,563	May 30, 2003
Utility Patent Application entitled "Advanced Communication Apparatus and Method for Verified Communication" Ser. No. 10/452,229	June 3, 2003
Utility Patent Application entitled "Advanced Telecommunications Processor" bearing Ser. No. 10/682,579	October 8, 2003
Utility Patent Application entitled "Method and Apparatus For Providing Internal Table Extensibility Based On Product Configuration" Ser. No. 10/687,789	October 17, 2003.
Utility Patent Application entitled "Encoding-Based Multicast Packet Duplication Control Suitable For VLAN Systems" Ser. No. 10/687,784	October 17, 2003
Utility Patent Application entitled "Method and Apparatus For Packet Transmit Queue Control" Ser. No. 10/687,786	October 17, 2003
Utility Patent Application planned for invention entitled "Advanced Hashing Table" Ser. No. 10/703,842	November 7, 2003
Utility Patent Application in Progress for invention entitled "SRAM-Based Exact Match Search And Dynamic Hash Address Generation" Ser. No. 10/735,107	December 12, 2003
Utility Patent Application entitled "Technique for Deallocation of Memory in a Multicasting Environment" bearing Ser. No. 10/739,874	December 17, 2003
Utility Patent Application entitled "Extended Reach Media Access" bearing Ser. No. 10/740,910	December 19, 2003
PCT Application for "Classification of Packets in a Heterogeneous Data Redirection Device" bearing Ser. No. PCT/US04/02399	January 27, 2004
Utility Patent Application in Progress for invention entitled "Classification Key Construction: Mixture Of Ipv6 Address, User Programmable Offset And Meaningful Fields As Search Key" bearing Ser. No. 10/789,668	February 27, 2004
Utility Patent Application in Progress for invention entitled "Scheme Of Generating And Arbitrating Between Multiple Actions Using Action Group In Classifier" bearing Ser. No. 10/789,791	February 27, 2004
Utility Patent Application entitled "Stacked Network Switch Using Resilient Packet Ring Communication Protocol" bearing Ser. No. 10/826,215	April 16, 2004

Patent Cooperation Treaty Application entitled, "Advanced Processor" bearing Appl. No. PCT/US2004/023871	July 23, 2004
Utility Patent Application entitled "Advanced Processor With System On A Chip Interconnect Technology" bearing Ser. No. 10/898,008	July 23, 2004
Utility Patent Application entitled "Advanced Processor With Cache Coherency" bearing Ser. No. 10/897,577 filed (priority claim to Ser. No. 10/682,579	July 23, 2004
Utility Patent Application entitled "Advanced Processor With Novel Level 2 Cache Design" bearing Ser. No. 10/897,576 filed (priority claim to Ser. No. 10/682,579	July 23, 2004
Taiwan Patent Application entitled "Advanced Processor" bearing Ser. No. 93122312	July 26, 2004
Utility Patent Application entitled "Advanced Processor With Out of Order Load Store Scheduling in an In Order Pipeline" bearing Ser. No. 10/930,938	August 31, 2004
Utility Patent Application entitled "Advanced Processor With Mechanism For Maximizing Resource Usage In An In-Order Pipeline With Multiple Threads" bearing Ser. No. 10/930,939	August 31, 2004
Utility Patent Application entitled "Advanced Processor With Scheme For Optimal Packet Flow In A Multi-Processor System On A Chip" bearing Ser. No. 10/930,186	August 31, 2004
Utility Patent Application entitled "Advanced Processor With Interfacing Messaging Network To A CPU" bearing Ser. No. 10/930,937	August 31, 2004
Utility Patent Application entitled "Advanced Processor With Mechanism for Packet Distribution at High Line Rate" bearing Ser. No. 10/931,014	August 31, 2004
Utility Patent Application entitled "Advanced Processor With Use Of Bridges On A Data Movement Ring For Optimal Redirection Of Memory And I/O traffic" bearing Ser. No. 10/930,179	August 31, 2004
Utility Patent Application entitled "Advanced Processor With Implementation Of Memory Ordering On A Ring Based Data Movement Network" bearing Ser. No. 10/930,187	August 31, 2004
Utility Patent Application entitled "Advanced Processor With Mechanism For Enforcing Ordering Between Information Sent On Two Independent Networks" bearing Ser. No. 10/930,456	August 31, 2004
Utility Patent Application entitled "Advanced Processor With A Thread Aware Return Address Stack Optimally Used Across Active Threads" bearing Ser. No. 10/930,175	August 31, 2004
Utility Patent Application entitled "Prefix Matching Structure and Method For Fast Packet Switching" bearing Ser. No. 10/968,460	October 18, 2004
Utility Patent Application entitled "Mechanism for Managing Access to Resources in a Heterogeneous Data Redirection Device" bearing US Ser. No. 11/093,184	March 28, 2005
PCT Patent Application SN WO 2006/104804 A2, entitled "Mechanism for Managing Access to Resources in a Heterogeneous Data Redirection Device" bearing US Ser. No. 11/093,184	March 28, 2005
Utility Patent Application for "Scaleable Channel Scheduler System and Method" bearing Ser. No. 11/236,324	September 26, 2005
PCT Patent Application SN PCT 2006, 9/26/2006, for "Scaleable Channel Scheduler System and Method" bearing Ser. No. 11/236,324	September 26, 2005
US Utility Patent Application for "High Performance Integrated Circuit With Low Skew Clocking	November 18, 2005

Network" bearing Ser. No. 11/283,154	
India Patent Application entitled, "Advanced Processor" bearing Appl. No. 431/PT/US/06	January 24, 2006
Japan Patent Application entitled, "Advanced Processor" bearing Appl. No. 2006-521286	January 24, 2006
China Patent Application entitled, "Advanced Processor" bearing Appl. No 200480024380.7	February 24, 2006
Utility Patent Application entitled "Method and Apparatus For Providing Internal Table Extensibility With External Interface" bearing Ser. No. PCT/US2006/010401	March 21, 2006
Utility Patent Application entitled "Systems And Methods For Utilizing An Extended Translation Look-Aside Buffer Having A Hybrid Memory Structure" bearing Ser. No. 11/652,827	January 11, 2007
Utility Patent Application entitled "Automated Clock Grid Synthesis" bearing Ser. No. [TBA]	February 23, 2007

EXHIBIT C

TRADEMARKS

COUNTRY	REGISTERED MARK	CLASS
US	RAZA MICROELECTRONICS, Reg. No. 2986086	009, electronics
IN	RAZA MICROELECTRONICS, Ser. No. 1208074	009, electronics
US	RAZA MICROELECTRONICS, Reg. No. 3024284	042, engineering services
US	RMI, Reg. No. 2984009	009, electronics
CTM	RMI, Ser. No. 004137171	009, electronics
US	RMI and Design, Reg. No. 3048934	009, electronics
IN	RMI, Ser. No. 1237584	042, engineering services
KO	Alchemy, Reg. No. Kor223523	009, electronics
EP	ALCHEMY SEMICONDUCTOR and Design, Reg. No. 002079440	009, 016, 042
TW	ALCHEMY SEMICONDUCTOR and Design, Reg. No.1012833	009, electronics
US	AU 1100, Reg. No. 2865549	009, electronics
EP	AU 1100, Reg. No. 003101888	009, electronics
KR	AU 1100, Reg. No. 585369	009, electronics
TW	AU 1100, Reg. No. 1104036	009, electronics
US	AU 1000, Reg. No. 2936552	009, electronics
US	AU1500, Reg. No. 2897576	009, electronics
US	PB1000, Reg. No. 2936657	009, electronics
US	PB1100, Reg. No. 2935358	009, electronics
US	PB1500, Reg. No. 2944421	009, electronics
US	INTELLIGENT TRANSPORT, Reg. No. 3038510	009, electronics

COUNTRY	REGISTERED MARK- EXCLUSIVE LICENSE	CLASS
US	AMD ALCHEMY, Reg. No. 2917937	009, electronics
CA	AMD ALCHEMY, Reg. No. TMA661656	009, electronics
CN	AMD ALCHEMY, Reg. No. 3416458	009, electronics
BR	AMD ALCHEMY, Ser. No. 825179866	009, electronics
EP	AMD ALCHEMY, Reg. No. 002983112	009, electronics
HK	AMD ALCHEMY, Reg. No. 11655/2003	009, electronics
JP	AMD ALCHEMY, Reg. No. 4657832	009, electronics
KR	AMD ALCHEMY, Reg. No. 578350	009, electronics
MY	AMD ALCHEMY, Reg. No. 2002-15905	009, electronics

MX	AMD ALCHEMY, Reg. No. 786638	009, electronics
RU	AMD ALCHEMY, Reg. No. 275173	009, electronics
SG	AMD ALCHEMY, Reg. No. T02/195841	009, electronics
TW	AMD ALCHEMY, Reg. No. 1066030	009, electronics

COUNTRY	TRADEMARK APPLICATION	CLASS
IN	RAZA MICROELECTRONICS, Ser. No. 1237583	042, engineering services
CN	RMI, Ser. No. 3946972	009, electronics
IN	RMI, Ser. No. 1237580	009, electronics
IN	RMI TECHNOLOGIES, Ser. No. 1237581, 1237582	009, 042
CN	RMI and Design, Ser. No. 4375130	009, electronics
CTM	RMI and Design, Ser. No. 004137171	009, electronics
CTM	XLR, Ser. No. 004567459	009, electronics
CN	XLR, Ser. No. 4813145	009, electronics
TW	XLR, Ser. No. None.	009, electronics
US	ORION, Ser. No. 78592849 (unrecorded transfer to RMI 2006)	009, electronics
CN	ORION, Ser. No. None.	009, electronics
CTM	ORION, Ser. No. 004640728	009, electronics
IN	ORION, Ser. No. None.	009, electronics
US	PEGASUS, Ser. No. 78592854 (unrecorded transfer to RMI 2006)	009, electronics
CN	PEGASUS, Ser. No. None.	009, electronics
CTM	PEGASUS, Ser. No. 004640694	009, electronics
IN	PEGASUS, Ser. No. None.	009, electronics
CTM	INTELLIGENT ACCESS, Ser. No. None	009, electronics
CN	INTELLIGENT ACCESS, Ser. No. None.	009, electronics
CTM	THREAD PROCESSOR, Ser. No. None.	009, electronics
CN	THREAD PROCESSOR, Ser. No. None.	009, electronics
US	MICROMSAP, Ser. No. 78614252	009, electronics
US	RMI, Ser. No. 78626845	042, engineering services
US	XL, Ser. No. 78626856	009, electronics
US	I/O DISTRIBUTED INTERCONNECT, Ser. No. 78626878	009, electronics
US	PDH ACCESS PROCESSOR, Ser. No. 78642686	009, electronics
US	AUTONOMOUS SECURITY ACCELERATOR, Ser. No. 78756626	009, electronics
US	XLT, Ser. No. 76657092	009, electronics
CH	XLT, Ser. No. None.	009, electronics
EP	XLT, Ser. No. None.	009, electronics
TW	XLT, Ser. No. None.	009, electronics

US	XLT PROCESSOR, Ser. No. 76657096	009, electronics
US	XLS, Ser. No. 76657095	009, electronics
US	XLS PROCESSOR, Ser. No. 76657094	009, electronics
CH	XLS, Ser. No. None.	009, electronics
EP	XLS, Ser. No. None.	009, electronics
TW	XLS, Ser. No. None.	009, electronics
US	AUTONOMOUS ACCELERATION ENGINE, Ser. No. 76657097	009, electronics
US	AUTONOMOUS SECURITY ACCELERATION ENGINE, Ser. No. 76657098	009, electronics
US	AUTONOMOUS NETWORK ACCELERATION ENGINE, Ser. No. 76657099	009, electronics
US	DEDICATEDPLUS CACHE, Ser. No. 76657093	009, electronics
US	ALCHEMY INTERNET EDGE PROCESSOR, Ser. No. 76108104	009, electronics
US	ALCHEMY SEMICONDUCTOR and Design, Ser. No. 76108109	009, electronics
CN	AU 1100, Ser. No. 3493422	009, electronics
US	RMI ALCHEMY, Ser. No. 76669040	009, 042
CH	RMI ALCHEMY, Ser. No. None.	009, 042
EP	RMI ALCHEMY, Ser. No. None.	009, 042
TW	RMI ALCHEMY, Ser. No. None.	009, 042
US	AU1200, Ser. No. 76669446	009, 042
CH	AU1200, Ser. No. None.	009, 042
EP	AU1200, Ser. No. None.	009, 042
TW	AU1200, Ser. No. None.	009, 042
US	AU1550, Ser. No. 76669448	009, 042
CH	AU1550, Ser. No. None.	009, 042
EP	AU1550, Ser. No. None.	009, 042
TW	AU1550, Ser. No. None.	009, 042
US	ADVANCED PROCESSOR SOLUTIONS, Ser. No. 78422606	009, electronics
US	MSAP, Ser. No. 78642675	009, electronics
US	XLR PROCESSOR, Ser. No. 78472856 (Petition to revive Granted-Extension Request filed)	009, electronics
US	XLR, Ser. No. 78561058 (Petition to revive granted –Extension Request filed)	009, electronics

Attachment to Trademark Cover Sheet
Raza Microelectronics, Inc.

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