TRADEMARK ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE BY SECURED PARTY

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
VENTURE LENDING & LEASING IV, INC.		12/17/2007	CORPORATION: MARYLAND

RECEIVING PARTY DATA

Name:	COWARE, INC.
Street Address:	1732 N. FIRST STREET
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95112
Entity Type:	CORPORATION: DELAWARE

PROPERTY NUMBERS Total: 5

Property Type	Number	Word Mark
Registration Number:	2938869	CONVERGENSC
Registration Number:	2938868	DIFFERENTIATE BY DESIGN
Registration Number:	2780613	INTERFACE SYNTHESIS
Registration Number:	2577551	COWARE N2C
Registration Number:	2669389	COWARE

OP $140.00 2938869

CORRESPONDENCE DATA

Fax Number: (404)962-6736
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: (404) 885-3038
Email: michael.brignati@troutmansanders.com
Correspondent Name: MICHAEL J. BRIGNATI, PH.D.
Address Line 1: TROUTMAN SANDERS LLP
Address Line 2: 600 PEACHTREE STREET, N.E.
Address Line 4: ATLANTA, GEORGIA 30308-2216

ATTORNEY DOCKET NUMBER:	031372.000044
NAME OF SUBMITTER:	Michael J. Brignati, Ph.D.
Signature:	/Michael J. Brignati 60,890/
Date:	01/02/2008

Total Attachments: 5
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RELEASE OF SECURITY INTEREST IN INTELLECTUAL PROPERTY

THIS RELEASE OF SECURITY INTEREST IN INTELLECTUAL PROPERTY (the "Release") is made as of the 17th day of December 2007, between CoWare, Inc., a Delaware corporation ("Assignee") and Venture Lending & Leasing IV, Inc., a Maryland corporation (the "Assignor").

WHEREAS, in connection with certain loan documents, Assignee and Assignor entered into certain loan and security agreements (as amended, supplemented, or otherwise modified from time to time, the "Agreements") for the purpose of securing certain obligations of Assignee to Assignor;

WHEREAS, pursuant to the Agreements, Assignee granted the Assignor, for the benefit of the Assignor, a security interest in all of the Patents, Trademarks, and Copyrights (as defined in the Agreements) (collectively hereinafter the "Intellectual Property"), including the Patents, Trademarks, and Copyrights, identified on Exhibits A, B, and C, attached hereto, and pledged and mortgaged (but did not transfer title to) the Intellectual Property to Assignor; and

WHEREAS, all of the indebtedness and other obligations secured by the Assignor's security interest in the Intellectual Property have been repaid in their entirety, and the Assignor is therefore obligated to release its security interest in the Intellectual Property.

NOW, THEREFORE, for valuable consideration and pursuant to the terms and conditions set forth in the Agreements:

The Assignor hereby terminates and releases its security interest in the Intellectual Property, including without limitation, the Patents, Trademarks, and Copyrights identified on Exhibits A, B, and C attached hereto, and the Assignor hereby assigns and transfers to Assignee, without any representation, warranty, or recourse whatsoever, the Assignor's entire right, title, and interest in and to the Intellectual Property, effective as of the date set forth above.

Assignor hereby agrees to execute such further instruments and documents and perform such further acts as Assignee may deem necessary to secure to Assignee the rights herein conveyed.

"ASSIGNOR"

VENTURE LENDING & LEASING IV, INC.

By: _____

Name: Jay Cohan

Title: VP

EXHIBIT A TO RELEASE OF SECURITY INTEREST IN INTELLECTUAL PROPERTY

	A	B	C
1	**Title**	**Serial No.**	**Filing/Issue Date**
2	Method for determining an optimized data organization	6324629	11/27/01
3	METHOD AND SYSTEM FOR INSTRUCTION-SET ARCHITECTURE SIMULATION USING JUST IN TIME COMPILATION	10/309,554	12/3/02
4	METHOD AND SYSTEM FOR DEBUGGING A SYSTEM OF A CHIP DESIGN	10/410,116	4/8/03
5	AUTOMATIC GENERATION OF STRUCTURE AND CONTROL PATH USING HARDWARE DESCRIPTION LANGUAGE	10/641,457	8/14/03
6	AUTOMATIC GENERATION OF TRANSACTION LEVEL BUS SIMULATION INSTRUCTIONS FROM BUS PROTOCOL ESCRIPTION	10/700,601	11/3/03
7	METHOD OF PROTOCOL CONVERSION	10/700,600	11/3/03
8	GENERATION OF COMPILER DESCRIPTION FROM ARCHITECTURE DESCRIPTION	10/815,228	3/30/04
9	Resource Management in a multicore architecture	10/816,328	3/31/04
10	GENERATION OF INSTRUCTION SET FROM ARCHITECTURE DESCRIPTION	10/936,230	9/7/04
11	LARGE-SCALE FINITE STATE MACHINES	10/937,645	9/8/04
12	OUTPUT PARTITIONING OF LARGE-SCALE FINITE STATE MACHINES	10/937,161	9/8/04
13	DETERMING LARGE-SCALE FINITE STATE MACHINES USING CONSTRAINT RELAXATION	10/937,068	9/8/04
14	Debug in a multicore architecture	10/941,457	9/14/04
15	TRANSACTION LEVEL MODELING SYNTHESIS	10/976,402	10/28/04
16	INTERFACE CONVERTER FOR UNIFIED VIEW OF MULTIPLE COMPUTER SYSTEM SIMULATIONS	11/066,841	2/25/05
17	METHOD AND SYSTEM FOR DYNAMICALLY ADJUSTING SPEED VERSUS ACCURACY OF COMPUTER PLATFORM SIMULATION	11/066,945	2/25/05
18	PROCESSOR/MEMORY CO-EXPLORATION AT MULTIPLE ABSTRACTION LEVELS	11/069,496	2/28/05
19	EFFICIENT CLOCK MODELS AND THEIR USE IN SIMULATION	11/069,616	2/28/05
20	METHOD AND SYSTEM OF SCHEDULING INSTRUCTIONS	11/096,184	3/30/05

EXHIBIT A TO RELEASE OF SECURITY INTEREST IN INTELLECTUAL PROPERTY

	A	B	C
21	METHOD AND DEVICE FOR COMPILER RETARGETING BASED ON INSTRUCTION SEMANTIC MODELS	11/140,353	5/26/05
22	METHOD AND DEVICE FOR SIMULATOR GENERATION BASED ON SEMANTIC TO BEHAVIORAL TRANSLATION	11/139,373	5/26/05
23	METHOD AND SYSTEM FOR AUTOMATIC GENERATION OF INSTRUCTION-SET DOCUMENTATION FROM AN ABSTRACT 'ROCESSOR MODEL DESCRIBED USING AHIERARCHICAL RIPTION LANGUAGE	11/145,240	6/3/05
24	SCALABLE C++ LANGUAGE INFRASTRUCTURE FOR ESL TOOLS	11/356,578	12/22/05
25	CORXpert, A TECHNOLOGY AUTOMATING THE DESIGN OF INSTRUCTION-SET EXTENSIONS FOR PROCESSOR \RCHITECTURES	11/388,484	3/23/06
26	Scheduling in a multicore architecture	11/540,146	9/29/06
27	Managind Power Consumption in Multicore Processor	11/541,315	9/29/06
28	SIMULATING EXECUTION OF PROCESSOR INSTRUCTIONS	11/584,402	10/19/06
29	TECHNIQUES FOR CREATING AND USING A HIEARCHICAL DATA STRUCTURE	11/607,243	12/1/06
30	SYSTEM AND METHOD FOR ENHANCED DEBUGGING OF VIRTUAL PLATFORMS	60/874,436	12/11/06
31	A METHOD AND SYSTEM FOR INSTRUCTION SET SIMULATION WITH CONCURRENT ATTACHMENT OF MULTIPLE DEBUGGERS)ebug 2)	11/637,418	12/11/06
32	SYSTEM AND METHOD FOR STOPPING SIMULATION (Debug 1)	11/637,374	12/11/06
33	Debug 3: Cooperative coordination of debuggers attached to the same hardware	11/637,376	12/11/06
34	SIMULATION CONTROL TECHNIQUES	60/889,523	2/12/07
35	CONVERSION OF ALGORITHMIC SIMULATION MODELS TO ARCHITECTURAL MODELS	60/901,374	2/13/07
36	SIMULATION WITH DYNAMIC RUN-TIME ACCURACY ADJUSTMENT	11/707,412	2/16/07
37	simulation	11/707,413	2/16/07
38	CACHING INFORMATION TO MAP SIMULATION ADDRESSES TO HOST ADDRESSES IN COMPUTER SYSTEM SIMULATIONS	11/824,880	7/2/07
39	RUN-TIME SWITCHING FOR SIMULATION WITH DYNAMIC RUN-TIME ACCURACY ADJUSTMENT		

EXHIBIT B TO RELEASE OF SECURITY INTEREST IN INTELLECTUAL PROPERTY AGREEMENT

Trademark	Registration Number	Registration Date
COWARE	2,669,389	12/31/02
COWARE N2C	2,577,551	6/11/02
INTERFACE SYNTHESIS	2,780,613	11/4/03
CONVERGENSC	2,938,869	4/5/05
DIFFERENTIATE BY DESIGN	2,938,868	4/5/05

EXHIBIT C – COPYRIGHTS

NONE