TRADEMARK ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Formerly	Execution Date	Entity Type
Icera Inc.		11/22/2010	CORPORATION: DELAWARE

RECEIVING PARTY DATA

Name:	Silicon Valley Bank
Street Address:	275 Grove Street
Internal Address:	Suite 2-200
City:	Newton
State/Country:	MASSACHUSETTS
Postal Code:	02466
Entity Type:	CORPORATION: CALIFORNIA

PROPERTY NUMBERS Total: 10

Property Type	Number	Word Mark
Serial Number:	78736564	ARPEGGIO
Serial Number:	78736591	DXP
Serial Number:	85128238	ICE
Serial Number:	77880470	ICECLEAR
Serial Number:	78736603	ICERA
Serial Number:	78736588	ICERA
Serial Number:	85128232	ICERA ADAPTIVE WIRELESS
Serial Number:	78736611	ICERA SEMICONDUCTOR
Serial Number:	78736599	LIVANTO
Serial Number:	85128243	VIVALTO

CH $265.00 78736564

CORRESPONDENCE DATA

Fax Number: (202)408-3141

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

Phone:	800-927-9801 x2348
Email:	jpaterso@cscinfo.com
Correspondent Name:	Corporation Service Company
Address Line 1:	1090 Vermont Avenue NW, Suite 430
Address Line 4:	Washington, DISTRICT OF COLUMBIA 20005

ATTORNEY DOCKET NUMBER:	585374
NAME OF SUBMITTER:	Jean Paterson
Signature:	/jep/
Date:	11/22/2010

Total Attachments: 17
source=11-22-10 Icera-TM#page1.tif
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Form **PTO-1594** (Rev. 12-08)
OMB Collection 0651-0027 (exp. 01/31/2009)

U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

RECORDATION FORM COVER SHEET
TRADEMARKS ONLY

To the Director of the U. S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies):

ICERA INC.

☐ Individual(s) ☐ Association
☐ General Partnership ☐ Limited Partnership
☒ Corporation- State: Delaware
☐ Other

Citizenship (see guidelines) Delaware

Additional names of conveying parties attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies)

Additional names, addresses, or citizenship attached? ☐ Yes ☒ No

Name: Silicon Valley Bank
Internal Address:
Street Address: 275 Grove Street, Suite 2-200
City: Newton
State: MA
Country: USA Zip: 02466

☐ Association Citizenship
☐ General Partnership Citizenship
☐ Limited Partnership Citizenship
☒ Corporation Citizenship California
☐ Other Citizenship

If assignee is not domiciled in the United States, a domestic representative designation is attached: ☐ Yes ☐ No
(Designations must be a separate document from assignment)

3. Nature of conveyance)/Execution Date(s) :

Execution Date(s) November 22, 2010

☐ Assignment ☐ Merger
☒ Security Agreement ☐ Change of Name
☐ Other

4. Application number(s) or registration number(s) and identification or description of the Trademark.

A. Trademark Application No.(s)

See Exhibit C

B. Trademark Registration No.(s)

See Exhibit C

Additional sheet(s) attached? ☐ Yes ☒ No

C. Identification or Description of Trademark(s) (and Filing Date if Application or Registration Number is unknown):

See Exhibit C

5. Name & address of party to whom correspondence concerning document should be mailed:

Name: Corporation Service Company
Internal Address: Suite 210
Street Address: 1180 Avenue of the Americas
City: New York
State: NY Zip: 10036
Phone Number: 212-299-5600
Fax Number: 212-299-5656
Email Address: ORDER#

6. Total number of applications and registrations involved:

7. Total fee (37 CFR 2.6(b)(6) & 3.41) $

☐ Authorized to be charged to deposit account
☐ Enclosed

8. Payment Information:

Deposit Account Number
Authorized User Name

9. Signature:

Signature — November 22, 2010 Date

S. Ryan Black
Name of Person Signing

Total number of pages including cover sheet, attachments, and document: 17

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O. Box 1450, Alexandria, VA 22313-1450

INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement is entered into as of November 22, 2010 by and between **SILICON VALLEY BANK**, a California corporation, with a loan production office located at 275 Grove Street, Suite 2-200, Newton, Massachusetts 02466 ("Bank") and **ICERA INC.**, a Delaware corporation, with its principal place of business at 2520 The Quadrant, Aztec West, Bristol, BS32 4 AO, United Kingdom ("Grantor").

RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodations to Grantor (the "Loans") in the amounts and manner set forth in that certain Loan and Security Agreement by and among Bank, Grantor and Icera Semiconductor, Inc., dated as of November 22, 2010 (as the same may be amended, modified or supplemented from time to time, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in its Copyrights, Trademarks, Patents, and Mask Works (as each term is described below) to secure the obligations of Grantor under the Loan Agreement.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

To secure its obligations under the Loan Agreement, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its intellectual property (all of which shall collectively be called the "Intellectual Property Collateral"), including, without limitation, the following:

1. Any and all copyright rights, copyright applications, copyright registrations and like protections in each work or authorship and derivative work thereof, whether published or unpublished and whether or not the same also constitutes a trade secret, now or hereafter existing, created, acquired or held, including without limitation those set forth on Exhibit A attached hereto (collectively, the "Copyrights");

2. Any and all trade secrets, and any and all intellectual property rights in computer software and computer software products now or hereafter existing, created, acquired or held;

3. Any and all design rights that may be available to Grantor now or hereafter existing, created, acquired or held;

4. All patents, patent applications and like protections including, without limitation, improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the same, including without limitation the patents and patent applications set forth on Exhibit B attached hereto (collectively, the "Patents");

5. Any trademark and servicemark rights, whether registered or not, applications to register and registrations of the same and like protections, and the entire goodwill of the business of Grantor connected with and symbolized by such trademarks, including without limitation those set forth on Exhibit C attached hereto (collectively, the "Trademarks");

6. All mask works or similar rights available for the protection of semiconductor chips, now owned or hereafter acquired, including, without limitation those set forth on Exhibit D attached hereto (collectively, the "Mask Works");

7. Any and all claims for damages by way of past, present and future infringements of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above;

8. All licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works and all license fees and royalties arising from such use to the extent permitted by such license or rights;

9. All amendments, extensions, renewals and extensions of any of the Copyrights, Trademarks, Patents, or Mask Works; and

10. All proceeds and products of the foregoing, including, without limitation, all payments under insurance or any indemnity or warranty payable in respect of any of the foregoing.

This security interest is granted in conjunction with the security interest granted to Bank under the Loan Agreement. The rights and remedies of Bank with respect to the security interest granted hereby are in addition to those set forth in the Loan Agreement and the other Loan Documents, and those which are now or hereafter available to Bank as a matter of law or equity. Each right, power and remedy of Bank provided for herein or in the Loan Agreement or any of the Loan Documents, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right, power or remedy provided for herein and the exercise by Bank of any one or more of the rights, powers or remedies provided for in this Intellectual Property Security Agreement, the Loan Agreement or any of the other Loan Documents, or now or hereafter existing at law or in equity, shall not preclude the simultaneous or later exercise by any person, including Bank, of any or all other rights, powers or remedies.

[Signature page follows.]

TRADEMARK
REEL: 004419 FRAME: 0559

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

Address of Grantor:

ICERA INC.

2520 THE QUADRANT
AZTEC WEST BRISTOL

By: STAN BOLAND

Title: PRESIDENT T.C.E.O

Attn: STEVE CHANDLER

BANK:

Address of Bank:

SILICON VALLEY BANK

275 Grove Street, Suite 2-200
Newton, Massachusetts 02466

By:_____

Title:_____

Attn: Ms. Kate Leland

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

Address of Grantor:

ICERA INC.

_____

_____

By:_____

Title:_____

Attn: _____

BANK:

Address of Bank:

SILICON VALLEY BANK

275 Grove Street, Suite 2-200
Newton, Massachusetts 02466

By:_____

Title:_____

Attn: Ms. Kate Leland

EXHIBIT A

Copyrights

Description	Registration/ Application Number	Registration/ Application Date
None.		

EXHIBIT B

Patents

Description	Registration/ Application Number		Registration/Application Date
Single-Ray Channel Detection (3i-0001)	GB	1001389.4	28-Jan-10
Single Ray Channel Detection (3i-0001)	US	12/794211	04-Jun-10
LS Implementation (3i-0002)	GB	1001488.4	29-Jan-10
Hybrid Equalizer (3i-0003)	GB	1001469.4	29-Jan-10
Selected Interference Scenario (3i-0004)	US	12/848636	02-Aug-10
Dynamic Equalisation Length (A-0001-CN)	CN	[TBC]	26-Mar-09
Dynamic Equalisation Length (A-0001-EP)	EP	0972834.5	26-Mar-09
Dynamic Equalisation Length (A-0001-JP)	JP	[TBC]	26-Mar-09
Dynamic Equalisation Length (A-0001-TW)	TW	98108746	18-Mar-09
Dynamic Equalisation Length (A-0001-US)	US	12/935849	26-Mar-09
Dynamic Equalisation Length (A-0001-WO)	WO	PCT/EP2009/053603	26-Mar-09
Blind Transport/Format (A-0002-GB)	GB	1009581.8	11-Dec-08
Blind Transport/Format (A-0002-TW)	TW	97148451	12-Dec-08
Blind Transport/Format (A-0002-US)	US	12/808169	11-Dec-08
Blind Transport/Format (A-0002-WO)	WO	PCT/EP2008/067332	11-Dec-08
Multiple Transport Channels (A-0003-GB1)	GB	1009580	10-Dec-08
Multiple Transport Channels (A-0003-TW)	TW	97148468	12-Dec-08
Multiple Transport Channels (A-0003-US)	US	12/808167	10-Dec-08
Multiple Transport Channels (A-0003-WO)	WO	PCT/EP2008/067248	10-Dec-08
Anti-Winddown (A-0004-GB)	GB	1008970.4	11-Dec-08
Anti-Winddown (A-0004-TW)	TW	97148456	12-Dec-08
Anti-Winddown (A-0004-US)	US	12/808173	11-Dec-08
Anti-Winddown (A-0004-WO)	WO	PCT/EP2008/067310	11-Dec-08
Coarse Frequency Estimation (A-0005-CN)	CN	200880124582.7	24-Oct-08
Coarse Frequency Estimation (A-0005-EP)	EP	08847476.2	24-Oct-08
Coarse Frequency Estimation (A-0005-JP)	JP	2010-531501	24-Oct-08
Coarse Frequency Estimation (A-0005-TW)	TW	97140635	23-Oct-08
Coarse Frequency Estimation (A-0005-US)	US	12/741796	24-Oct-08
Coarse Frequency Estimation (A-0005-WO)	WO	PCT/EP2008/064473	24-Oct-08
Variable Instruction Set (A-0006/7-BR)	BR	PI0819926-4	12-Nov-08
Variable Instruction Set (A-0006/7-CN)	CN	200880120470.4	12-Nov-08
Variable Instruction Set (A-0006/7-EP)	EP	08859492.4	12-Nov-08
Variable Instruction Set (A-0006/7-IN)	IN	3913/DELNP/2010	12-Nov-08
Variable Instruction Set (A-0006/7-JP)	JP	2010-537353	12-Nov-08
Variable Instruction Set (A-0006/7-KR)	KR	10-2010-7015439	12-Nov-08

Variable Instruction Set (A-0006/7-TW)	TW	97145693	26-Nov-08
Variable Instruction Set (A-0006/7-US)	US	12/808175	12-Nov-08
Variable Instruction Set (A-0006/7-WO)	WO	PCT/EP2008/065420	12-Nov-08
RSSI Spectrum Estimation (A-0008-EP)	EP	08862589.2	11-Dec-08
RSSI Spectrum Estimation (A-0008-JP)	JP	2010-537451	11-Dec-08
RSSI Spectrum Estimation (A-0008-TW)	TW	97148465	12-Dec-08
RSSI Spectrum Estimation (A-0008-US)	US	12/808070	11-Dec-08
RSSI Spectrum Estimation (A-0008-WO)	WO	PCT/EP2008//067330	11-Dec-08
RSSI Spectrum Estimation (A-0008-WO CN)	CN	200880126890.3	11-Dec-08
STTD Channel Estimation (A-0009-GB)	GB	1009579.2	04-Dec-08
STTD Channel Estimation (A-0009-TW)	TW	97146272	28-Nov-08
STTD Channel Estimation (A-0009-US)	US	12/808157	04-Dec-08
STTD Channel Estimation (A-0009-WO)	WO	PCT/EP2008/066775	04-Dec-08
STTD SIR Estimation (A-0010-GB)	GB	1009576.8	04-Dec-08
STTD SIR Estimation (A-0010-TW)	TW	97145935	27-Nov-08
STTD SIR Estimation (A-0010-US)	US	12/808161	04-Dec-08
STTD SIR Estimation (A-0010-WO)	WO	PCT/EP2008/066768	04-Dec-08
Physical Channel Establishment (A-0011-CN)	CN	200880126855.1	28-Nov-08
Physical Channel Establishment (A-0011-EP)	EP	08862721.1	28-Nov-08
Physical Channel Establishment (A-0011-JP)	JP	2010-537374	28-Nov-08
Physical Channel Establishment (A-0011-TW)	TW	97145694	26-Nov-08
Physical Channel Establishment (A-0011-US)	US	12/808050	28-Nov-08
Physical Channel Establishment (A-0011-WO)	WO	PCT/EP2008/066453	28-Nov-08
Crystal Frequency Discovery (A-0014.1-GB)	GB	0807924.6	30-Apr-08
Crystal Frequency Discovery (A-0014.1-US)	US	12/428728	23-Apr-09
Boot Source Discovery (A-0014.2-US)	US	12/580249	15-Oct-09
Clock Gear Box (A-0016/B69.US)	US	11/957352	14-Dec-07
Go-Slow Bits (A-0017-GB)	GB	0722967.7	22-Nov-07
Go-Slow Bits (A-0017-US)	US	12/275375	21-Nov-08
Low Voltage SRAM Writeability (A-0019-GB)	GB	0724420.5	14-Dec-07
Kasumi Block (A-0020-GB)	GB	1011024.5	28-Nov-08
Kasumi Block (A-0020-WO)	WO	PCT/EP2008/066475	28-Nov-08
NAND FLASH (A-0022/23)	GB	0723316.6	28-Nov-07
NAND FLASH (A-0022/23-US)	US	12/323563	26-Nov-08
Smart Card Module (A-0024-GB)	GB	0920858.8	11-Jul-08
Smart Card Module (A-0024-US)	US	12/668404	11-Jul-08
Smart Card Module (A-0024-WO)	WO	PCT/EP2008/059116	11-Jul-08
SIR-based Processing (B-0026-CN)	CN	200980109472.8	27-Feb-09
SIR-based Processing (B-0026-EP)	EP	09721711.1	27-Feb-09
SIR-based Processing (B-0026-JP)	JP	[TBC]	27-Feb-09
SIR-based Processing (B-0026-TW)	TW	98106399	27-Feb-09
SIR-based Processing (B-0026-US)	US	12/933377	27-Feb-09
SIR-based Processing (B-0026-WO)	WO	PCT/EP2009/052360	27-Feb-09

TRADEMARK
REEL: 004419 FRAME: 0564

Ramp Control Voltage (B-0031.1-US)	US	12/703319	10-Feb-10
Ramp Control Voltage (B-0031.3-GB)	GB	0902348.2	12-Feb-09
IPP V.2 (B-0033-WO)	WO	PCT/EP2010/058315	14-Jun-10
FLEXIBLE INTERFACE (B-0034-GB)	GB	0724178.9	11-Dec-07
FLEXIBLE INTERFACE (B-0034-US)	US	12/330905	09-Dec-08
Voltage Level Shifter (B-0035-GB)	GB	0724441.1	14-Dec-07
Voltage Level Shifter (B-0035-US)	US	12/331718	10-Dec-08
Viterbi Traceback Instruction (B-0044-GB)	GB	1010462.8	04-Dec-08
Viterbi Traceback Instruction (B-0044-WO)	WO	PCT/EP2008/066779	04-Dec-08
DMA Ping-Pong Context Pairing (B-0045.1-GB)	GB	0808987.2	16-May-08
DMA Ping-Pong Context Pairing (B-0045.1-US)	US	12/466038	14-May-09
DMA Delay Per Descriptor (B-0045.3-WO)	WO	PCT/EP2009/056371	26-May-09
DMA Driven Read (B-0045.5-GB)	GB	0900758.4	16-Jan-09
DMA Driven Read (B-0045.5-US)	US	12/643674	21-Dec-09
Die ID Encryption (B-0048-GB)	GB	1010340.6	15-Dec-08
Die ID Encryption (B-0048-WO)	WO	PCT/EP2008/067573	15-Dec-08
DEBUG COUNT (B-0056-GB)	GB	0808360.2	08-May-08
DEBUG COUNT (B-0056-US)	US	12/437081	07-May-09
Configurable Boot Mechanism (B-0063-USa)	US	12/127131	27-May-08
NON-RESET DEVICES (B-0065-GB)	GB	0724422.1	14-Dec-07
NON-RESET DEVICES (B-0065-US)	US	12/328952	05-Dec-08
HRL DMA Engine (B-0067-GB)	GB	1011025.2	04-Dec-08
HRL DMA Engine (B-0067-WO)	WO	PCT/EP2008/066781	04-Dec-08
DDR Interface (B-0070-US)	US	11/967540	31-Dec-07
SPI Format (B-0075-GB)	GB	0807503.8	24-Apr-08
SPI Format (B-0075-US)	US	12/425471	17-Apr-09
LLR (EX-0003-WO)	WO	PCT/EP2010/058796	22-Jun-10
Memory Cell (FS-0001-CN)	CN	200880124130.9	24-Oct-08
Memory Cell (FS-0001-EP)	EP	08847755.9	24-Oct-08
Memory Cell (FS-0001-JP)	JP	2010-532542	24-Oct-08
Memory Cell (FS-0001-TW)	TW	97140637	23-Oct-08
Memory Cell (FS-0001-US)	US	12/810786	24-Oct-08
Memory Cell (FS-0001-WO)	WO	PCT/EP2008/064459	24-Oct-08
CQI Slope Data (FS-0002-BR)	BR	PI 0815537-2	18-Aug-08
CQI Slope Data (FS-0002-CN)	CN	200880103656.9	18-Aug-08
CQI Slope Data (FS-0002-EP)	EP	08787287.5	18-Aug-08
CQI Slope Data (FS-0002-IN)	IN	24/DELNP/2010	18-Aug-08
CQI Slope Data (FS-0002-JP)	JP	2010-521407	18-Aug-08
CQI Slope Data (FS-0002-KR)	KR	10-2010-7001833	18-Aug-08
CQI Slope Data (FS-0002-US)	US	12/673568	18-Aug-08
CQI Slope Data (FS-0002-WO)	WO	PCT/EP2008/060804	18-Aug-08
LTE CQI (FS-0003(a)-GB)	GB	0721188.1	29-Oct-07
LTE CQI (FS-0003(b)-EP)	EP	10176887.7	18-Sep-08

TRADEMARK
REEL: 004419 FRAME: 0565

LTE CQI (FS-0003(b)-US)	US	12/739587	18-Sep-08
LTE CQI (FS-0003-BR)	BR	PI 0818682-0	18-Sep-08
LTE CQI (FS-0003-CN)	CN	200880123168.4	18-Sep-08
LTE CQI (FS-0003-EP)	EP	08804397.1	18-Sep-08
LTE CQI (FS-0003-IN)	IN	3329/DELNP/2010	18-Sep-08
LTE CQI (FS-0003-JP)	JP	2010-530376	18-Sep-08
LTE CQI (FS-0003-KR)	KR	10-2010-7011167	18-Sep-08
LTE CQI (FS-0003-TW)	TW	97136648	24-Sep-08
LTE CQI (FS-0003-WO)	WO	PCT/EP2008/062460	18-Sep-08
PMI FEEDBACK (FS-0004(b)-GB)	GB	0805813.3	31-Mar-08
PMI FEEDBACK (FS-0004-BR)	BR	[TBC]	08-Jan-09
PMI FEEDBACK (FS-0004-CN)	CN	200980108348.X	08-Jan-09
PMI FEEDBACK (FS-0004-EP)	EP	09700917.9	08-Jan-09
PMI FEEDBACK (FS-0004-IN)	IN	5585/DELNP/2010	08-Jan-09
PMI FEEDBACK (FS-0004-JP)	JP	[TBC]	08-Jan-09
PMI FEEDBACK (FS-0004-KR)	KR	10-2010-7017698	08-Jan-09
PMI FEEDBACK (FS-0004-TW)	TW	98100487	08-Jan-09
PMI FEEDBACK (FS-0004-US)	US	12/812362	08-Jan-09
PMI FEEDBACK (FS-0004-WO)	WO	PCT/EP2009/050184	08-Jan-09
Estimation of Transmit Signal (FS-0005-GB1)	GB	[TBC]	26-May-09
Estimation of Transmit Signal (FS-0005-US)	US	[TBC]	26-May-09
Estimation of Transmit Signal (FS-0005-WO)	WO	PCT/EP2009/056375	26-May-09
I-Cache Optimiser (FS-0006-GB)	GB	0818165.3	03-Oct-08
I-Cache Optimiser (FS-0006-US)	US	12/572836	02-Oct-09
MIMO SIR Estimation (FS-0007-WO)	WO	PCT/EP2009/057566	18-Jun-09
Drop of RI Transmission (FS-0008-GB)	GB	0814495.8	07-Aug-08
Drop of RI Transmission (FS-0008-TW)	TW	98113454	23-Apr-09
Drop of RI Transmission (FS-0008-WO)	WO	PCT/EP2009/054460	15-Apr-09
Software Activation (FS-0009-WO)	WO	PCT/EP2010/054784	13-Apr-10
Slot Based APM (FS-0010-TW)	TW	98118916	06-Jun-09
Slot Based APM (FS-0010-WO)	WO	PCT/EP2009/056634	29-May-09
CMOS Metastability Resolving (FS-0011-GB)	GB	0903687.2	03-Mar-09
CMOS Metastability Resolving (FS-0011-US)	US	12/713412	26-Feb-10
TPC Symbols (FS-0012-WO)	WO	PCT/EP2010/053959	25-Mar-10
Standard Agnostic Adaption (FS-0013-GB)	GB	0912581.6	20-Jul-09
Standard Agnostic Adaptation (FS-0013-WO)	WO	PCT/EP2010/053994	26-Mar-10
Sync Channel Cancellation (FS-0014)	WO	PCT/EP2010/061102	30-Jul-10
Low Complexity Interpolation (FS-0015)	US	12/889035	23-Sep-10
Windowed Log MAP (FS-0015-WO)	WO	PCT/EP2010/062515	26-Aug-10
Low Complexity Interpolation (FS-0016-GB)	GB	0916913.7	25-Sep-09
High Resolution Digital (ICL-0001-GB)	GB	1005764.4	07-Apr-10
Selectable Noise Whitener (ICL-0002-GB)	GB	1003703.4	05-Mar-10
Partitioning of IP Block (ICL-0003-GB)	GB	1005983	09-Apr-10

TRADEMARK
REEL: 004419 FRAME: 0566

Selected Interference Scenario (ICL-0004-GB)	GB	1001482.7	29-Jan-10
3GPP Priority Mechanism (ICX-0001-WO)	WO	PCT/EP2010/064942	06-Oct-10
Fast Fading (ICX-0002-WO)	WO	PCT/EP2010/066069	25-Oct-10
Dual Channel Processor (ICX-0003-GB)	GB	1014318.8	27-Aug-10
Ordered SIC Decoding (ICX-0004-GB)	GB	1006103.4	13-Apr-10
Selective SIC Decoding (ICX-0004-GB2)	GB	1006104.2	13-Apr-10
Independent MIMO streams (ICX-0004-GB3)	GB	1006105.9	13-Apr-10
LTC PRACH (ICX-0005-GB)	GB	1005319.7	30-Mar-10
Bypass of Secure Boot (ICX-0006-GB)	GB	1002403.2	12-Feb-10
DFLL For Vivalto (ICX-0007-GB)	GB	1003030.2	23-Feb-10
Crash and Reboot (ICX-0008-GB)	GB	1003017.9	23-Feb-10
PAR Limiter (ICX-0009-GB)	GB	1014659.5	03-Sep-10
Transport Block Size (ICX-0010-GB)	GB	1013039.1	03-Aug-10
Decoding Reliability (MC-0001-EP)	EP	06849424.4	26-Jun-06
Decoding Reliability (MC-0001-EP-DE)	DE	06849424.4	26-Jun-06
Decoding Reliability (MC-0001-EP-FR)	FR	06849424.4	26-Jun-06
Decoding Reliability (MC-0001-EP-GB)	GB	06849424.4	26-Jun-06
Decoding Reliability (MC-0001-EP-NL)	NL	06849424.4	26-Jun-06
Decoding Reliability (MC-0001-JP)	JP	2008-517611	26-Jun-06
Decoding Reliability (MC-0001-US)	US	11/168642	27-Jun-05
Configurable Processing (MWE-0001-BR)	BR	PI0611659-0	04-May-06
Configurable Processing (MWE-0001-CN)	CN	200680024524.8	04-May-06
Configurable Processing (MWE-0001-EP)	EP	06727002.5	04-May-06
Configurable Processing (MWE-0001-IN)	IN	1802/MUMNP/2007	04-May-06
Configurable Processing (MWE-0001-JP)	JP	2008-509504	04-May-06
Configurable Processing (MWE-0001-KR)	KR	7028459/2007	04-May-06
Configurable Processing (MWE-0001-TW)	TW	95116018	05-May-06
Configurable Processing (MWE-0001-US)	US	11/122385	05-May-05
Configurable Processing (MWE-0001-WO)	WO	PCT/GB2006/001629	04-May-06
Turbo Decoder (MWE-0003-AU)	AU	2004231907	13-Apr-04
Turbo Decoder (MWE-0003-CN)	CN	200480016302.2	13-Apr-04
Turbo Decoder (MWE-0003-EP)	EP	04727039.2	13-Apr-04
Turbo Decoder (MWE-0003-JP)	JP	2006-506117	13-Apr-04
Turbo Decoder (MWE-0003-TW)	TW	93108644	30-Mar-04
Turbo Decoder (MWE-0003-US)	US	10/825212	16-Apr-04
Turbo Decoder (MWE-0003-USP)	US	60/463344	17-Apr-03
Turbo Decoder (MWE-0003-WO)	WO	PCT/GB2004/001588	13-Apr-04
Register Access (MWE-0004-BR)	BR	PI0609742-1	06-Apr-06
Register Access (MWE-0004-CN)	CN	200680011240.5	06-Apr-06
Register Access (MWE-0004-EP)	EP	06726668.4	06-Apr-06
Register Access (MWE-0004-IN)	IN	1577/MUMNP/2007	06-Apr-06
Register Access (MWE-0004-JP)	JP	2008-504843	06-Apr-06
Register Access (MWE-0004-KR)	KR	7022857/2007	06-Apr-06

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Register Access (MWE-0004-TW)	TW	95112369	07-Apr-06
Register Access (MWE-0004-US)	US	11/102266	08-Apr-05
Register Access (MWE-0004-WO)	WO	PCT/GB2006/001265	06-Apr-06
Log-Likelihood Ratios (MWE-0005-CN)	CN	200580045896.4	11-Oct-05
Log-Likelihood Ratios (MWE-0005-EP)	EP	05791641.3	11-Oct-05
Log-Likelihood Ratios (MWE-0005-JP)	JP	2007-539624	11-Oct-05
Log-Likelihood Ratios (MWE-0005-KR)	KR	7010397/2007	11-Oct-05
Log-Likelihood Ratios (MWE-0005-TW)	TW	94135862	14-Oct-05
Log-Likelihood Ratios (MWE-0005-US)	US	11/258385	26-Oct-05
Log-Likelihood Ratios (MWE-0005-USP)	US	60/625126	05-Nov-04
Log-Likelihood Ratios (MWE-0005-WO)	WO	PCT/GB2005/003917	11-Oct-05
Excess Current Leakage (MWE-0006-EP)	EP	06709806.1	17-Feb-06
Excess Current Leakage (MWE-0006-JP)	JP	2007-556649	17-Feb-06
Excess Current Leakage (MWE-0006-TW)	TW	95105359	17-Feb-06
Excess Current Leakage (MWE-0006-US)	US	11/065904	24-Feb-05
Excess Current Leakage (MWE-0006-WO)	WO	PCT/GB2006/000569	17-Feb-06
Aligned Logic Cell Grid (MWE-0007-EP)	EP	06709809.5	17-Feb-06
Aligned Logic Cell Grid (MWE-0007-JP)	JP	2007-556650	17-Feb-06
Aligned Logic Cell Grid (MWE-0007-TW)	TW	95105355	17-Feb-06
Aligned Logic Cell Grid (MWE-0007-US)	US	11/066041	24-Feb-05
Aligned Logic Cell Grid (MWE-0007-WO)	WO	PCT/GB2006/000573	17-Feb-06
Transistor Performance (MWE-0008-EP)	EP	06709805.3	17-Feb-06
Transistor Performance (MWE-0008-JP)	JP	2007-556648	17-Feb-06
Transistor Performance (MWE-0008-TW)	TW	95105363	17-Feb-06
Transistor Performance (MWE-0008-US)	US	11/067200	24-Feb-05
Transistor Performance (MWE-0008-WO)	WO	PCT/GB2006/000568	17-Feb-06
Dual Data Path Processing (MWE-0009-CN)	CN	200580010665.X	22-Mar-05
21-Bit Instruction (MWE-0009-CN1)	CN	201010276291.9	22-Mar-05
Dual Data Path Processing (MWE-0009-EP)	EP	05729261.7	22-Mar-05
Dual Data Path Processing (MWE-0009-JP)	JP	2007-505615	22-Mar-05
Dual Data Path Processing (MWE-0009-KR)	KR	7020243/2006	22-Mar-05
Dual Data Path Processing (MWE-0009-TW)	TW	94109120	24-Mar-05
Dual Data Path Processing (MWE-0009-US)	US	10/813433	31-Mar-04
Dual Data Path Processing (MWE-0009-WO)	WO	PCT/GB2005/001073	22-Mar-05
Asymmetric Dual Path (MWE-0010-CN)	CN	200580017666.7	22-Mar-05
Asymmetric Dual Path (MWE-0010-EP)	EP	05729258.3	22-Mar-05
Asymmetric Dual Path (MWE-0010-JP)	JP	2007-505614	22-Mar-05
Asymmetric Dual Path (MWE-0010-KR)	KR	7020245/2006	22-Mar-05
Asymmetric Dual Path (MWE-0010-TW)	TW	94109122	24-Mar-05
Asymmetric Dual Path (MWE-0010-US)	US	10/813615	31-Mar-04
Asymmetric Dual Path (MWE-0010-WO)	WO	PCT/GB2005/001069	22-Mar-05
Control Processor (MWE-0011-CN)	CN	200580010660.7	22-Mar-05
Control Processor (MWE-0011-EP)	EP	05729441.5	22-Mar-05

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21 Bit Instruction (MWE-0011-EP DIV)	EP	10177669.8	22-Mar-05
Control Processor (MWE-0011-JP)	JP	2007-505612	22-Mar-05
21 Bit Instructions (MWE-0011-JP-DIV)	JP	[TBC]	22-Mar-05
Control Processor (MWE-0011-KR)	KR	7020244/2006	22-Mar-05
Control Processor (MWE-0011-TW)	TW	94109124	24-Mar-05
21 Bit Instruction (MWE-0011-TW-DIV)	TW	[TBC]	24-Mar-05
Control Processor (MWE-0011-US)	US	10/813628	31-Mar-04
21 Bit Instruction (MWE-0011-US-DIV)	US	[TBC]	[TBC]
Control Processor (MWE-0011-WO)	WO	PCT/GB2005/001059	22-Mar-05
Blind Format Detection (O-0001-CN)	CN	200880022753.5	20-Jun-08
Blind Format Detection (O-0001-EP)	EP	08774185.6	20-Jun-08
Blind Format Detection (O-0001-JP)	JP	2010-513868	20-Jun-08
Blind Format Detection (O-0001-US)	US	12/667142	20-Jun-08
Blind Format Detection (O-0001-WO)	WO	PCT/EP2008/057889	20-Jun-08
Reliability of Received Data (O-0002-US)	US	11/812116	15-Jun-07
Adaptive Parameter Selection (PS-0001-CN)	CN	200880122994.7	24-Oct-08
Adaptive Parameter Selection (PS-0001-EP)	EP	08844815.4	24-Oct-08
Adaptive Parameter Selection (PS-0001-JP)	JP	2010-531498	24-Oct-08
Adaptive Parameter Selection (PS-0001-TW)	TW	97140625	23-Oct-08
Adaptive Parameter Selection (PS-0001-US)	US	12/016640	18-Jan-08
Adaptive Parameter Selection (PS-0001-WO)	WO	PCT/EP2008/064461	24-Oct-08
Adaptive Parameter Selection (PS-0002-EP)	EP	08843584.7	24-Oct-08
Adaptive Parameter Selection (PS-0002-TW)	TW	97140622	23-Oct-08
Adaptive Parameter Selection (PS-0002-US)	US	12/016629	18-Jan-08
Adaptive Parameter Selection (PS-0002-WO)	WO	PCT/EP2008/064464	24-Oct-08
Receive Diversity (PS-0003-BR)	BR	PI0818149-7	24-Oct-08
Receive Diversity (PS-0003-CN)	CN	200880123547.3	24-Oct-08
Receive Diversity (PS-0003-EP)	EP	08845079.6	24-Oct-08
Receive Diversity (PS-0003-IN)	IN	3328/DELNP/2010	24-Oct-08
Receive Diversity (PS-0003-JP)	JP	2010-531502	24-Oct-08
Receive Diversity (PS-0003-KR)	KR	10-2010-7012015	24-Oct-08
Receive Diversity (PS-0003-TW)	TW	97140624	23-Oct-08
Receive Diversity (PS-0003-US)	US	12/016688	18-Jan-08
Receive Diversity (PS-0003-WO)	WO	PCT/EP2008/064474	24-Oct-08
Processing Resources (PS-0004-BR)	BR	PI0818123-3	24-Oct-08
Processing Resources (PS-0004-CN)	CN	200880122748.1	24-Oct-08
Processing Resources (PS-0004-EP)	EP	08843736.3	24-Oct-08
Processing Resources (PS-0004-IN)	IN	3577/DELNP/2010	24-Oct-08
Processing Resources (PS-0004-JP)	JP	2010-531500	24-Oct-08
Processing Resources (PS-0004-KR)	KR	10-2010-7012019	24-Oct-08
Processing Resources (PS-0004-TW)	TW	97140629	23-Oct-08
Processing Resources (PS-0004-US)	US	12/016671	18-Jan-08
Processing Resources (PS-0004-WO)	WO	PCT/EP2008/064472	24-Oct-08

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LIVANTO ADAPTION (PS-0005-CN)	CN	200880123546.9	24-Oct-08
LIVANTO ADAPTION (PS-0005-EP)	EP	08844348.6	24-Oct-08
LIVANTO ADAPTION (PS-0005-JP)	JP	2010-531499	24-Oct-08
LIVANTO ADAPTION (PS-0005-TW)	TW	97140636	23-Oct-08
LIVANTO ADAPTION (PS-0005-US)	US	12/016681	18-Jan-08
LIVANTO ADAPTION (PS-0005-WO)	WO	PCT/EP2008/064467	24-Oct-08
Monitoring Specific Channel (PS-0006-EP)	EP	08843940.1	24-Oct-08
Monitoring Specific Channel (PS-0006-TW)	TW	97140628	23-Oct-08
Monitoring Channel Conditions (PS-0006-US)	US	12/016652	18-Jan-08
Monitoring Specific Channel (PS-0006-WO)	WO	PCT/EP2008/064468	24-Oct-08
Geometry Estimation Algorithm (PS-0007-EP)	EP	08846072.0	24-Oct-08
Geometry Estimation Algorithm (PS-0007-GB1)	GB	1007027.4	24-Oct-08
Geometry Estimation Algorithm (PS-0007-TW)	TW	97140631	23-Oct-08
Geometry Estimation Algorithm (PS-0007-US)	US	12/016663	18-Jan-08
Geometry Estimation Algorithm (PS-0007-WO)	WO	PCT/EP2008/064471	24-Oct-08

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EXHIBIT C

Trademarks

Description		Registration/ Application Number	Registration/ Application Date
ARPEGGIO	EU	4633673	05/10/2005
ARPEGGIO	USA	78/736564	19/10/2005
DEEP EXECUTION	EU	4401014	22/04/2005
Deep Execution Processor	Japan	2005-099487	24/10/2005
DXP	Brazil	[TBC]	[TBC]
DXP	EU	4401469	22/04/2005
DXP	India	2015256	27/08/2010
DXP	International (Australia, China, South Korea)	[TBC]	27/08/2010
DXP	Taiwan	99043082	31/08/2010
DXP	USA	78/736591	19/10/2005
ESPRESSO	International (USA, EU)	914891	08/12/2006
ESPRESSO	United Kingdom	2438499	15/11/2006
ICE	EU	9335671	26/08/2010
ICE	USA	85/128238	13/09/2010
ICECLEAR	EU	8676975	10/11/2009
ICECLEAR	USA	77/880470	25/11/2009
ICERA	Brazil	[TBC]	[TBC]
ICERA	EU	4400982	22/04/2005
ICERA	India	2015255	27/08/2010
ICERA	International (Australia, China, South Korea)	1050710	27/08/2010
ICERA	Japan	2005-099482	24/10/2005
ICERA	Taiwan	99043081	31/08/2010
ICERA	USA	78/736603	19/10/2005
ICERA & Logo	Japan	2005-099484	24/10/2005
ICERA & Logo	USA	78/736588	19/10/2005
ICERA ADAPTIVE WIRELESS	EU	9335696	26/08/2010
ICERA ADAPTIVE WIRELESS	USA	85/128232	13/09/2010
ICERA Logo	EU	4554499	22/08/2005
ICERA SEMICONDUCTOR	EU	4400842	22/04/2005
ICERA SEMICONDUCTOR	Japan	2005-099483	24/10/2005
ICERA SEMICONDUCTOR	USA	78/736611	19/10/2005
LIVANTO	EU	4400784	22/04/2005
LIVANTO	Japan	2005-099485	24/10/2005
LIVANTO	USA	78/736599	19/10/2005

SEMICONDUCTOR icera (stylised)	Japan	2004-058075	23/06/2004
VIVALTO	EU	9335654	26/08/2010
Vivalto	USA	85/128243	13/09/2010

EXHIBIT D

Mask Works

Description	Registration/ Application Number	Registration/ Application Date
None.		

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